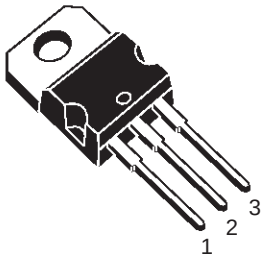
STP100NF04L

N-CHANNEL 40V - 0.0036Ω - 100A TO-220
STripFET™ POWER MOSFET

PRELIMINARY DATA

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STP100NF04L	40 V	< 0.0042 Ω	100 A

- TYPICAL $R_{DS}(on)$ = 0.0036Ω
- LOW THRESHOLD DRIVE
- 100% AVALANCHE TESTED
- LOGIC LEVEL DEVICE
- FOR THROUGH-HOLE VERSION CONTACT SALES OFFICE

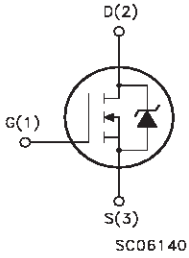


TO-220

DESCRIPTION

This Power Mosfet is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalance characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

INTERNAL SCHEMATIC DIAGRAM



APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- MOTOR CONTROL, AUDIO AMPLIFIERS
- DC-DC & DC-AC CONVERTERS
- SOLENOID AND RELAY DRIVERS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	40	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	40	V
V_{GS}	Gate- source Voltage	±20	V
I_D	Drain Current (continuos) at T_C = 25°C	100	A
I_D	Drain Current (continuos) at T_C = 100°C	70	A
I_{DM} (●)	Drain Current (pulsed)	400	A
P_{TOT}	Total Dissipation at T_C = 25°C	210	W
	Derating Factor	1.43	W/°C
E_{AS} (1)	Single Pulse Avalanche Energy	1.4	mJ
T_{stg}	Storage Temperature	–65 to 175	°C
T_j	Max. Operating Junction Temperature	175	°C

(●) Pulse width limited by safe operating area

(1) Starting T_j = 25°C, I_{AR} = 50A, V_{DD}=50 V

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	0.7	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose	300	°C

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0	40			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating			1	µA
		V_{DS} = Max Rating, T_C = 125 °C			10	µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ±20V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250µA	1			V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10 V, I_D = 50 A		0.0036	0.0042	Ω
		V_{GS} = 4.5 V, I_D = 50 A		0.0040	0.0065	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$, I_D =15 A		60		S
C_{iss}	Input Capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		6400		pF
C_{oss}	Output Capacitance			1300		pF
C_{rss}	Reverse Transfer Capacitance			190		pF

ELECTRICAL CHARACTERISTICS (CONTINUED)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	V_{DD} = 20V, I_D = 50A		37		ns
t_r	Rise Time	R_G = 4.7Ω V_{GS} = 4.5V (see test circuit, Figure 3)		270		ns
Q_g	Total Gate Charge	V_{DD} = 32 V, I_D = 100A,		72	97	nC
Q_{gs}	Gate-Source Charge	V_{GS} = 4.5V		20		nC
Q_{gd}	Gate-Drain Charge			28.5		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off-Delay Time	V_{DD} = 20V, I_D = 50A,		90		ns
t_f	Fall Time	R_G = 4.7Ω, V_{GS} = 4.5V (see test circuit, Figure 5)		80		ns
$t_{d(off)}$	Off-voltage Rise Time	Vclamp =32V, I_D =100A		85		ns
t_f	Fall Time	R_G = 4.7Ω, V_{GS} = 4.5V		125		ns
t_c	Cross-over Time			160		ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				100	A
I_{SDM} (2)	Source-drain Current (pulsed)				400	A
V_{SD} (1)	Forward On Voltage	I_{SD} = 100A, V_{GS} = 0			1.3	V
t_{rr}	Reverse Recovery Time	I_{SD} = 100A, di/dt = 100A/µs,		88		ns
Q_{rr}	Reverse Recovery Charge	V_{DD} = 20V, T_j = 150°C		240		nC
I_{RRM}	Reverse Recovery Current	(see test circuit, Figure 5)		5.5		A

Note: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

Fig. 1: Unclamped Inductive Load Test Circuit

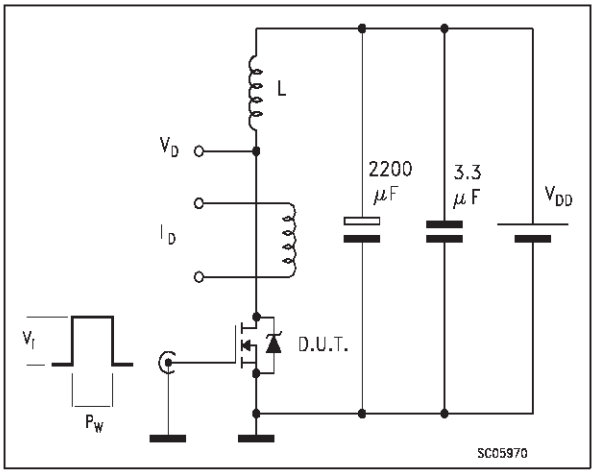


Fig. 2: Unclamped Inductive Waveform

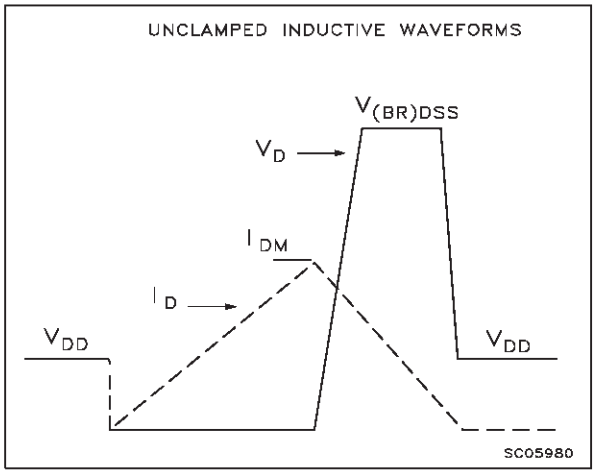


Fig. 3: Switching Times Test Circuit For Resistive Load

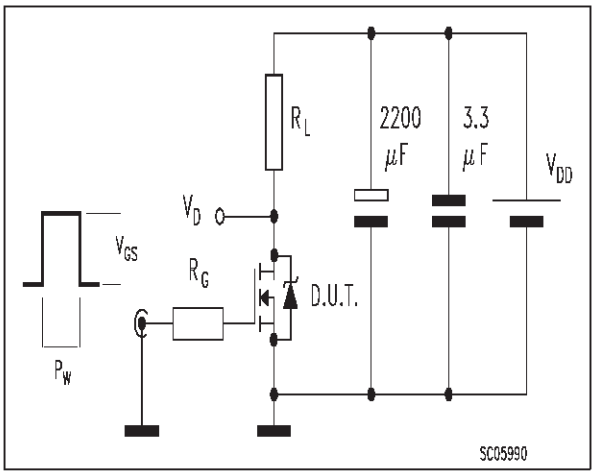


Fig. 4: Gate Charge test Circuit

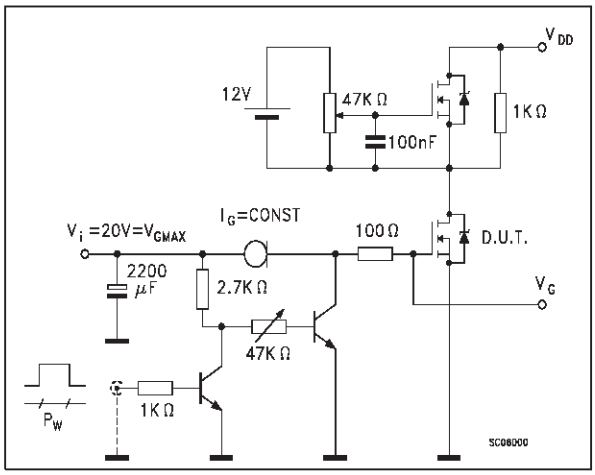
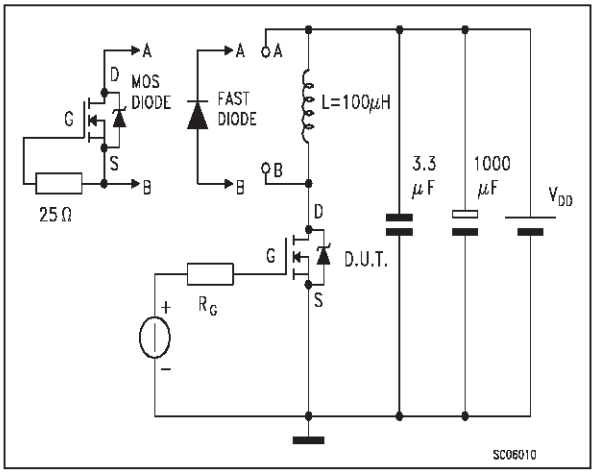


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-220 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
D1		1.27			0.050	
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.2		6.6	0.244		0.260
L9	3.5		3.93	0.137		0.154
DIA.	3.75		3.85	0.147		0.151