



STB100NF04L

N-CHANNEL 40V - 0.0036Ω - 100A D2PAK

STripFET™ POWER MOSFET

PRELIMINARY DATA

TYPE	V _{DSS}	R _{DS(on)}	I _D
STB100NF04L	40 V	< 0.0042 Ω	100 A

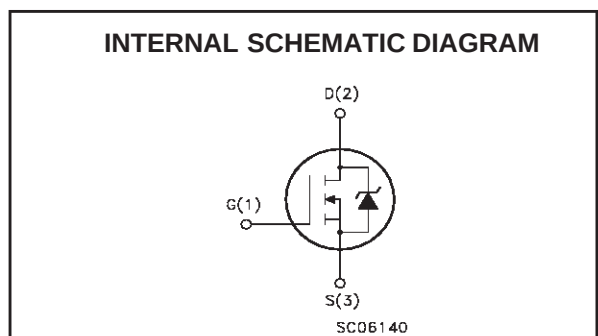
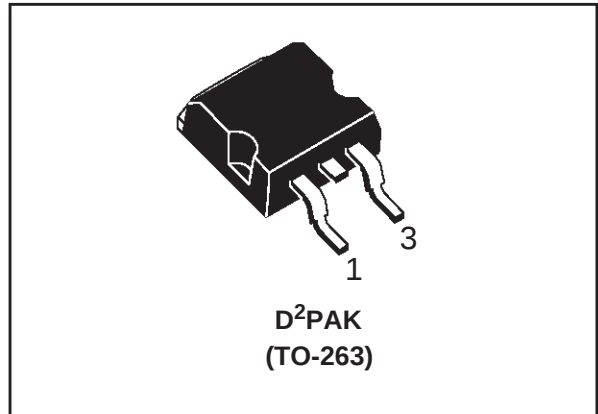
- TYPICAL R_{DS(on)} = 0.0036Ω
- LOW THRESHOLD DRIVE
- 100% AVALANCHE TESTED
- LOGIC LEVEL DEVICE
- FOR THROUGH-HOLE VERSION CONTACT SALES OFFICE

DESCRIPTION

This Power Mosfet is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- MOTOR CONTROL, AUDIO AMPLIFIERS
- DC-DC & DC-AC CONVERTERS
- SOLENOID AND RELAY DRIVERS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	40	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	40	V
V _{GS}	Gate- source Voltage	± 20	V
I _D	Drain Current (continuous) at T _C = 25°C	100	A
I _D	Drain Current (continuous) at T _C = 100°C	70	A
I _{DM} (●)	Drain Current (pulsed)	400	A
P _{TOT}	Total Dissipation at T _C = 25°C	210	W
	Derating Factor	1.43	W/°C
E _{AS} (1)	Single Pulse Avalanche Energy	1.4	mJ
T _{stg}	Storage Temperature	-65 to 175	°C
T _j	Max. Operating Junction Temperature	175	°C

(●) Pulse width limited by safe operating area

(1) Starting T_j = 25°C, I_{AR} = 50A, V_{DD} = 50 V

STB100NF04L

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	0.7	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5	°C/W
T _I	Maximum Lead Temperature For Soldering Purpose	300	°C

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 µA, V _{GS} = 0	40			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125 °C			1 10	µA µA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ±20V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250µA	1			V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10 V, I _D = 50 A V _{GS} = 4.5 V, I _D = 50 A		0.0036 0.0040	0.0042 0.0065	Ω Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (1)	Forward Transconductance	V _{DS} > I _{D(on)} × R _{DS(on)max} , I _D = 15 A		60		S
C _{iss}	Input Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		6400		pF
C _{oss}	Output Capacitance			1300		pF
C _{rss}	Reverse Transfer Capacitance			190		pF

ELECTRICAL CHARACTERISTICS (CONTINUED)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 20V, I_D = 50A$		37		ns
t_r	Rise Time	$R_G = 4.7\Omega, V_{GS} = 4.5V$ (see test circuit, Figure 3)		270		ns
Q_g	Total Gate Charge	$V_{DD} = 32V, I_D = 100A,$		72	97	nC
Q_{gs}	Gate-Source Charge	$V_{GS} = 4.5V$		20		nC
Q_{gd}	Gate-Drain Charge			28.5		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off-Delay Time	$V_{DD} = 20V, I_D = 50A,$		90		ns
t_f	Fall Time	$R_G = 4.7\Omega, V_{GS} = 4.5V$ (see test circuit, Figure 5)		80		ns
$t_{d(off)}$	Off-voltage Rise Time	$V_{clamp} = 32V, I_D = 100A$		85		ns
t_f	Fall Time	$R_G = 4.7\Omega, V_{GS} = 4.5V$		125		ns
t_c	Cross-over Time			160		ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				100	A
$I_{SDM(2)}$	Source-drain Current (pulsed)				400	A
$V_{SD(1)}$	Forward On Voltage	$I_{SD} = 100A, V_{GS} = 0$			1.3	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 100A, di/dt = 100A/\mu s,$		88		ns
Q_{rr}	Reverse Recovery Charge	$V_{DD} = 20V, T_j = 150^\circ C$		240		nC
I_{RRM}	Reverse Recovery Current	(see test circuit, Figure 5)		5.5		A

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.
 2. Pulse width limited by safe operating area.

Fig. 1: Unclamped Inductive Load Test Circuit

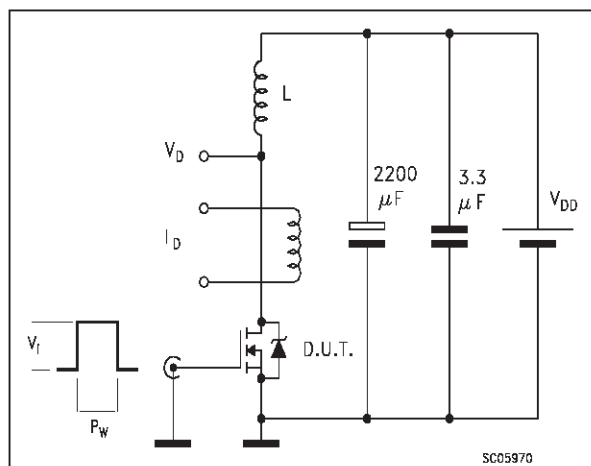


Fig. 2: Unclamped Inductive Waveform

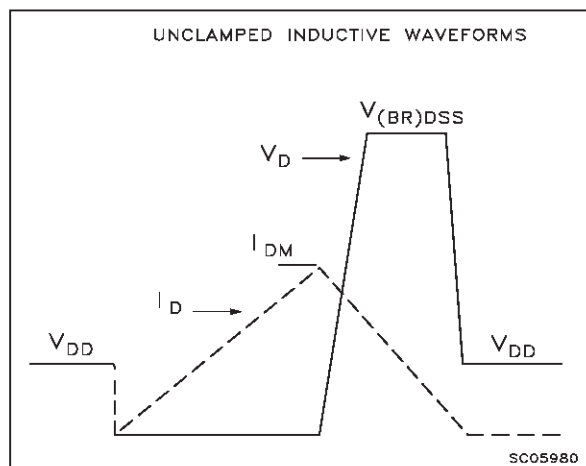


Fig. 3: Switching Times Test Circuit For Resistive Load

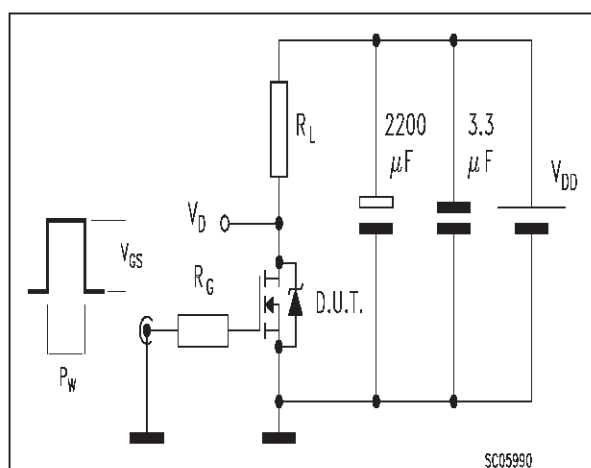


Fig. 4: Gate Charge test Circuit

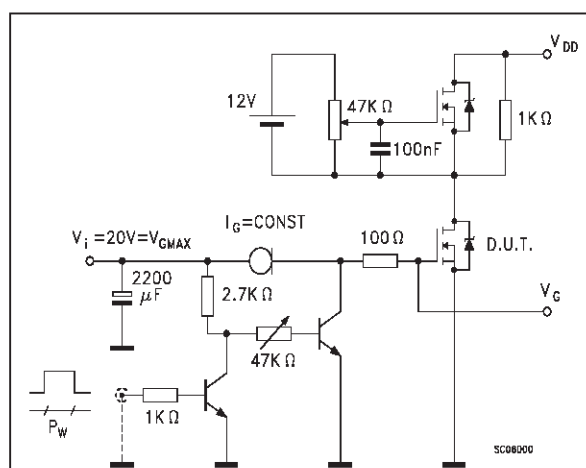
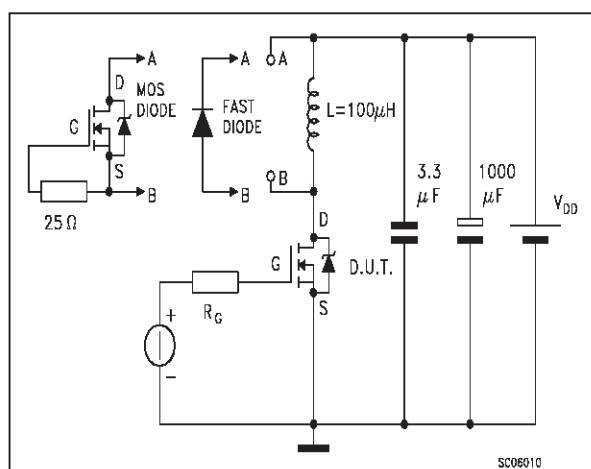
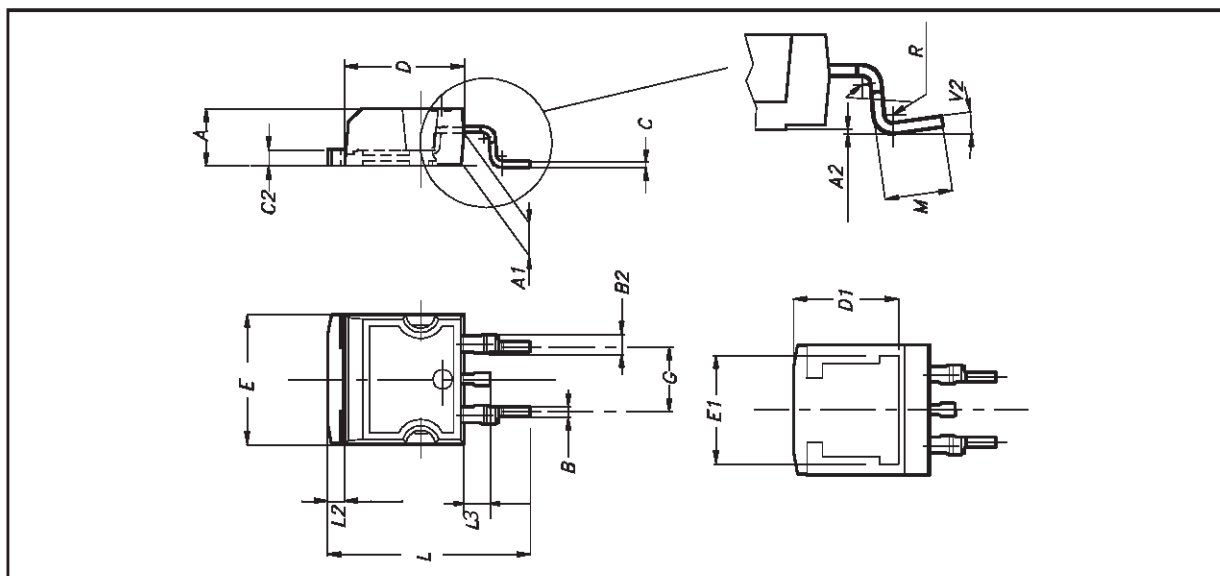


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



D²PAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		8°			



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specification mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a trademark of STMicroelectronics

© 2000 STMicroelectronics – Printed in Italy – All Rights Reserved

STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco -
Singapore - Spain - Sweden - Switzerland - United Kingdom - U.S.A.

<http://www.st.com>