M41T81

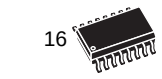
512 Bit (64 bit x 8)
SERIAL ACCESS RTC SRAM with ALARMS

PRELIMINARY DATA

FEATURES SUMMARY

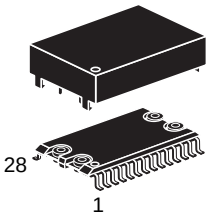
- 2.0 to 5.5V CLOCK OPERATING VOLTAGE
- COUNTERS for TENTHS/HUNDREDTHS of SECONDS, SECONDS, MINUTES, HOURS, DAY, DATE, MONTH, YEAR, and CENTURY
- AUTOMATIC SWITCH-OVER and DESELECT CIRCUITRY
- SERIAL INTERFACE SUPPORTS I^2C BUS (400KHz PROTOCOL)
- 44 BYTES of GENERAL PURPOSE RAM
- PROGRAMMABLE ALARM and INTERRUPT FUNCTION (VALID EVEN DURING BATTERY BACK-UP MODE)
- WATCHDOG TIMER
- LOW OPERATING CURRENT of 400µA
- OPERATING TEMPERATURE of –40 to 85°C
- BATTERY LOW FLAG
- ULTRA-LOW BATTERY SUPPLY CURRENT of 1µA

Figure 1. Packages



SO16 (MQ)

SNAPHAT (SH)
Battery & Crystal



SO28 (MH)

TABLE OF CONTENTS

SUMMARY DESCRIPTION

The M41T81 Serial Access TIMEKEEPER SRAM is a low power 512 bit static CMOS SRAM organized as 64 words by 8 bits. A built-in 32.768 KHz oscillator (external crystal controlled) and 8 bytes of the SRAM (see Table 3, page 12) are used for the clock/calendar function and are configured in binary coded decimal (BCD) format. An additional 12 bytes of RAM provide status/control of Alarm, Watchdog and Square Wave functions. Addresses and data are transferred serially via a two line, bi-directional I^2C interface. The built-in address register is incremented automatically after each write or read data byte.

The M41T81 has a built-in power sense circuit which detects power failures and automatically switches to the battery supply when a power failure occurs. The energy needed to sustain the SRAM and clock operations can be supplied by a small lithium button supply when a power failure occurs. Functions available to the user include a non-volatile, time-of-day clock/calendar, Alarm interrupts, Watchdog Timer and programmable Square Wave output. The eight clock address locations contain the century, year, month, date, day, hour, minute, second and tenths/hundredths of a second in 24 hour BCD format. Corrections for 28, 29 (leap year - valid until year 2100), 30 and 31 day months are made automatically. The ninth clock address location controls user access to the clock information and also stores the clock software calibration setting.

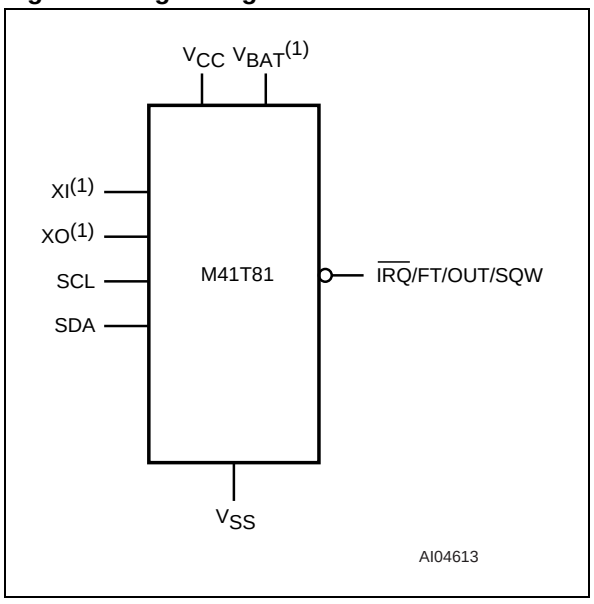
The M41T81 is supplied in either a 28 lead SOIC SNAPHAT package (which integrates both crystal and battery in a single SNAPHAT top) or a 16 pin SOIC. The 28 pin 330mil SOIC provides sockets with gold plated contacts at both ends for direct connection to a separate SNAPHAT housing containing the battery and crystal. The unique design allows the SNAPHAT battery/crystal package to be mounted on top of the SOIC package after the completion of the surface mount process.

Insertion of the SNAPHAT housing after reflow prevents potential battery and crystal damage due to the high temperatures required for device surface-mounting. The SNAPHAT housing is also keyed to prevent reverse insertion.

The SOIC and battery/crystal packages are shipped separately in plastic anti-static tubes or in Tape & Reel form. For the 28 lead SOIC, the battery/crystal package (i.e. SNAPHAT) part number is “M4TXX-BR12SH” (see Table 18, page 26).

Caution: Do not place the SNAPHAT battery/crystal top in conductive foam, as this will drain the lithium button-cell battery.

Figure 2. Logic Diagram



Note: 1. For SO16 package only.

Table 1. Signal Names

$XI^{(1)}$	Oscillator Input
$XO^{(1)}$	Oscillator Output
$\overline{IRQ}$/OUT/ FT/SQW	Interrupt / Output Driver / Frequency Test (Open Drain) Square Wave (CMOS)
SDA	Serial Data Input/Output
SCL	Serial Clock Input
V_{BAT} (1)	Battery Supply Voltage
V_{CC}	Supply Voltage
V_{SS}	Ground

Note: 1. For SO16 package only

Figure 3. 16-pin SOIC Connections

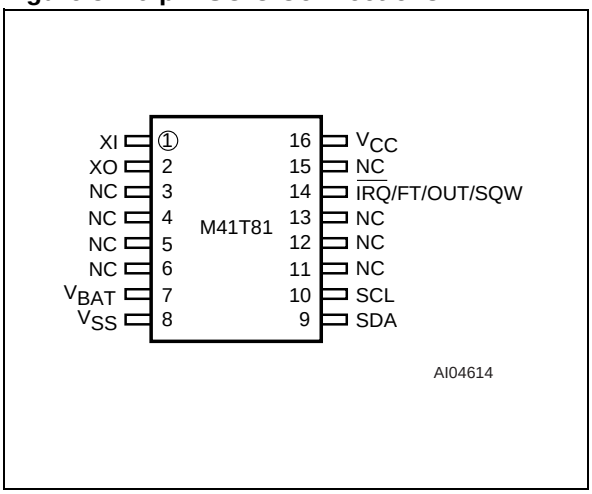


Figure 4. 28-pin SOIC Connections

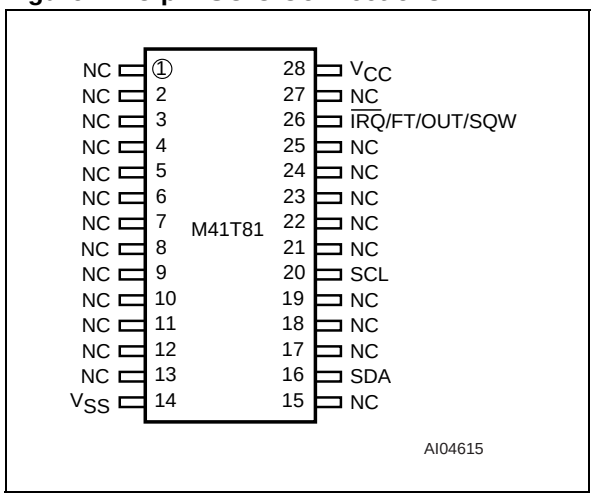
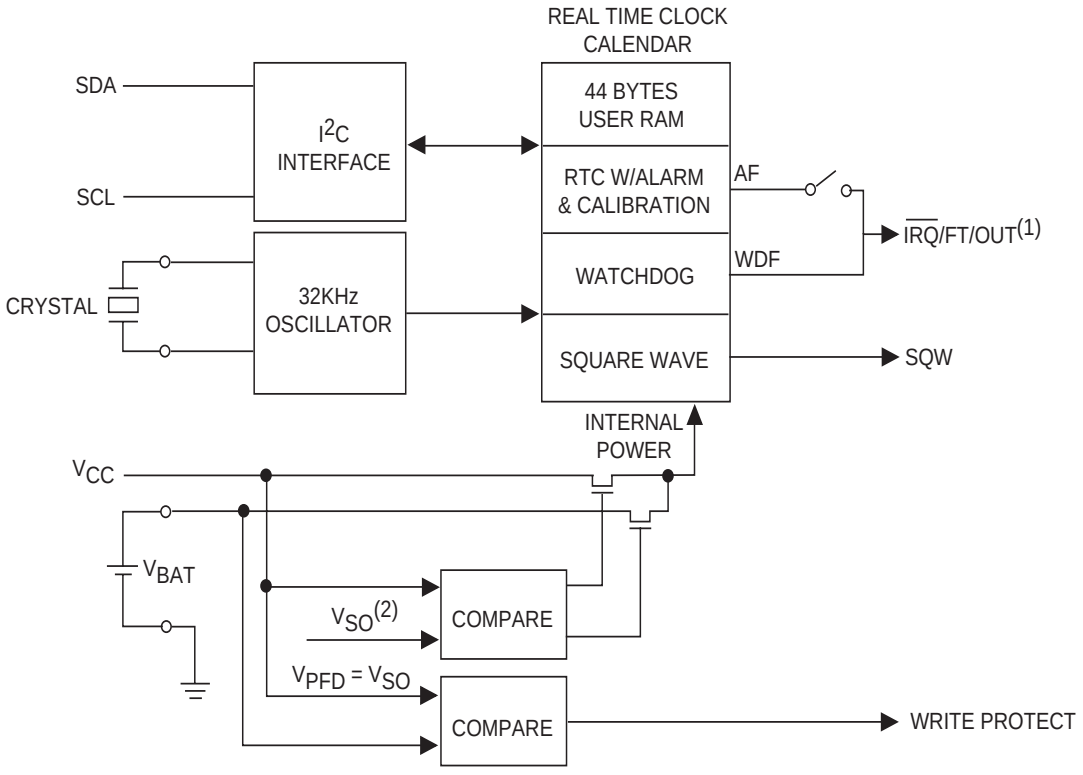


Figure 5. Block Diagram



Note 1. Open drain output
Note 2. $V_{(SO)} = V_{(BAT)} - 0.5V$ (typ)

AI04616

OPERATION

The M41T81 clock operates as a slave device on the serial bus. Access is obtained by implementing a start condition followed by the correct slave address (D0h). The 64 bytes contained in the device can then be accessed sequentially in the following order:

1. Tenths/Hundredths of a Second Register
2. Seconds Register
3. Minutes Register
4. Century/Hours Register
5. Day Register
6. Date Register
7. Month Register
8. Year Register
9. Control Register
10. Watchdog Register

11 - 16. Alarm Registers

17 - 19. Reserved

20. Square Wave Register

21 - 64. User RAM

The M41T81 clock continually monitors Vcc for an out-of tolerance condition. Should Vcc fall below V_{SO}, the device terminates an access in progress and resets the device address counter. Inputs to the device will not be recognized at this time to prevent erroneous data from being written to the device from a an out-of-tolerance system. The device also automatically switches over to the battery and powers down into an ultra low current mode of operation to conserve battery life. As system power returns and Vcc rises above Vso, the battery is disconnected, and the power supply is switched to external Vcc.

For more information on Battery Storage Life refer to Application Note AN1012.

2-Wire Bus Characteristics

The bus is intended for communication between different IC's. It consists of two lines: a bi-directional data signal (SDA) and a clock signal (SCL). Both the SDA and SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

– Data transfer may be initiated only when the bus is not busy.

– During data transfer, the data line must remain stable whenever the clock line is High.

– Changes in the data line, while the clock line is High, will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy. Both data and clock lines remain High.

Start data transfer. A change in the state of the data line, from high to Low, while the clock is High, defines the START condition.

Stop data transfer. A change in the state of the data line, from Low to High, while the clock is High, defines the STOP condition.

Data Valid. The state of the data line represents valid data when after a start condition, the data line is stable for the duration of the high period of the clock signal. The data on the line may be changed during the Low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition. The number of data bytes transferred between the start and stop conditions is not limited. The information is transmitted byte-wide and each receiver acknowledges with a ninth bit.

By definition a device that gives out a message is called "transmitter," the receiving device that gets the message is called "receiver." The device that controls the message is called "master." The devices that are controlled by the master are called "slaves."

Acknowledge. Each byte of eight bits is followed by one acknowledge bit. This acknowledge bit is a low level put on the bus by the receiver whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is a stable Low during the High period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case the transmitter must leave the data line High to enable the master to generate the STOP condition.

Figure 6. Serial Bus Data Transfer Sequence

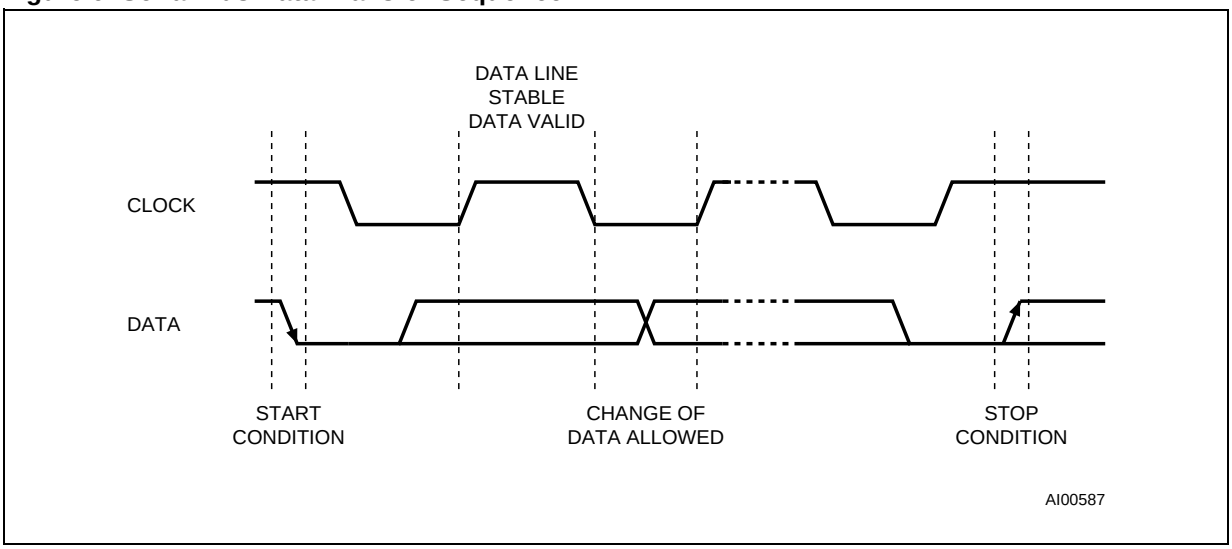


Figure 7. Acknowledgement Sequence

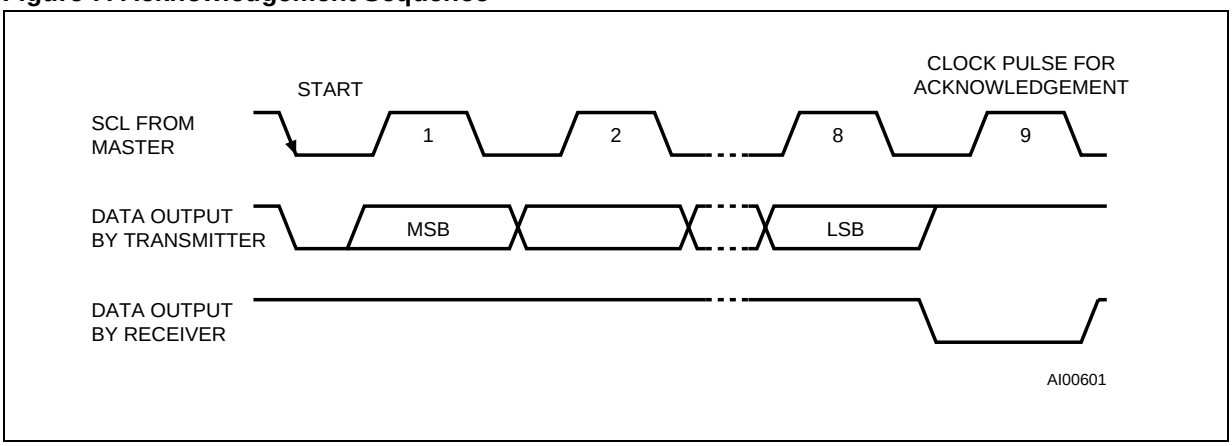


Figure 8. Bus Timing Requirements Sequence

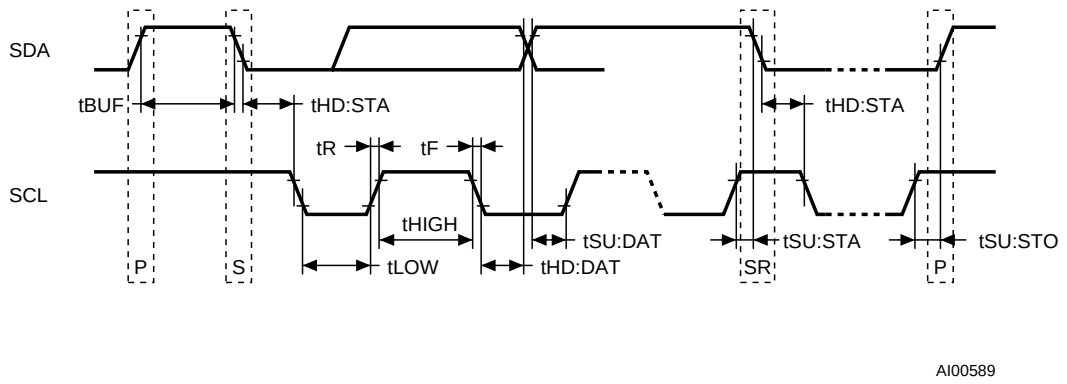


Table 2. AC Characteristics

Sym	Parameter	Min	Typ	Max	Units
f_{SCL}	SCL Clock Frequency	0		400	kHz
t_{LOW}	Clock Low Period	1.3			µs
t_{HIGH}	Clock High Period	600			ns
t_R	SDA and SCL Rise Time			300	ns
t_F	SDA and SCL Fall Time			300	ns
$t_{HD:STA}$	START Condition Hold Time (after this period the first clock pulse is generated)	600			ns
$t_{SU:STA}$	START Condition Setup Time (only relevant for a repeated start condition)	600			ns
$t_{SU:DAT}$ (1)	Data Setup Time	100			ns
$t_{HD:DAT}$	Data Hold Time	0			µs
$t_{SU:STO}$	STOP Condition Setup Time	600			ns
t_{BUF}	Time the bus must be free before a new transmission can start	1.3			µs

Read Mode

In this mode the master reads the M41T81 slave after setting the slave address (see Figure 10, page 10). Following the write mode control bit (R/$\overline{W}$=0) and the acknowledge bit, the word address 'An' is written to the on-chip address pointer. Next the START condition and slave address are repeated followed by the READ mode control bit (R/$\overline{W}$=1). At this point the master transmitter becomes the master receiver. The data byte which was addressed will be transmitted and the master receiver will send an acknowledge bit to the slave transmitter. The address pointer is only incremented on reception of an acknowledge bit. The M41T81 slave transmitter will now place the data byte at address An+1 on the bus, the master receiver reads and acknowledges the new byte and the address pointer is incremented to "An+2."

This cycle of reading consecutive addresses will continue until the master receiver sends a STOP condition to the slave transmitter.

The system-to-user transfer of clock data will be halted whenever the address being read is a clock address (00h to 07h). The update will resume either due to a Stop Condition or when the pointer increments to a RAM address.

An alternate READ mode may also be implemented whereby the master reads the M41T81 slave without first writing to the (volatile) address pointer. The first address that is read is the last one stored in the pointer (see Figure 11, page 10).

Write Mode

In this mode the master transmitter transmits to the M41T81 slave receiver. Bus protocol is shown in Figure 12, page 10. Following the START condition and slave address, a logic '0' (R/$\overline{W}$=0) is placed on the bus and indicates to the addressed device that word address "An" will follow and is to be written to the on-chip address pointer. The data word to be written to the memory is strobed in next and the internal address pointer is incremented to the next memory location within the RAM on the reception of an acknowledge clock. The M41T81 slave receiver will send an acknowledge clock to the master transmitter after it has received the slave address (see Figure 7, page 7) and again after it has received the word address and each data byte.

Figure 9. Slave Address Location

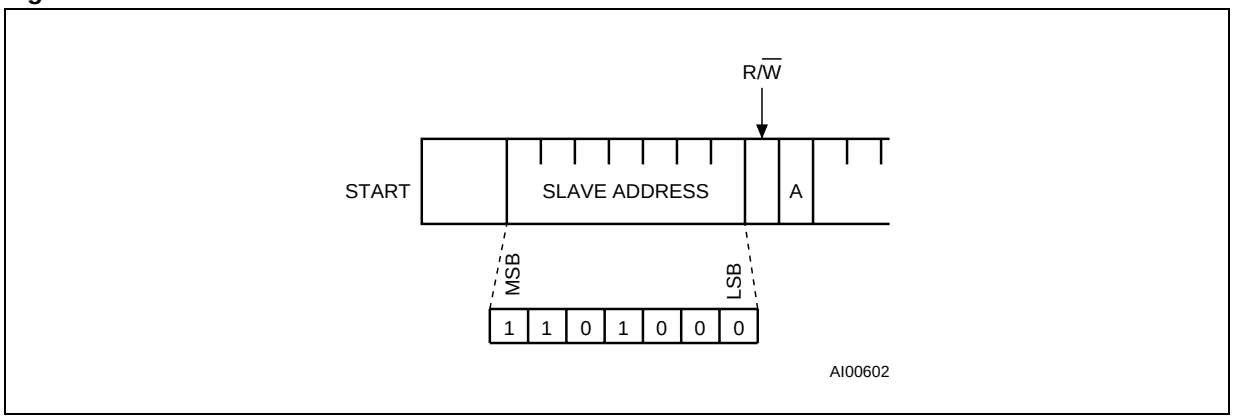


Figure 10. Read Mode Sequences

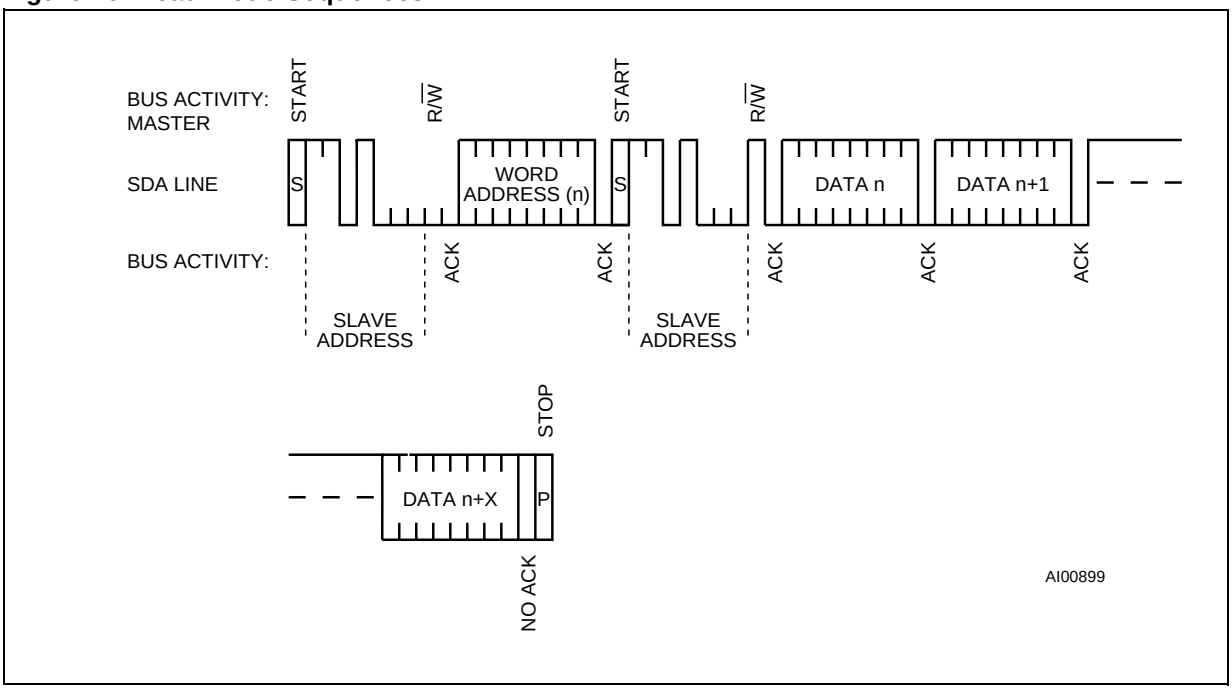


Figure 11. Alternative Read Mode Sequences

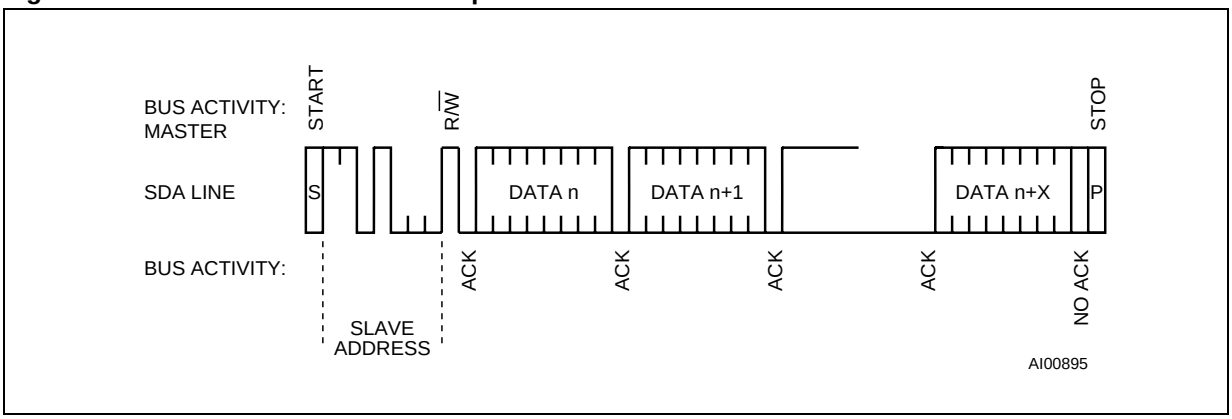
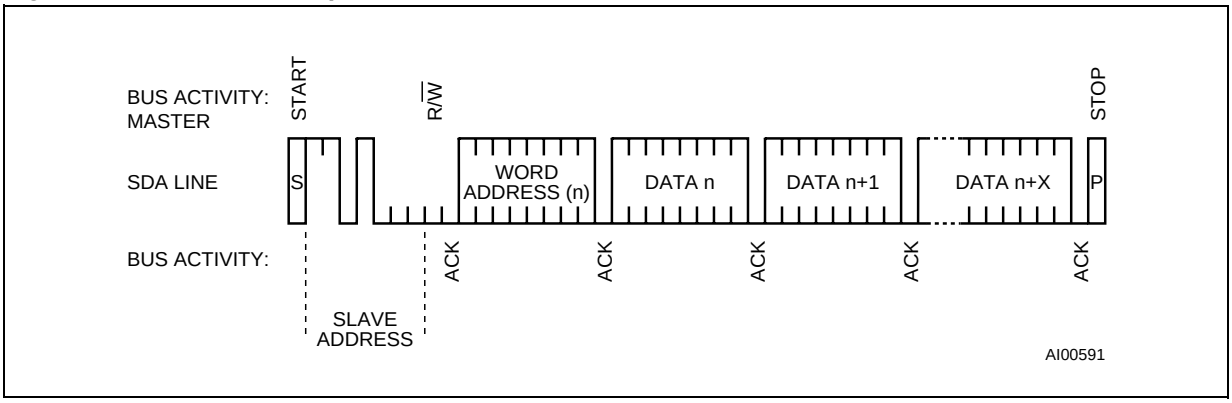


Figure 12. Write Mode Sequence



CLOCK OPERATION

The twenty byte clock register (see Table 3, page 12) is used to both set the clock and to read the date and time from the clock, in a binary coded decimal format. Tenths/Hundredths of Seconds, Seconds, Minutes, and Hours are contained within the first four registers. Bits D6 and D7 of clock register 3 (Century/Hours Register) contain the CENTURY ENABLE Bit (CEB) and the CENTURY Bit (CB). Setting CEB to a '1' will cause CB to toggle, either from '0' to '1' or from '1' to '0' at the turn of the century (depending upon its initial state). If CEB is set to a '0', CB will not toggle. Bits D0 through D2 of register 4 contain the Day (day of week). Registers 5, 6 and 7 contain the Date (day of month), Month and Years. The ninth clock register is the Control Register (this is described in the Clock Calibration section). Bit D7 of register 1 contains the STOP Bit (ST). Setting this bit to a '1' will cause the oscillator to stop. If the device is expected to spend a significant amount of time on the shelf, the oscillator may be stopped to reduce current drain. When reset to a '0' the oscillator restarts within one second.

The eight Clock Registers may be read one byte at a time, or in a sequential block. The Control Register (Address location 08h) may be accessed independently. Provision has been made to assure that a clock update does not occur while any of the seven clock addresses are being read. If a clock address is being read, an update of the clock registers will be halted. This will prevent a transition of data during the read.

Note: Upon power-up following a power failure, the HT bit will automatically be set to a '1'. This will prevent the clock from updating the TIMEKEEPER registers, and will allow the user to read the exact time of the power-down event. Resetting the HT bit to a '0' will allow the clock to update the TIMEKEEPER registers with the current time.

Data Retention Mode

With valid V_{CC} applied, the M41T81 can be accessed as described above with read or write cycles. Should the supply voltage decay, the M41T81 will automatically deselect, write protecting itself when Vcc falls between V_{PFD} (max) and V_{PFD} (min). This is accomplished by internally inhibiting access to the clock registers and SRAM. When Vcc falls below the Battery Back-up Switchover Voltage (V_{SO}), power input is switched from the V_{CC} pin to the battery and the clock registers and SRAM are maintained from the attached battery supply.

All outputs become high impedance. On power up, when Vcc returns to a nominal value, write protection continues for t_{REC}.

For a further more detailed review of lifetime calculations, please see Application Note AN1012.

TIMEKEEPER® Registers

The M41T81 offers 20 internal registers which contain Clock, Alarm, Watchdog, Flag, Square Wave and Control data. These registers are memory locations which contain external (user accessible) and internal copies of the data (usually referred to as BiPORT™ TIMEKEEPER cells). The external copies are independent of internal functions except that they are updated periodically by the simultaneous transfer of the incremented internal copy. TIMEKEEPER and Alarm Registers store data in BCD. Control, Watchdog and Square Wave Registers store data in Binary Format.

Table 3. TIMEKEEPER® Register Map

Addr									Function/Range BCD Format	
	D7	D6	D5	D4	D3	D2	D1	D0		
00h	0.1 Seconds				0.01 Seconds				Seconds	00-99
01h	ST	10 Seconds			Seconds				Seconds	00-59
02h	0	10 Minutes			Minutes				Minutes	00-59
03h	CEB	CB	10 Hours		Hours (24 Hour Format)				Century/ Hour	0-1/00-23
04h	0	0	0	0	0	Day of Week			Day	01-7
05h	0	0	10 Date		Date: Day of Month				Date	01-31
06h	0	0	0	10M	Month				Month	01-12
07h	10 Years				Year				Year	00-99
08h	OUT	FT	S	Calibration					Control	
09h	0	BMB4	BMB3	BMB2	BMB1	BMB0	RB1	RB0	Watchdog	
0Ah	AFE	SQWE	ABE	Al 10M	Alarm Month				Al Month	01-12
0Bh	RPT4	RPT5	Al 10 Date		Alarm Date				Al Date	01-31
0Ch	RPT3	HT	Al 10 Hour		Alarm Hour				Al Hour	00-23
0Dh	RPT2	Alarm 10 Minutes			Alarm Minutes				Al Min	00-59
0Eh	RPT1	Alarm 10 Seconds			Alarm Seconds				Al Sec	00-59
0Fh	WDF	AF	0	0	0	0	0	0	Flags	
10h	0	0	0	0	0	0	0	0	Reserved	
11h	0	0	0	0	0	0	0	0	Reserved	
12h	0	0	0	0	0	0	0	0	Reserved	
13h	RS3	RS2	RS1	RS0	0	0	0	0	SQW	

Keys:

S = Sign Bit
FT = Frequency Test Bit
ST = Stop Bit
0 = Must be set to zero
BMB0-BMB4 = Watchdog Multiplier Bits
CEB = Century Enable Bit
CB = Century Bit
OUT = Output level
AFE = Alarm Flag Enable Flag
RB0-RB1 = Watchdog Resolution Bits
ABE = Alarm in Battery Back-Up Mode Enable Bit
RPT1-RPT5 = Alarm Repeat Mode Bits
WDF = Watchdog flag
AF = Alarm flag
SQWE = Square Wave Enable
RS0-RS3 = SQW Frequency
HT = Halt Update Bit

Setting Alarm Clock Registers

Address locations 0Ah-0Eh contain the alarm settings. The alarm can be configured to go off at a prescribed time on a specific month, date, hour, minute, or second or repeat every year, month, day, hour, minute, or second. It can also be programmed to go off while the M41T81 is in the battery back-up to serve as a system wake-up call.

Bits RPT5-RPT1 put the alarm in the repeat mode of operation. Table 4, page 14 shows the possible configurations. Codes not listed in the table default to the once per second mode to quickly alert the user of an incorrect alarm setting.

When the clock information matches the alarm clock settings based on the match criteria defined by RPT5-RPT1, the AF (Alarm Flag) is set. If AFE (Alarm Flag Enable) is also set, the alarm condition activates the $\overline{IRQ}$/FT/OUT/SQW pin. The $\overline{IRQ}$/FT/OUT/SQW output is cleared by a read to the Flags register. This read of the Flags register will also reset the Alarm Flag (D6; Register 0Fh).

The $\overline{IRQ}$/FT/OUT/SQW pin can also be activated in the battery back-up mode. The $\overline{IRQ}$/FT/OUT/SQW will go low if an alarm occurs and both ABE (Alarm in Battery Back-up Mode Enable) and AFE are set. The ABE and AFE bits are reset during power-up, therefore an alarm generated during power-up will only set AF. The user can read the Flag Register at system boot-up to determine if an alarm was generated while the M41T81 was in the deselect mode during power-up. Figure 13, page 13 illustrates the back-up mode alarm timing.

Figure 13. Back-up Mode Alarm Waveform

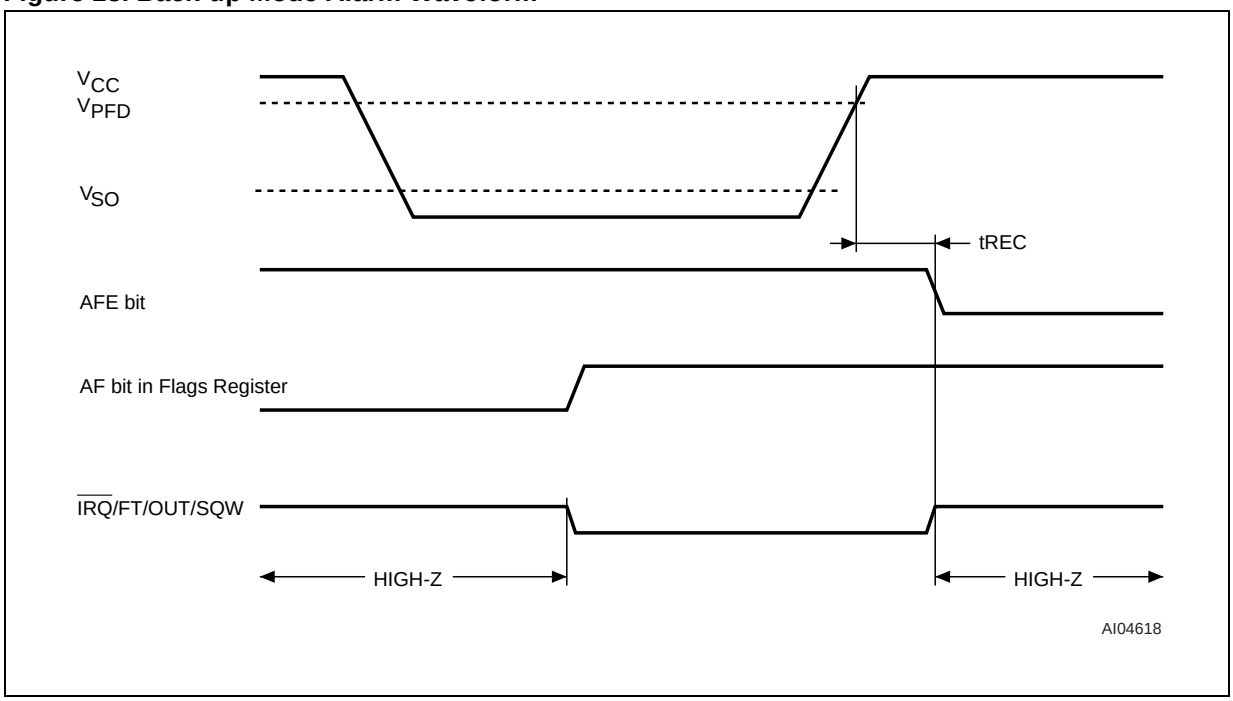


Figure 14. Alarm Interrupt Reset Waveforms

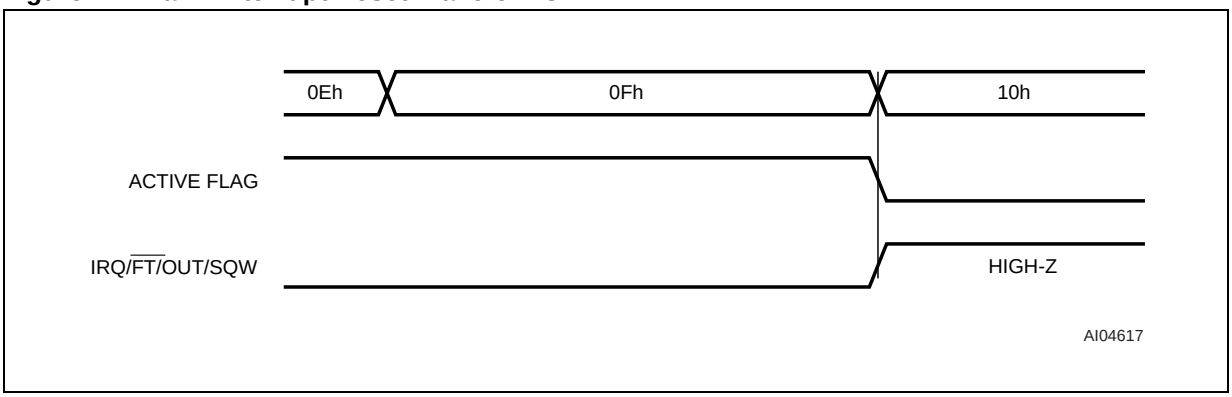


Table 4. Alarm Repeat Modes

RPT5	RPT4	RPT3	RPT2	RPT1	Alarm Setting
1	1	1	1	1	Once per Second
1	1	1	1	0	Once per Minute
1	1	1	0	0	Once per Hour
1	1	0	0	0	Once per Day
1	0	0	0	0	Once per Month
0	0	0	0	0	Once per Year

Watchdog Timer

The watchdog timer can be used to detect an out-of-control microprocessor. The user programs the watchdog timer by setting the desired amount of time-out into the Watchdog Register, address 09h. Bits BMB4-BMB0 store a binary multiplier and the two lower order bits RB1-RB0 select the resolution, where 00=1/16 second, 01=1/4 second, 10=1 second, and 11=4 seconds. The amount of time-out is then determined to be the multiplication of the five bit multiplier value with the resolution. (For example: writing 00001110 in the Watchdog Register = 3*1 or 3 seconds). If the processor does not reset the timer within the specified period, the M41T81 sets the WDF (Watchdog Flag) and generates a watchdog interrupt.

Note: If the Square Wave function is enabled, the accuracy of the Watchdog Timer will be a function of the selected resolution.

The watchdog timer can be reset by having the microprocessor perform a write of the Watchdog Register. The time-out period then starts over.

Should the watchdog timer time-out, a value of 00h needs to be written to the Watchdog Register in order to clear the IRQ/FT/OUT/SQW pin. This will also disable the watchdog function until it is again programmed correctly. A read of the Flags Register will reset the Watchdog Flag (Bit D7; Register 0Fh).

The watchdog function is automatically disabled upon power-up and the Watchdog Register is cleared. If the watchdog function is set and the frequency test function is activated, the watchdog function prevails and the frequency test function is denied. The OUT function has the lowest priority and will only be enabled when the Watchdog Register (09h), AFE Bit, SQWE Bit, and FT Bit are ‘0’.

Square Wave Output

The M41T81 offers the user a programmable square wave function which is output on the SQW pin. RS3-RS0 bits located in 13h establish the square wave output frequency. These frequencies are listed in Table 5. Once the selection of the SQW frequency has been completed, the $\overline{IRQ}$/FT/OUT/SQW pin can be turned on and off under software control with the Square Wave Enable Bit (SQWE) located in Register 0Ah.

Table 5. Square Wave Output Frequency

Square Wave Bits				Square Wave	
RS3	RS2	RS1	RS0	Frequency	Units
0	0	0	0	None	-
0	0	0	1	32.768	kHz
0	0	1	0	8.192	kHz
0	0	1	1	4.096	kHz
0	1	0	0	2.048	kHz
0	1	0	1	1.024	kHz
0	1	1	0	512	Hz
0	1	1	1	256	Hz
1	0	0	0	128	Hz
1	0	0	1	64	Hz
1	0	1	0	32	Hz
1	0	1	1	16	Hz
1	1	0	0	8	Hz
1	1	0	1	4	Hz
1	1	1	0	2	Hz
1	1	1	1	1	Hz

Calibrating the Clock

The M41T81 is driven by a quartz controlled oscillator with a nominal frequency of 32,768 Hz. The devices are tested not exceed +/-35 PPM (parts per million) oscillator frequency error at 25^{o}C, which equates to about +/-1.53 minutes per month (see Figure 15, page 17). When the Calibration circuit is properly employed, accuracy improves to better than +1/-2 PPM at 25°C.

The oscillation rate of crystals changes with temperature. The M41T81 design employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 256 stage, as shown in Figure 16, page 17. The number of times pulses which are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five Calibration bits found in the Control Register. Adding counts speeds the clock up, subtracting counts slows the clock down.

The Calibration bits occupy the five lower order bits (D4-D0) in the Control Register 8h. These bits can be set to represent any value between 0 and 31 in binary form. Bit D5 is a Sign bit; '1' indicates positive calibration, '0' indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles. If a binary '1' is loaded into the register, only the first 2 minutes in the 64 minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is +4.068 or -2.034 PPM of adjustment per calibration step in the calibration register. Assuming that the oscillator is running at exactly 32,768 Hz, each of the 31 increments in the Calibration byte would represent +10.7 or -5.35 seconds per month which corresponds to a total range of +5.5 or -2.75 minutes per month.

Two methods are available for ascertaining how much calibration a given M41T81 may require.

The first involves setting the clock, letting it run for a month and comparing it to a known accurate reference and recording deviation over a fixed period of time. Calibration values, including the number of seconds lost or gained in a given period, can be found in Application Note AN934: TIMEKEEPER CALIBRATION. This allows the designer to give the end user the ability to calibrate the clock as the environment requires, even if the final product is packaged in a non-user serviceable enclosure. The designer could provide a simple utility that accesses the Calibration byte.

The second approach is better suited to a manufacturing environment, and involves the use of the $\overline{IRQ}$/FT/OUT/SQW pin. The pin will toggle at 512Hz, when the Stop bit (ST, D7 of 1h) is '0',the Frequency Test bit (FT, D6 of 8h) is '1', the Alarm Flag Enable bit (AFE, D7 of Ah) is '0', and the Square Wave Enable Bit (SQWE, D6 of 0Ah) is 0 and the Watchdog Register (9h=0) is reset.

Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.010124 Hz would indicate a +20 PPM oscillator frequency error, requiring a -10 (XX001010) to be loaded into the Calibration Byte for correction. Note that setting or changing the Calibration Byte does not affect the Frequency Test output frequency.

The $\overline{IRQ}$/FT/OUT/SQW pin is an open drain output which requires a pull-up resistor to Vcc for proper operation. A 500-10k resistor is recommended in order to control the rise time. The FT bit is cleared on power-down.

Output Driver Pin

When the FT bit, AFE bit, SQWE bit, and watchdog register are not set, the $\overline{IRQ}$/FT/OUT/SQW pin becomes an output driver that reflects the contents of D7 of the Control Register. In other words, when D6 and D7 of locations 08h and 0Ah and the watchdog register are a '0,' then the $\overline{IRQ}$/FT/OUT/SQW pin will be driven low.

Note: The $\overline{IRQ}$/FT/OUT/SQW pin is an open drain which requires an external pull-up resistor (unless the SQW function is enabled).

Initial Power-on Defaults

Upon initial application of power to the device, the following register bits are set to a '0' state: Watchdog Register; AFE; ABE and SQWE. The following bits are set to a '1' state: ST; OUT; and HT.

Century Bit

Bits D7 and D6 of Clock Register 03h contain the CENTURY ENABLE Bit (CEB) and the CENTURY Bit (CB). Setting CEB to a "1" will cause CB to toggle, either from a "0" to "1" or from "1" to "0" at the turn of the century (depending upon its initial state). If CEB is set to a "0", CB will not toggle.

Figure 15. Crystal Accuracy Across Temperature

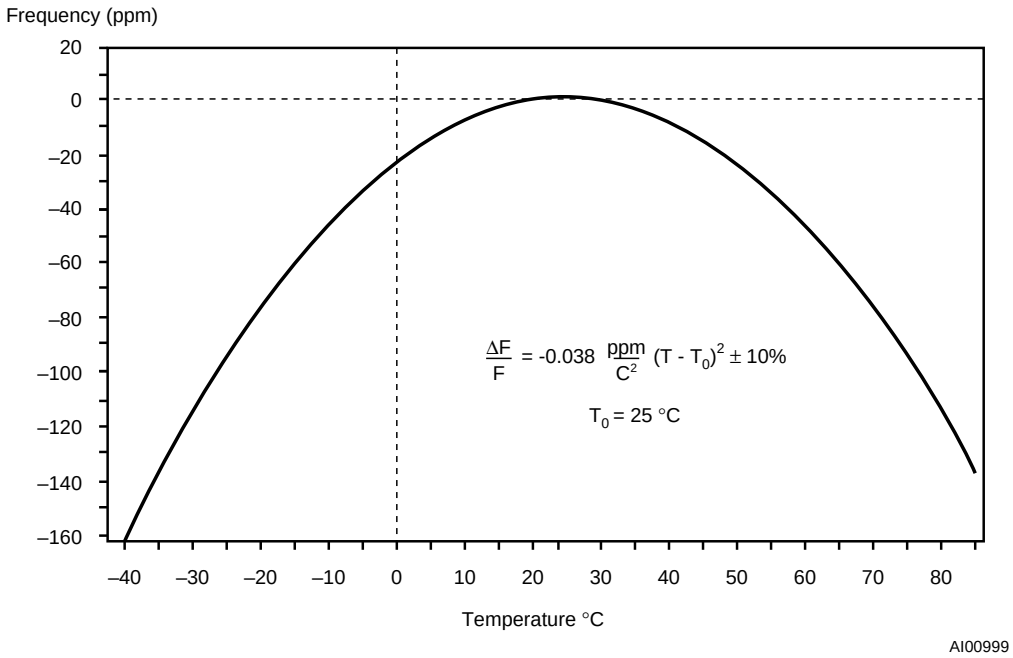
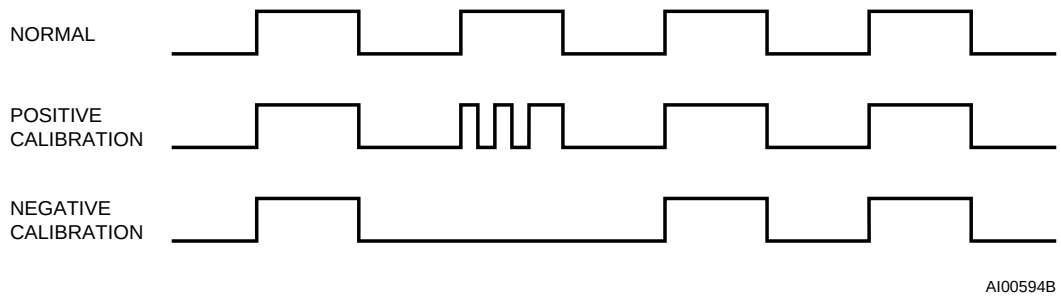


Figure 16. Clock Calibration



MAXIMUM RATING

Stressing the device above the rating listed in the Absolute Maximum Ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 6. Absolute Maximum Ratings

Sym	Parameter		Value	Unit
T_{STG}	Storage Temperature (V_{CC} Off, Oscillator Off)	SNAPHAT	-40 to 85	°C
		SOIC	-55 to 125	°C
T_{SLD}(2)	Lead Solder Temperature for 10 Seconds		260	°C
V_{IO}	Input or Output Voltages		-0.3 to Vcc+0.3	V
I_O	Output Current		20	mA
P_D	Power Dissipation		1	W

Note: Soldering temperature not to exceed 260°C for 10 seconds (total thermal budget not to exceed 150°C for longer than 30 seconds).

***CAUTION**: Negative undershoots below -0.3 volts are not allowed on any pin while in the Battery Back-Up Mode*

***CAUTION**: Do NOT wave solder SOIC to avoid damaging SNAPHAT socket.*

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the Measurement Conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 7. Operating and AC Measurement Conditions

Parameter		Unit
Supply Voltage (V_{CC})	-0.3 to 7.0	V
Ambient Operating Temperature (T_A)	-40 to 85	°C
Load Capacitance (C_L)	100	pF
Input Rise and Fall Times	≤ 50	ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8\ V_{CC}$	V
Input and Output Timing Ref. Voltages	$0.3V_{CC}$ to $0.7\ V_{CC}$	V

Note: Output Hi-Z is defined as the point where data is no longer driven.

Figure 17. AC Measurement I/O Waveform

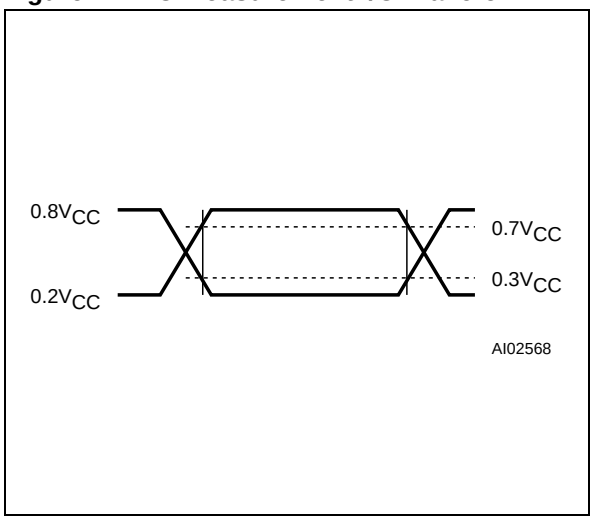


Figure 18. AC Measurement Load Circuit

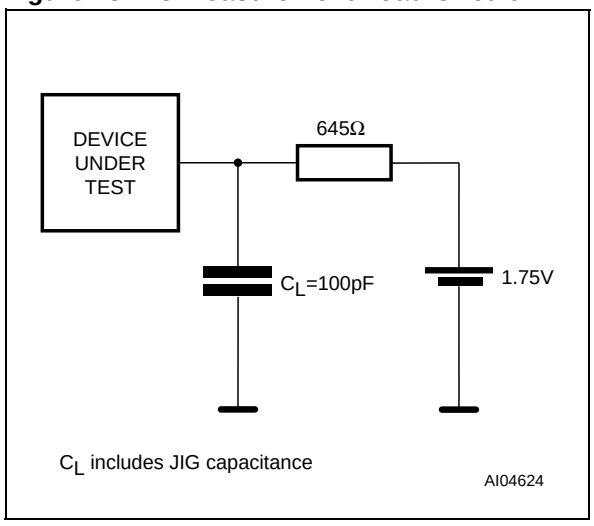


Table 8. Capacitance

Symbol	Parameter	Min	Max	Unit
C_{IN}	Input Capacitance		7	pF
C_{OUT}(1)	Output Capacitance		10	pF
t_{LP}	Low-pass filter input time constant (SDA and SCL)		50	ns

Note: Effective capacitance measured with power supply at 5V . Sampled only, not 100% tested.

1. Outputs deselected.

Table 9. DC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$			±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$			±1	µA
I_{CC1}	Supply Current	Switch Freq = 100kHz			300	µA
I_{CC2}	Supply Current (standby)	SCL,SDA = V_{CC}-0.3V			70	µA
V_{IL}	Input Low Voltage		-0.3		$0.3V_{CC}$	V
V_{IH}	Input High Voltage		$0.7V_{CC}$		V_{CC} + 0.8	V
V_{OL}	Output Low Voltage	I_{OL} = 3.0mA			0.4	V
	Output Low Voltage (Open Drain)	I_{OL} = 10mA			0.4	V
V_{OH}(1)	Output High Voltage	I_{OH} = –1.0mA	2.4			V
V_{BAT}(2)	Battery Supply Voltage		2	3	3.5(3)	V
I_{BAT}	Battery Supply Current	T_A = 25°C, V_{CC} = 0V Oscillator ON, V_{BAT} = 3V		0.8	1	µA

Note: 1. For SQW output (only).
2. STMicroelectronics recommends the RAYOVAC BR1225 or BR1632 (or equivalent) as the battery supply.
3. For rechargeable back-up, V_{BAT} (max) may be considered V_{CC} – 0.5V.

Table 10. Crystal Electrical Characteristics

Sym	Parameter	Min	Typ	Max	Units
f_O	Resonant Frequency		32.768		kHz
R_S	Series Resistance			60	kΩ
C_L	Load Capacitance		12.5		pF

Note: Externally supplied if using the SO16 package.

Load capacitors are integrated within the M41T81. Circuit board layout considerations for the 32.768 kHz crystal of minimum trace lengths and isolation from RF generating signals should be taken into account.

STMicroelectronics recommends the KDS DT-38 Tuning Fork Type (thru-hole) or DMX-26 (SMD) quartz crystal for industrial temperature conditions.

KDS can be contacted at kouhou@kdsj.co.jp or http://www.kdsj.co.jp for further information on this crystal type.

All SNAPHAT battery/crystal tops meet these specifications.

Figure 19. Power Down/Up Mode AC Waveforms

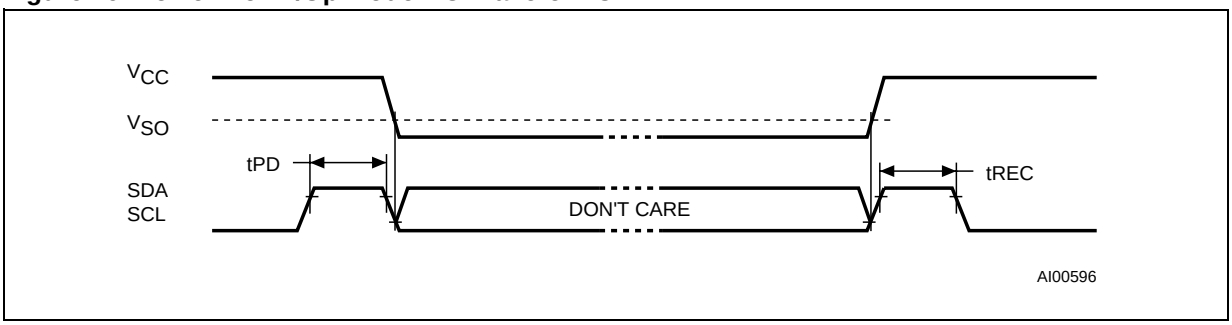


Table 11. Power Down/Up AC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{PD}	SCL and SDA at V_{IH} before Power Down	0			nS
t_{REC}	SCL and SDA at V_{IH} after Power Up	10			µS

Note: V_{CC} fall time should not exceed 5mV/µs.

Table 12. Power Down/Up Trip Points DC Characteristics

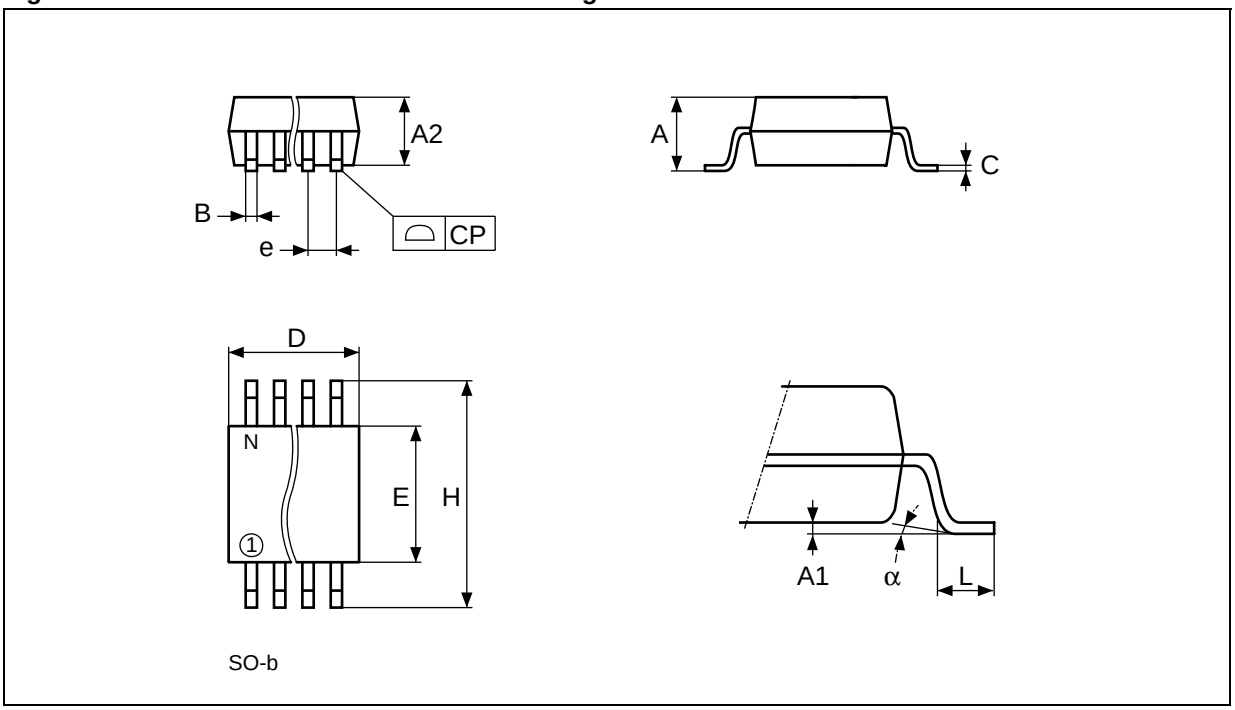
Sym	Parameter	Min	Typ	Max	Unit
V_{SO}(1)	Battery Back-up Switchover Voltage	V_{BAT} – 0.70	V_{BAT} – 0.50	V_{BAT} – 0.20	V

Note: All voltages referenced to V_{SS}.

1. Switch-over and deselect point

PACKAGE MECHANICAL

Figure 20. SO16 – 16-lead Plastic Small Package Outline

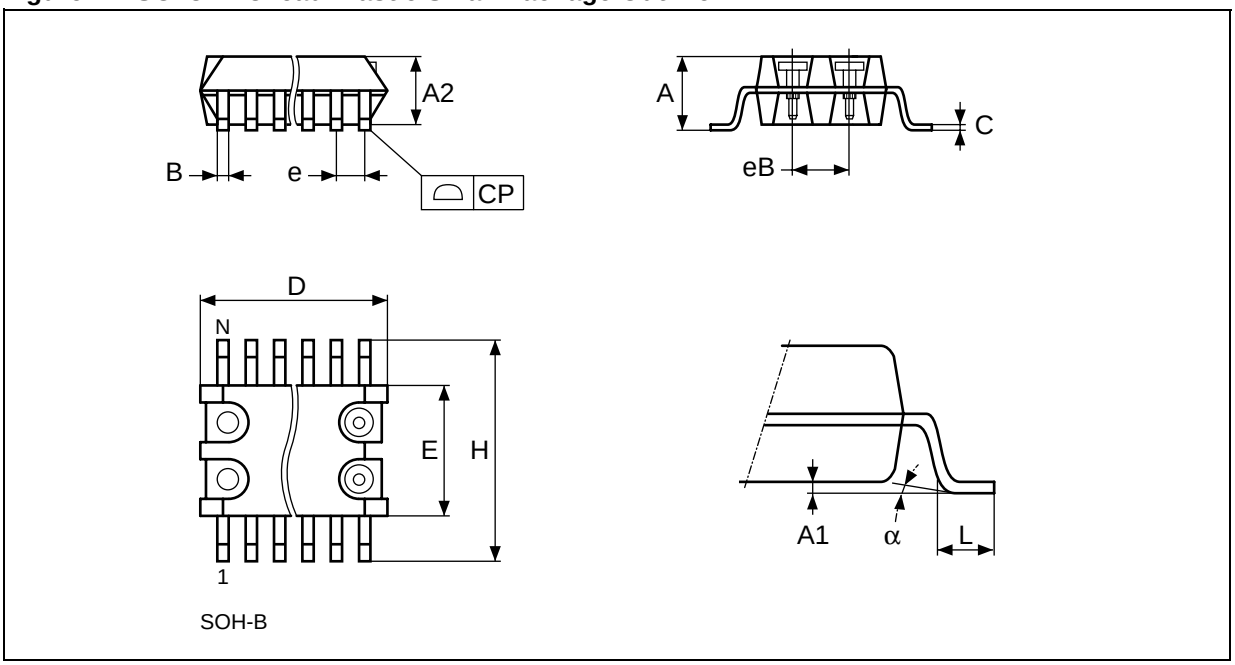


Note: Drawing is not to scale.

Table 13. SO16 – 16-lead Plastic Small Outline (150 mils body width), Package Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.75			0.069
A1		0.10	0.25		0.004	0.010
A2			1.60			0.063
B		0.35	0.46		0.014	0.018
C		0.19	0.25		0.007	0.010
D		9.80	10.00		0.386	0.394
E		3.30	4.00		0.150	0.158
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
L		0.40	1.27		0.016	0.050
a		0°	8°		0°	8°
N	16			16		
CP			0.10			0.004

Figure 21. SO28 – 28-lead Plastic Small Package Outline

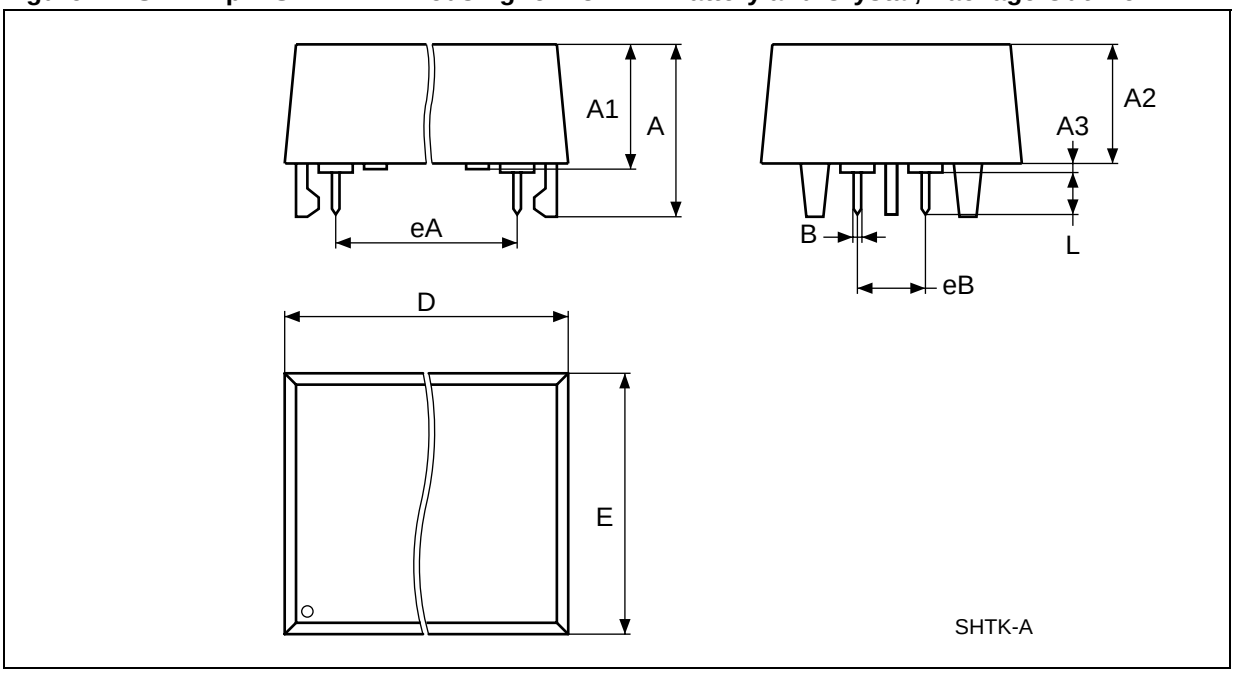


Note: Drawing is not to scale.

Table 14. SO28 – 28-lead Plastic Small Outline, Package Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			3.05			0.120
A1		0.05	0.36		0.002	0.014
A2		2.34	2.69		0.092	0.106
B		0.36	0.51		0.014	0.020
C		0.15	0.32		0.006	0.012
D		17.71	18.49		0.697	0.728
E		8.23	8.89		0.324	0.350
e	1.27	–	–	0.050	–	–
eB		3.20	3.61		0.126	0.142
H		11.51	12.70		0.453	0.500
L		0.41	1.27		0.016	0.050
a		0°	8°		0°	8°
N	28			28		
CP			0.10			0.004

Figure 22. SH – 4-pin SNAPHAT Housing for 48 mAh Battery and Crystal, Package Outline

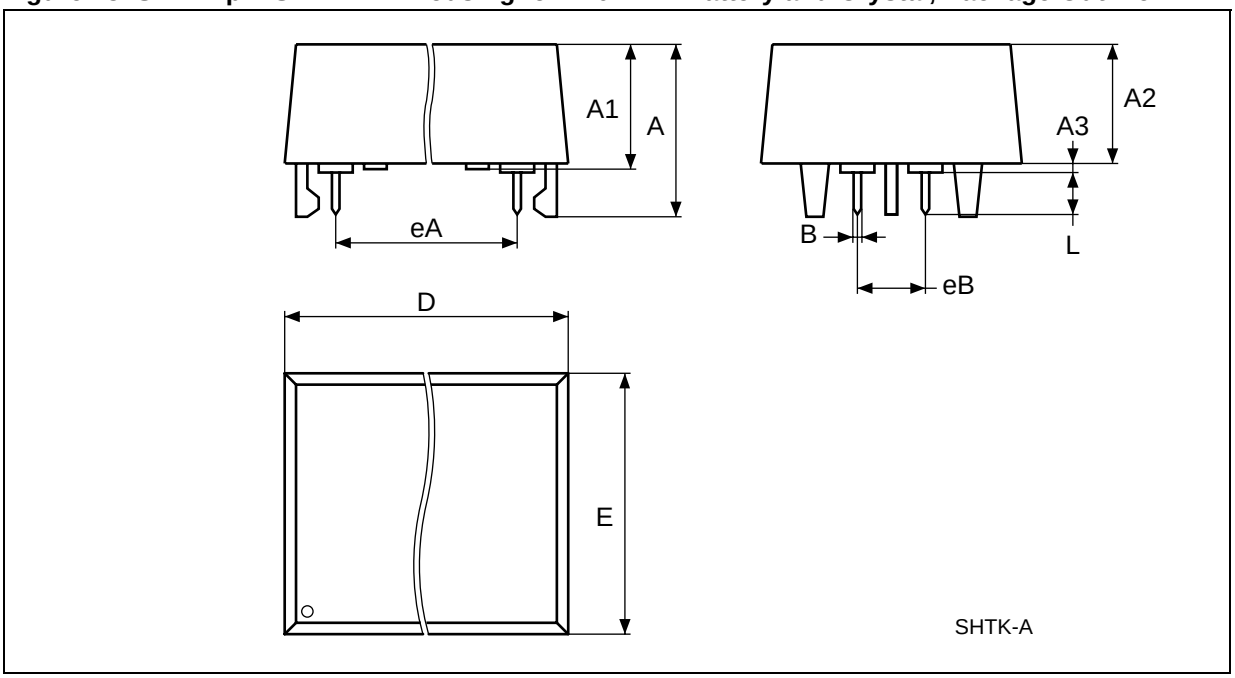


Note: Drawing is not to scale.

Table 15. SH – 4-pin SNAPHAT Housing for 48 mAh Battery and Crystal, Package Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			9.78		0	0.385
A1		6.73	7.24		0.265	0.285
A2		6.48	6.99		0.255	0.275
A3			0.38		0	0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		14.22	14.99		0.560	0.590
eA						
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

Figure 23. SH – 4-pin SNAPHAT Housing for 120 mAh Battery and Crystal, Package Outline



Note: Drawing is not to scale.

Table 16. SH – 4-pin SNAPHAT Housing for 120 mAh Battery and Crystal, Package Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			10.54		0	0.415
A1		8.00	8.51		0.315	0.335
A2		7.24	8.00		0.285	0.315
A3			0.38		0	0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		17.27	18.03		0.680	0.710
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

PART NUMBERING

Table 17. Ordering Information Scheme

Example: M41T 81 MH 6 TR

Device Type

M41T

Supply Voltage and Write Protect Voltage

81 = V_{CC} = 2.0 to 5.0V; V_{PFD} = 2.7 to 2.8V

Package

MQ = SO16

MH(1) = SO28

Temperature Range

6 = –40°C to 85°C

Shipping Method for SOIC

blank = Tubes

TR = Tape & Reel

Note: 1. The 28-pin SOIC package (SOH28) requires the battery/crystal package (SNAPHAT) which is ordered separately under the part number “M4TXX-BR12SHX” in plastic tube or “M4TXX-BR12SHXTR” in Tape & Reel form.

Caution: *Do not place the SNAPHAT battery package "M4TXX-BR12SH" in conductive foam since will drain the lithium button-cell battery.*

For a list of available options (e.g., Speed, Package) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

Table 18. SNAPHAT Battery/Crystal Table

Part Number	Description	Package
M4T28-BR12SH	Lithium Battery (48mAh)/Crystal SNAPHAT	SH
M4T32-BR12SH	Lithium Battery (120mAh)/Crystal SNAPHAT	SH

REVISION HISTORY

Table 19. Document Revision History

Date	Revision Details
October 2000	First Issue
10/9/00	Markups received October 6 entered
12/27/00	Reformatted