



STN3PF06

P-CHANNEL 60V - 0.18Ω - 3A SOT-223

STripFET™ II POWER MOSFET

PRELIMINARY DATA

TYPE	V _{DSS}	R _{DS(on)}	I _D
STN3PF06	60V	<0.20Ω	2.5A

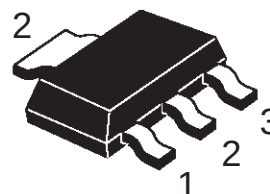
- TYPICAL R_{DS(on)} = 0.18Ω
- EXCEPTIONAL dv/dt CAPABILITY
- AVALANCHE RUGGED TECHNOLOGY
- 100% AVALANCHE TESTED
- LOW THRESHOLD DRIVE

DESCRIPTION

This Power Mosfet is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

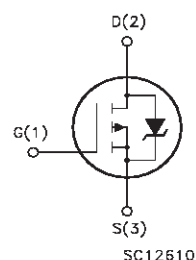
APPLICATIONS

- DC-DC & DC-AC CONVERTERS
- DC MOTOR CONTROL (DISK DRIVES, etc.)



SOT-223

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	60	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	60	V
V _{GS}	Gate- source Voltage	±20	V
I _D	Drain Current (continuous) at T _C = 25°C	2.5	A
I _D	Drain Current (continuous) at T _C = 100°C	1.5	A
I _{DM} (●)	Drain Current (pulsed)	10	A
P _{TOT}	Total Dissipation at T _C = 25°C	2.5	W
	Derating Factor	0.02	W/°C
dv/dt(1)	Peak Diode Recovery voltage slope	6	V/ns
T _{stg}	Storage Temperature	-65 to 175	°C
T _j	Max. Operating Junction Temperature	150	°C

(●) Pulse width limited by safe operating area

Note: For the P-CHANNEL MOSFET actual polarity of Voltages and current has to be reversed

(1) I_{SD} ≤ 3A, di/dt ≤ 200A/μs, V_{DD} ≤ V_{(BR)DSS}, T_j ≤ T_{JMAX}.

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THERMAL DATA

Rthj-pcb	Thermal Resistance Junction-PC Board Max	50	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max (Surface Mounted)	60	°C/W
T _l	Maximum Lead Temperature For Soldering Purpose	260	°C

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 µA, V _{GS} = 0	60			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125 °C			1 10	µA µA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ±20V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250µA	2		4	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10V, I _D = 1.25 A		0.18	0.20	Ω
I _{D(on)}	On State Drain Current	V _{DS} > I _{D(on)} × R _{DS(on)} max, V _{GS} = 10V	2.5			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (1)	Forward Transconductance	V _{DS} > I _{D(on)} × R _{DS(on)} max, I _D = 1.25 A		1.5		S
C _{iss}	Input Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		850		pF
C _{oss}	Output Capacitance			230		pF
C _{rss}	Reverse Transfer Capacitance			75		pF

ELECTRICAL CHARACTERISTICS (CONTINUED)**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 30V, I_D = 6A$		20		ns
t_r	Rise Time	$R_G = 4.7\Omega, V_{GS} = 10V$ (see test circuit, Figure 3)		40		ns
Q_g	Total Gate Charge	$V_{DD} = 48V, I_D = 12A,$ $V_{GS} = 10V$		16	21	nC
Q_{gs}	Gate-Source Charge			4		nC
Q_{gd}	Gate-Drain Charge			6		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off-Delay Time	$V_{DD} = 30V, I_D = 6A,$		40		ns
t_f	Fall Time	$R_G = 4.7\Omega, V_{GS} = 10V$ (see test circuit, Figure 3)		10		ns
$t_{r(off)}$	Off-voltage Rise Time	$V_{clamp} = 48V, I_D = 12A$ $R_G = 4.7\Omega, V_{GS} = 10V$		10		ns
t_f	Fall Time	(see test circuit, Figure 5)		17		ns
t_c	Cross-over Time			30		ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				2.5	A
$I_{SDM} (1)$	Source-drain Current (pulsed)				10	A
$V_{SD} (2)$	Forward On Voltage	$I_{SD} = 2.5A, V_{GS} = 0$			1.2	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 12A, di/dt = 100A/\mu s,$		100		ns
Q_{rr}	Reverse Recovery Charge	$V_{DD} = 30V, T_J = 150^\circ C$		260		nC
I_{RRM}	Reverse Recovery Current	(see test circuit, Figure 5)		5.2		A

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

2. Pulse width limited by safe operating area.

Fig. 1: Unclamped Inductive Load Test Circuit

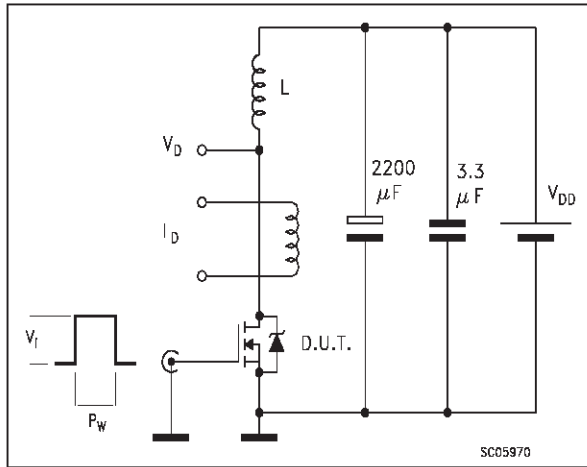


Fig. 2: Unclamped Inductive Waveform

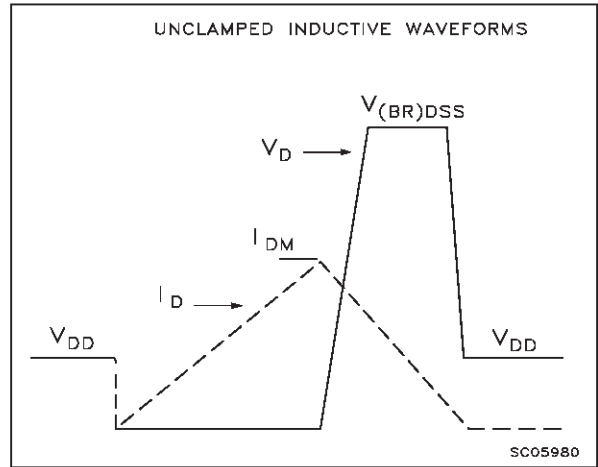


Fig. 3: Switching Times Test Circuit For Resistive Load

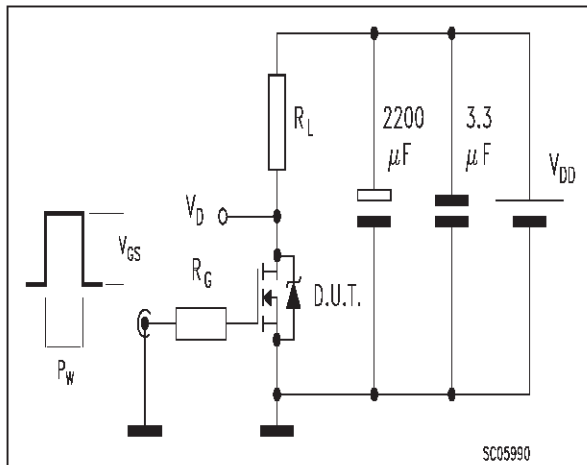


Fig. 4: Gate Charge test Circuit

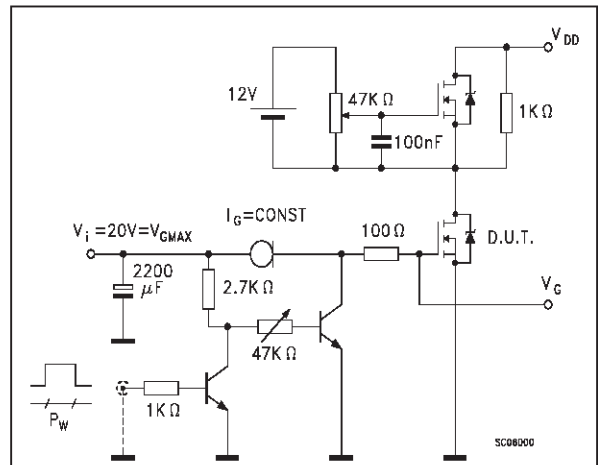
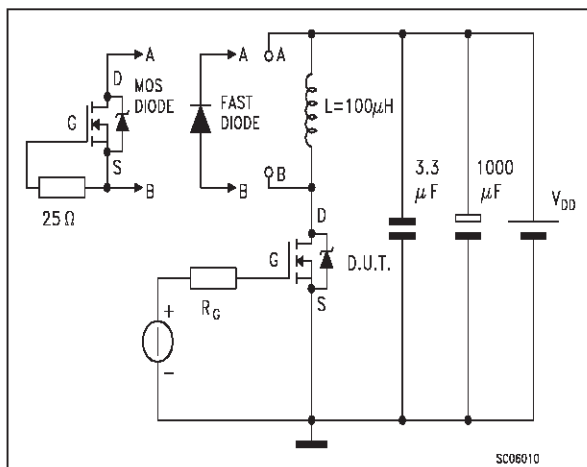
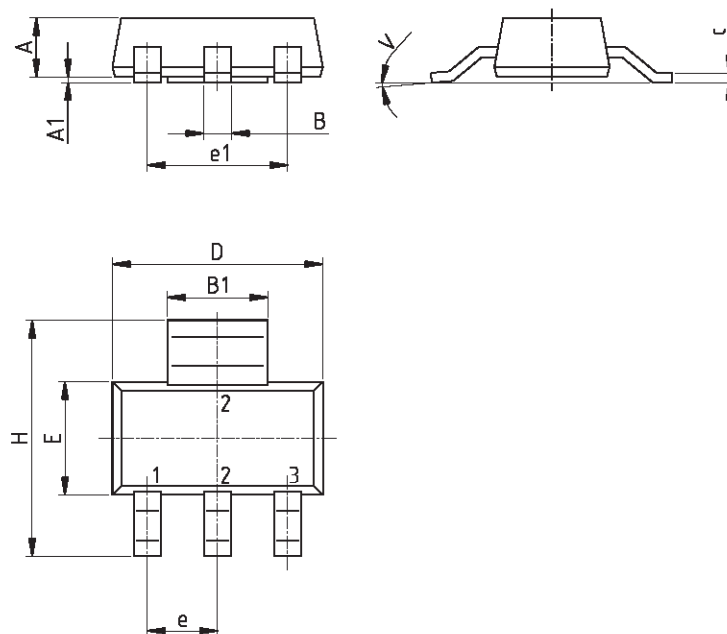


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



SOT-223 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.80			0.071
B	0.60	0.70	0.80	0.024	0.027	0.031
B1	2.90	3.00	3.10	0.114	0.118	0.122
c	0.24	0.26	0.32	0.009	0.010	0.013
D	6.30	6.50	6.70	0.248	0.256	0.264
e		2.30			0.090	
e1		4.60			0.181	
E	3.30	3.50	3.70	0.130	0.138	0.146
H	6.70	7.00	7.30	0.264	0.276	0.287
V			10°			10°
A1		0.02				



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