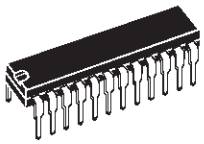
L6207

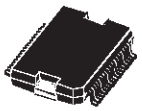
DUAL DMOS FULL BRIDGE DRIVER

PRELIMINARY DATA

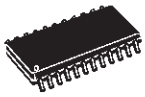
- OPERATING SUPPLY VOLTAGE FROM 8 TO 52V
- 5A PEAK CURRENT (2.8A DC)
- RDS ON 0.3Ω TYP. VALUE @ T_j = 25 °C
- BUILT-IN CONSTANT OFF TIME PWM CURRENT CONTROL
- HIGH SIDE OVER CURRENT SHUTDOWN PROTECTION 5.6A TYP.
- CROSS CONDUCTION PROTECTION
- THERMAL SHUTDOWN
- OPERATING FREQUENCY UP TO 100KHz
- INTRINSIC FAST FREE WHEELING DIODES.
- UVLO: UNDER VOLTAGE LOCKOUT



PowerDIP24 (20+2+2)



PowerSO36



SO24 (20+2+2)

ORDERING NUMBERS:

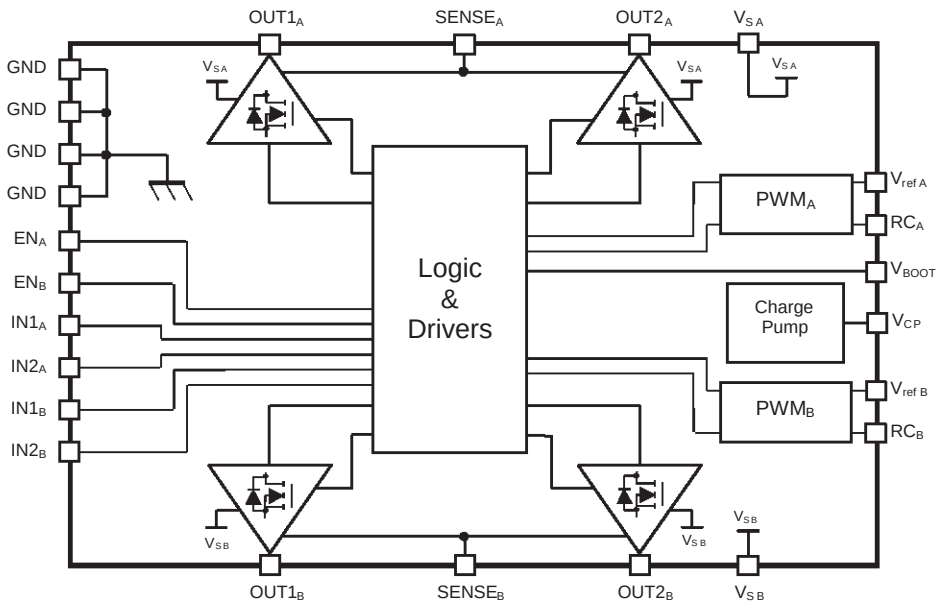
L6207N **L6207PD** **L6207D**

DESCRIPTION

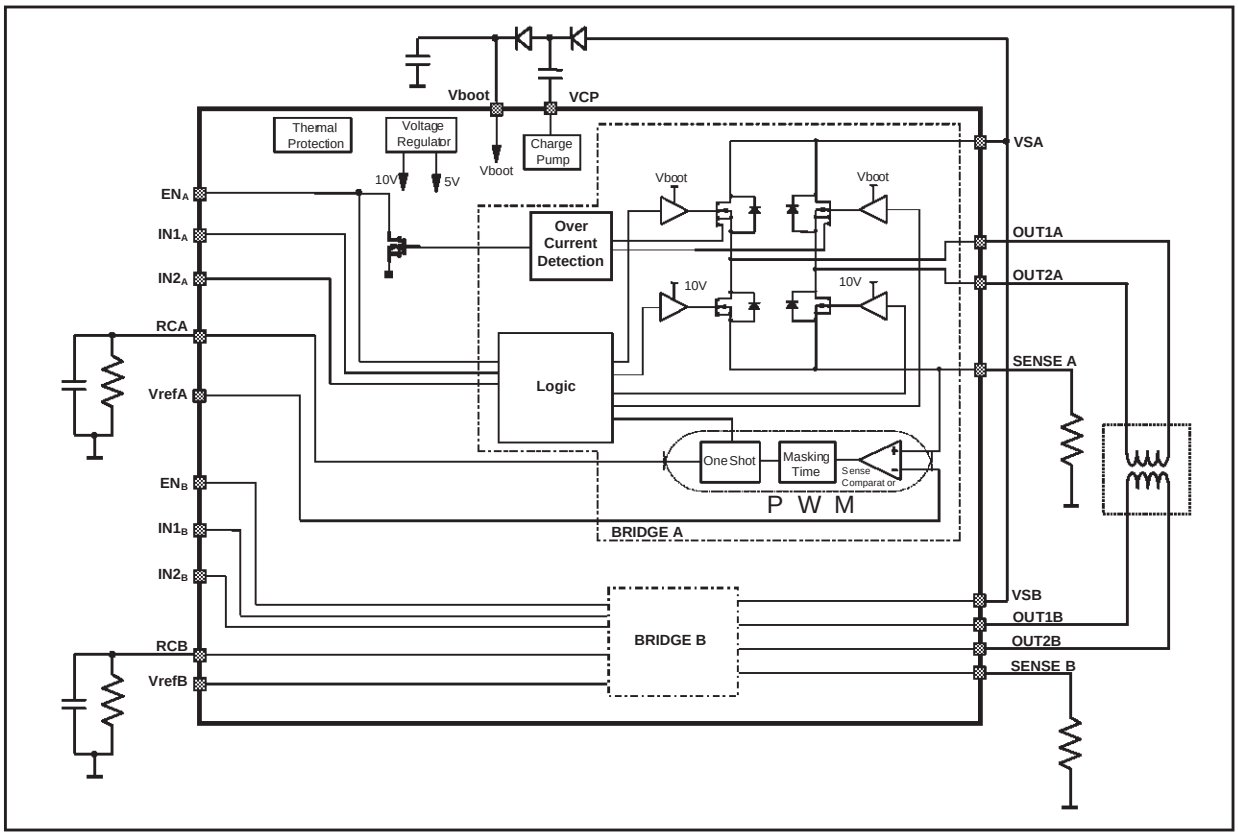
The L6207 is a dual full bridge driver for motor control manufactured with Multipower BCD technology which combines isolated DMOS power transistors with CMOS and bipolar circuits on the same chip.
The Logic Inputs are CMOS/TTL and µP compatible.

Additional circuitry to realize a constant off time PWM control has been implemented for each bridge.
Each full bridge is controlled by a separate Enable and has a sense pin for the current sense resistor insertion. Other features are the protection of the high side switches against unsafe over current conditions and the thermal shutdown.
The L6207 is assembled in PowerDIP24(20+2+2), PowerSO36 and SO24(20+2+2) packages.

BLOCK DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



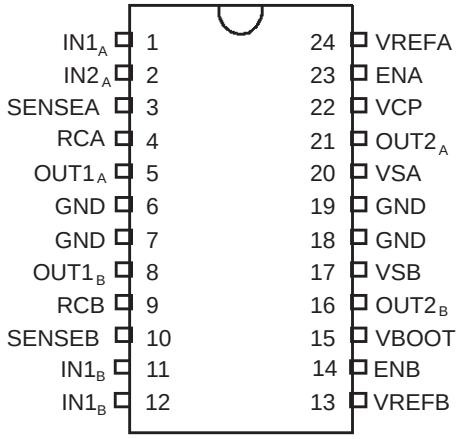
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test conditions	Value	Unit
V_S	Supply Voltage		60	V
V_{IN},V_{EN}	Input and Enable Voltage Range		-0.3 to +7	V
V_{refA}, V_{refB}	Voltage Range at V_{ref} pins		-0.3 to +7	V
$V_{RCA,VRCB}$	Voltage Range at RC_A and RC_B pins		-0.3 to +7	V
V_{SENSE}	DC Sensing Voltage Range		-1 to +4	V
V_{BOOT}	Bootstrap Peak Voltage		V_S + 10	V
$I_{S(peak)}$	Pulsed Supply Current (for each V_S pin), internally limited by the overcurrent protection.	t_{PULSE} < 1ms	7.1	A
I_S	DCvSupply Current (for each V_S pin)		2.8	A
V_{OD}	Differential Voltage Between $V_{S\,A}$, $OUT1_A$, $OUT2_A$, $SENSE_A$ and $V_{S\,B}$, $OUT1_B$, $OUT2_B$, $SENSE_B$		60	V
T_{stg}, T_{OP}	Storage and Operating Temperature Range		-40 to 150	°C

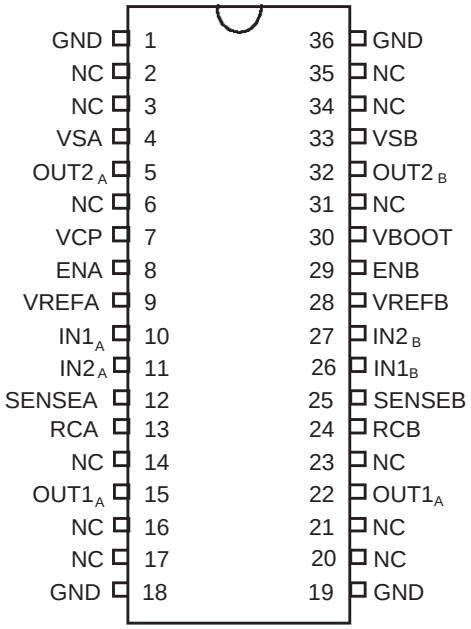
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		MIN	MAX	Unit
V_S	Supply Voltages		12	52	V
V_{OD}	Differential Voltage Between $V_{S\,A}$, $OUT1_A$, $OUT2_A$, $SENSE_A$ and $V_{S\,B}$, $OUT1_B$, $OUT2_B$, $SENSE_B$			52	V
V_{SENSE}	Sensing voltage (pulsed tw<t_{rr}) (DC)		-6 -1	6 1	V V
V_{ref}	V_{ref} Operating Voltage		-0.1	5	
I_{OUT}	DC Output Current			2.8	V
T_j	Operating Junction Temperature		-25	+125	°C
f_c	Commutation Frequency			100	kHz

PIN CONNECTION (Top View)



PDIP24/SO24



PowerSO36

PIN DESCRIPTION

Name	PowerSO36	PDIP24/ SO24	Function
V_{SA}	4	20	Supply Voltage of the Bridge A
V_{SB}	33	17	Supply Voltage of the Bridge B. This pin must be connected to VSA
$OUT1_A$ $OUT2_A$	15 5	5 21	Bridge A outputs.
$OUT1_B$ $OUT2_B$	22 32	8 16	Bridge B outputs.
SENSEA	12	3	Sense resistor for the bridge A
SENSEB	25	10	Sense resistor for the bridge B
GND	1,18,19,36	6,7,18,19	Common ground terminals. In Powerdip and SO packages, these pins are also used for heat dissipation toward the PCB.
ENA	8	23	Enable of the Bridge A. A LOW logic level applied to this pin switches off all the power DMOSs of the related bridge. The OCSA open drain is internally connected to this pin.
ENB	29	14	Enable of the Bridge B. A LOW logic level applied to this pin switches off all the power DMOSs of the related bridge. The OCSB open drain is internally connected to this pin.
$IN1_A$ $IN2_A$	10 11	1 2	Logic inputs of the Bridge B. Provided the ENA signal is HIGH, a HIGH logic level applied to any of these pins switches on the related high side power DMOS, while a logic LOW switches on the related low side power DMOS .
IN3 IN4	26 27	11 12	Logic inputs of the Bridge B. Provided the ENB signal is HIGH, a HIGH logic level applied to any of these pins switches on the related high side power DMOS, while a logic LOW switches on the related low side power DMOS .
V_{CP}	7	22	Bootstrap Oscillator. Oscillator output for the external charge pump.
V_{BOOT}	30	15	Supply voltage to overdrive the upper DMOSs.
RC_A	13	4	A parallel RC network connected to these pins sets the OFF time of the low-side power DMOS of the correspondent bridge. The pulse generator is a monostable triggered by the output of the sense comparator of the bridge (t_{OFF} = 0.69 RC).
RC_B	24	9	
$V_{ref\ A}$	9	24	A voltage applied to these pins sets the reference voltage of the sense comparators, determining the output current in PWM current control.
$V_{ref\ B}$	28	13	

THERMAL DATA

Symbol	Description	PDIP24	SO24	PowerSO36	Unit
$R_{th\text{-}j\text{-}pins}$	MaximumThermal Resistance Junction-Pins	18	14	-	°C/W
$R_{th\text{-}j\text{-}case}$	Maximum Thermal Resistance Junction-Case	-	-	1	°C/W
$R_{th\text{-}j\text{-}amb1}$	MaximumThermal Resistance Junction-Ambient [1]	42	50	35	°C/W
$R_{th\text{-}j\text{-}amb2}$	Maximum Thermal Resistance Junction-Ambient [2]	58	77	62	°C/W

<1>Mounted on a multiplayer PCB with a dissipating copper surface on the bottom side of 2 x 12mm x 25mm (with a thickness of at least 35 µm).
<2>It's the same condition of the point above, without any heatsinking surface on the board.

ELECTRICAL CHARACTERISTICS

(T_{amb} = 25 °C, V_S = 48V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_S	Supply Voltage		8		52	V
I_S	Quiescent Supply Current	All Bridges OFF		5.5	10	mA
T_j	Thermal Shutdown Temperature		150			°C
Output DMOS Transistors						
I_{DSS}	Leakage Current	V_S = 52V			1	mA
$R_{DS(ON)}$	High-side Switch ON Resistance	T_j = 25 °C		0.34	0.4	Ω
		T_j =125 °C		0.53	0.59	Ω
	Low-side Switch ON Resistance	T_j = 25 °C		0.28	0.34	Ω
		T_j =125 °C		0.47	0.53	Ω
Source Drain Diodes						
V_{SD}	Forward ON Voltage	I_{SD} = 2.8A, EN = LOW		1.2	1.4	V
t_{rr}	Reverse Recovery Time	I_f = 2.8A		300		ns
t_{fr}	Forward Recovery Time			200		ns
Switching Rates						
$t_{D(on)EN}$	Enable to out turn ON delay time [3]	I_{LOAD} = 2.8 A		250		ns
$t_{D(on)IN}$	Input to out turn ON delay time [3]	I_{LOAD} = 2.8 A		600		ns
t_{ON}	Output rise time[3]	I_{LOAD} = 2.8 A	20	105	300	ns
$t_{D(off)EN}$	Enable to out turn OFF delay time [3]	I_{LOAD} = 2.8 A		450		ns
$t_{D(off)IN}$	Input to out turn OFF delay time [3]	I_{LOAD} = 2.8 A		500		ns
t_{off}	Output fall time[3]	I_{LOAD} = 2.8 A	20	78	300	ns

ELECTRICAL CHARACTERISTICS (continued)
(T_{amb} = 25 °C, V_S = 48V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t_{dt}	Dead time protection			1		µs
t_{blank}	Internal blanking time on SENSE pins			1	1.5	µs
f_{CP}	Charge pump frequency			0.75	1	MHz
UVLO comp						
$V_{th(ON)}$	Turn ON threshold		6.6	7	7.4	µs
$V_{th(OFF)}$	Turn OFF threshold		5.6	6	6.4	µs
Logic Input						
V_{INL}	Low level logic input voltage		-0.3		0.8	V
V_{INH}	High level logic input voltage		2		7	V
I_{INH}	High level logic input current	$V_{IN, EN}$ = 5 V			70	µA
I_{INL}	Low level logic input current	$V_{IN, EN}$ = GND			-10	µA
Over Current Protection						
$I_{S\ OVER}$	Input supply over current protection threshold	Tj = 25 °C	4	5.6	7.1	A
V_{DIAG}	Open drain low level output voltage	I = 4 mA			0.4	V
Comparator and Monostable						
$I_{RCA, RCB}$	Source current at RC pins	V_{RC}=2.5 V	3	5		mA
V_{ref}	Input common mode comparator voltage range		-0.1		5	V
V_{th}	Comparator threshold voltage on SENSE pins	$V_{ref\ A, B}$ = 0.5 V	V_{ref} - 5mV		V_{ref} + 5mV	
t_{prop}	Turn OFF propagation delay (4)	$V_{ref\ A, B}$ = 0.5 V	0.1	0.2	0.3	µs
t_{OFF}	PWM Recirculation time	20 kΩ < R < 100 kΩ 0.1 nF < C < 100 nF	0.67RC	0.69RC	0.71RC	s
I_{bias}	Input bias current at V_{ref} pins			0.2		µA
UVLO comp						
V_{thon}	Turn On Threshold		6.6	7	7.4	V
V_{thoff}	Turn Off		5.6	6	6.4	V

<(3)>Resistive load used. See Fig. 1.
<(4)>Defined as the time between the voltage at the input of the current sense reaching the V_{ref} threshold and the lower DMOS switch beginning to turn off. The voltage at SENSE pin is increased instantaneously from V_{ref} -10 mV to V_{ref} +10 mV.

Figure 1. Switching rates definition

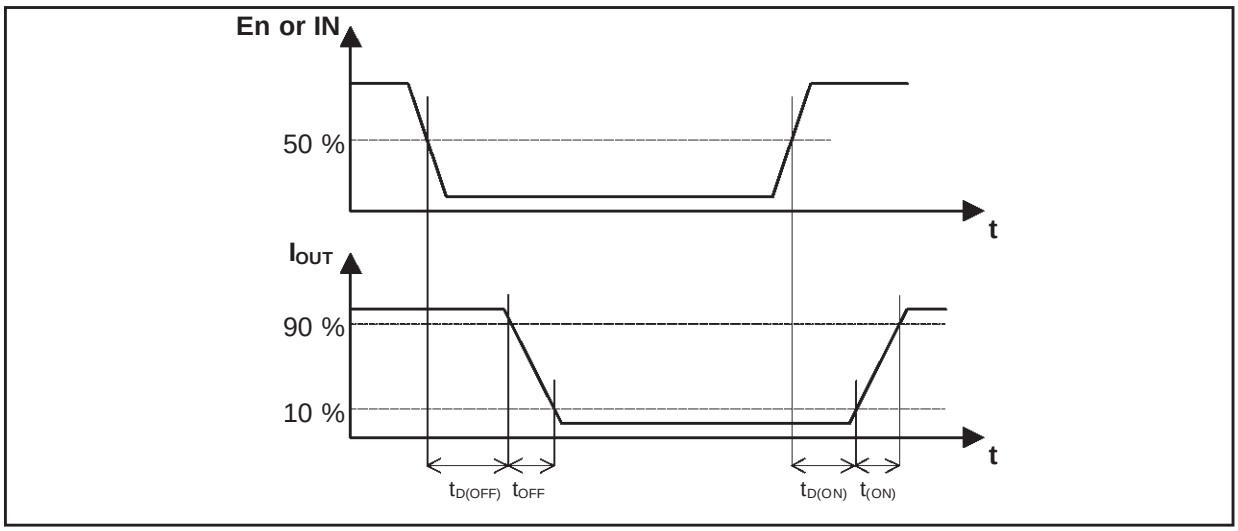


Figure 2. Typical Quiescent Current vs. Supply Voltage

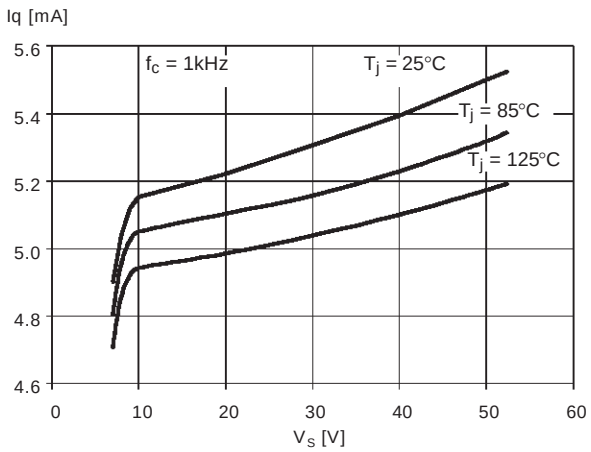


Figure 3. Normalized Typical Quiescent Current vs. Switching Frequency

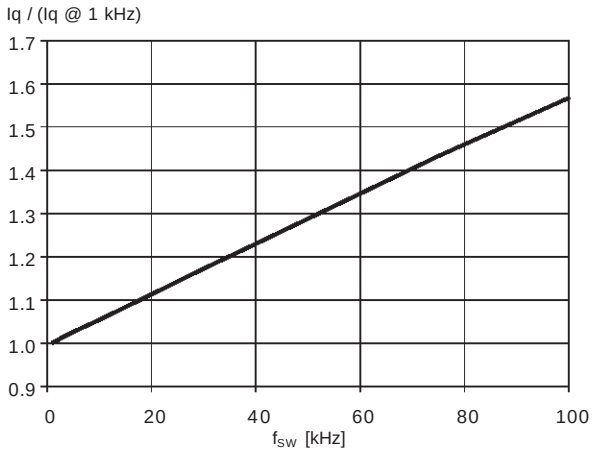


Figure 4. Typical Low-Side RDS(ON) vs. Supply Voltage

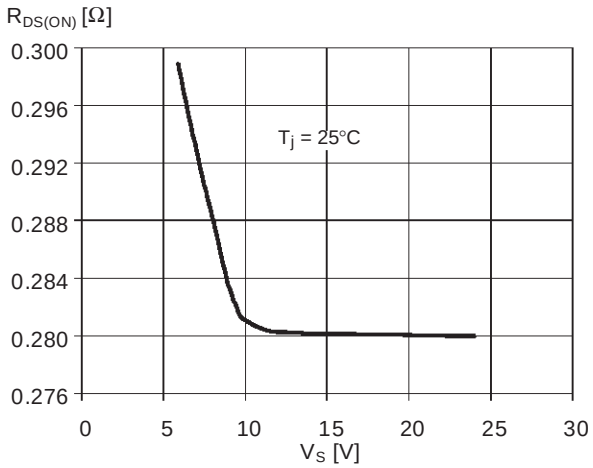


Figure 5. Typical High-Side RDS(ON) vs. Supply Voltage

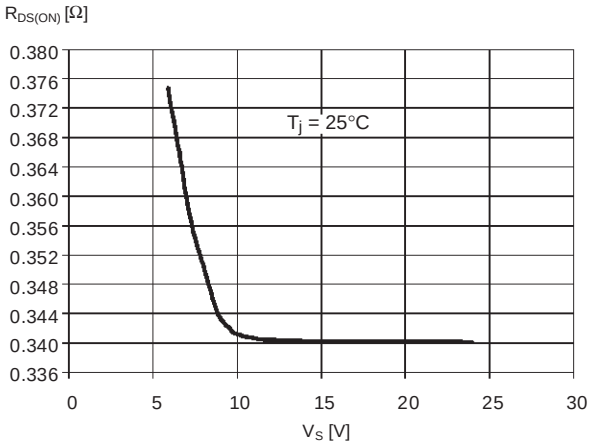


Figure 6. Normalized $R_{DS(ON)}$ vs.Junction Temperature (typical value)

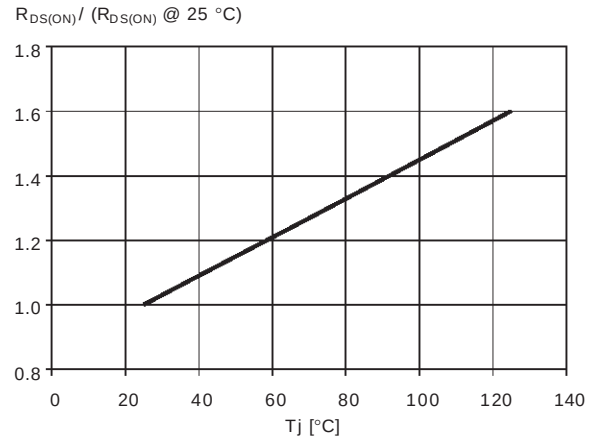
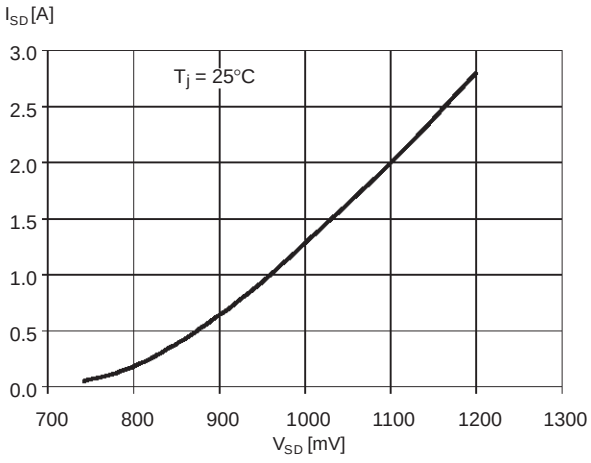


Figure 7. Typical Drain-Source Diode Forward ON Characteristic



CIRCUIT DESCRIPTION

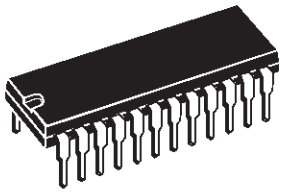
The L6207 is a dual full bridge IC designed to drive DC or Stepper motors and other inductive loads. Each bridge has 4 power DMOS transistors with a typical R_{DSON} of 0.3 Ohm. Any of the 4 half bridges can be controlled independently by means of the 4 TTL/CMOS compatible inputs $IN1_A$, $IN2_A$, $IN1_B$, $IN2_B$, and 2 enable ENA, ENB .

External connections are provided so that sensing resistor can be added for constant current chopping application. A non dissipative current sensing on the supply rails to the high side power DMOS of each bridge, together with an Internal Reference and an internal open drain, with a pull down capability of 4mA (typical value) will pull to GND the ENABLE pin of the bridge under fault conditions, turning OFF all the four PowerMOS. This ensures a protection against Short Circuit to GND and between two phases of each of the two independent full bridges. By using an external R-C on the EN pins, the off time before recover normal operation conditions after a fault can be easily programmed, by means of the accurate threshold of the logic inputs. Note that protection for short to the supply rail is typically provided by the external current control circuitry.The trip point of this protection is internally set at 5.6A (typ value). For each of the two indipendent bridges a monostable and a comparator can be used to perform a constant t_{off} current control.

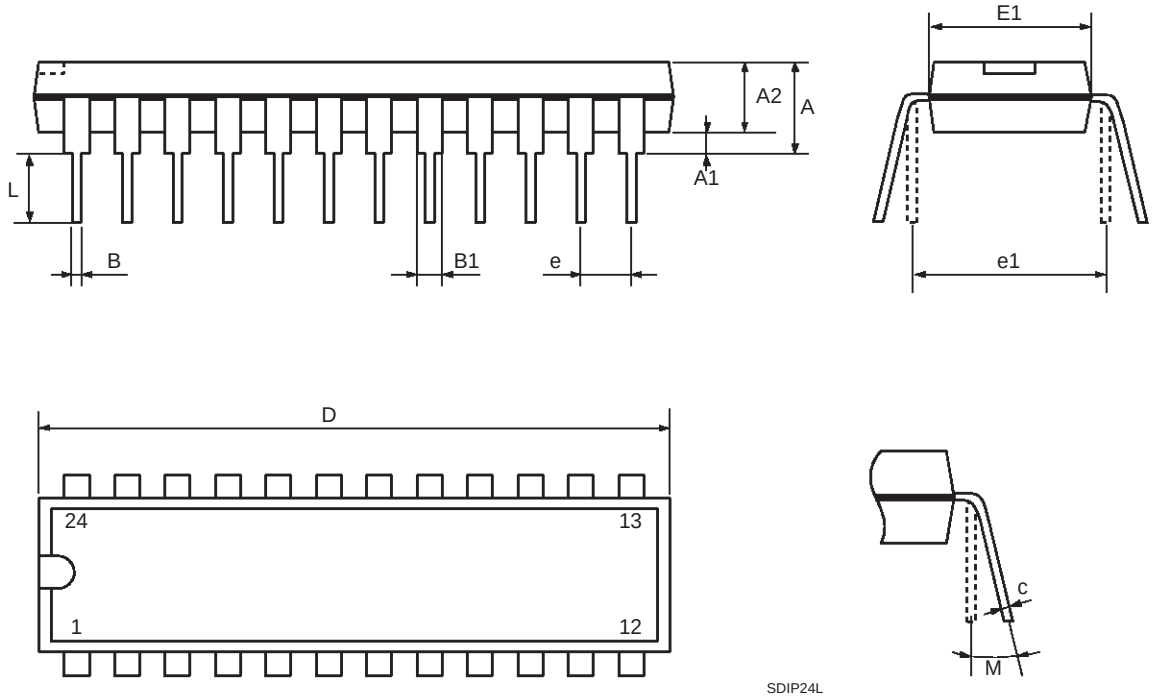
This features makes the L6207 a complete bipolar stepper motor driver, or a Dual DC Motor Driver, that outperforms the component currently available on the market.

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.320			0.170
A1	0.380			0.015		
A2		3.300			0.130	
B	0.410	0.460	0.510	0.016	0.018	0.020
B1	1.400	1.520	1.650	0.055	0.060	0.065
c	0.200	0.250	0.300	0.008	0.010	0.012
D	31.62	31.75	31.88	1.245	1.250	1.255
E	7.620		8.260	0.300		0.325
e		2.54			0.100	
E1	6.350	6.600	6.860	0.250	0.260	0.270
e1		7.620			0.300	
L	3.180		3.430	0.125		0.135
M	0° min, 15° max.					

OUTLINE AND MECHANICAL DATA

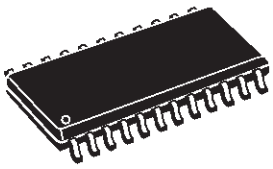


Powerdip 24

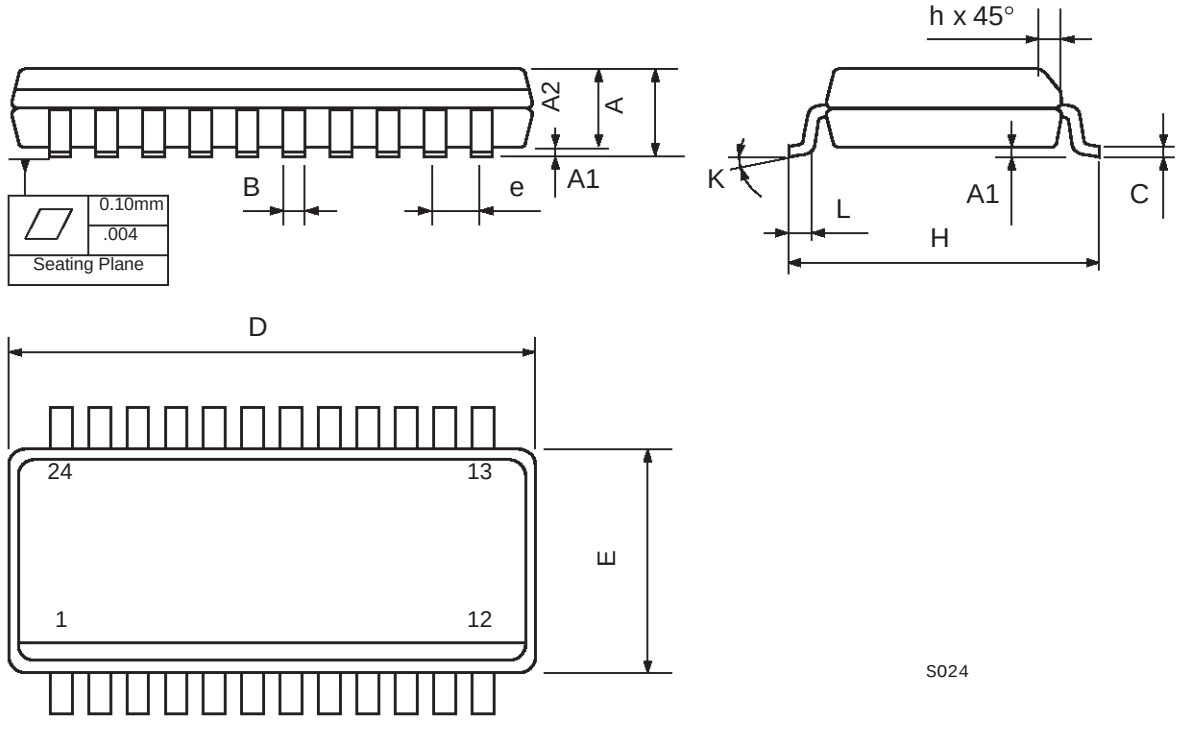


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.10		0.30	0.004		0.012
A2			2.55			0.100
B	0.33		0.51	0.013		0.0200
C	0.23		0.32	0.009		0.013
D	15.20		15.60	0.598		0.614
E	7.40		7.60	0.291		0.299
e		1.27			0,050	
H	10.0		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
k	0° (min.), 8° (max.)					
L	0.40		1.27	0.016		0.050

OUTLINE AND MECHANICAL DATA



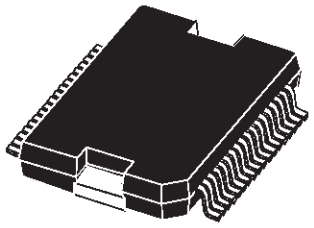
SO24



DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.60			0.141
a1	0.10		0.30	0.004		0.012
a2			3.30			0.130
a3	0		0.10	0		0.004
b	0.22		0.38	0.008		0.015
c	0.23		0.32	0.009		0.012
D (1)	15.80		16.00	0.622		0.630
D1	9.40		9.80	0.370		0.385
E	13.90		14.50	0.547		0.570
e		0.65			0.0256	
e3		11.05			0.435	
E1 (1)	10.90		11.10	0.429		0.437
E2			2.90			0.114
E3	5.80		6.20	0.228		0.244
E4	2.90		3.20	0.114		0.126
G	0		0.10	0		0.004
H	15.50		15.90	0.610		0.626
h			1.10			0.043
L	0.80		1.10	0.031		0.043
N	10°(max.)					
S	8 °(max.)					

(1): "D" and "E1" do not include mold flash or protrusions
- Mold flash or protrusions shall not exceed 0.15mm (0.006 inch)
- Critical dimensions are "a3", "E" and "G".

OUTLINE AND MECHANICAL DATA



PowerSO36