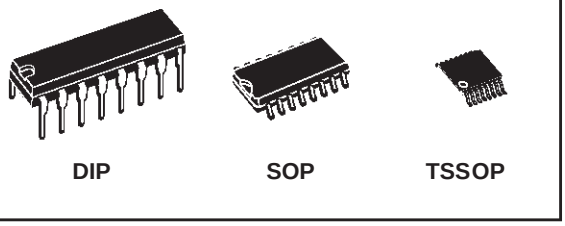
74HC165

8 BIT PISO SHIFT REGISTER

- HIGH SPEED: t_{PD} = 15ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION: I_{CC} = 4µA(MAX.) at T_A=25°C
- HIGH NOISE IMMUNITY: $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- SYMMETRICAL OUTPUT IMPEDANCE: $|I_{OH}| = I_{OL}$ = 4mA (MIN)
- BALANCED PROPAGATION DELAYS: $t_{PLH} \cong t_{PHL}$
- OUTPUTS DRIVE CAPABILITY 10 LSTTL LOADS
- WIDE OPERATING VOLTAGE RANGE: V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 165



ORDER CODES

PACKAGE	TUBE	T & R
DIP	M74HC165B1R	
SOP	M74HC165M1R	M74HC165RM13TR
TSSOP		M74HC165TTR

DESCRIPTION

The HC165 is an high speed CMOS 8 BIT PISO SHIFT REGISTER fabricated with silicon gate C^2MOS tecnology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

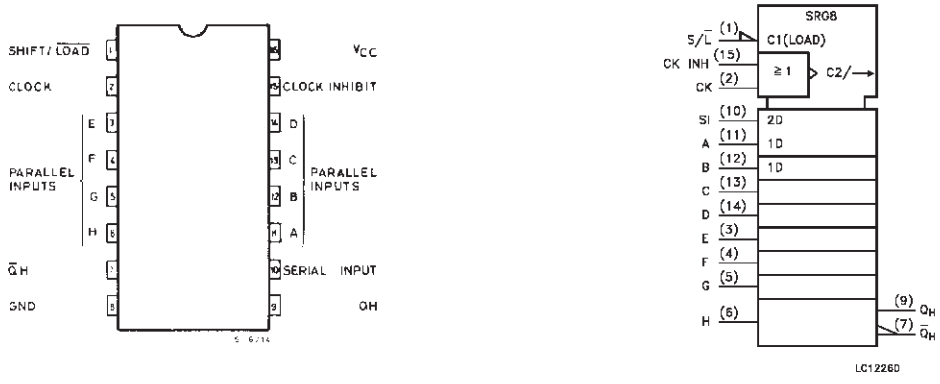
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

This device contains eight clocked master slave RS flip-flops connected as a shift register, with auxiliary gating to provide over-riding asynchronous parallel entry. Parallel data entres when the shift/load input is low. The parallel data can change while shift/load is low, provided that the recommended set-up and hold times are observed. For clocked operation, shift/load must be high. The two clock input perform identically; one can be used as a clock inhibit by applying a high signal; to permit this operation clocking is accomplished through a 2 input nor gate.

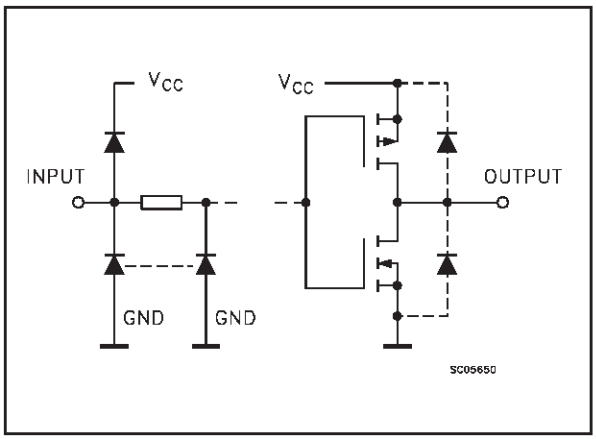
To avoid double clocking, however, the inhibit signal should only go high while the clock is high. Otherwise the rising inhibit signal will cause the same response as rising clock edge.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS



INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{S/L}$	Asynchronous Parallel Load Input
2	$\overline{QH}$	Complementary Output
7	QH	Serial Output
9	CLOCK	Clock Input (LOW to HIGH edge triggered)
10	SI	Serial Data Input
11, 12, 13, 14, 3, 4, 5, 6	A to H	Parallel Data Inputs
15	CLOCK INH	Clock Inhibit
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

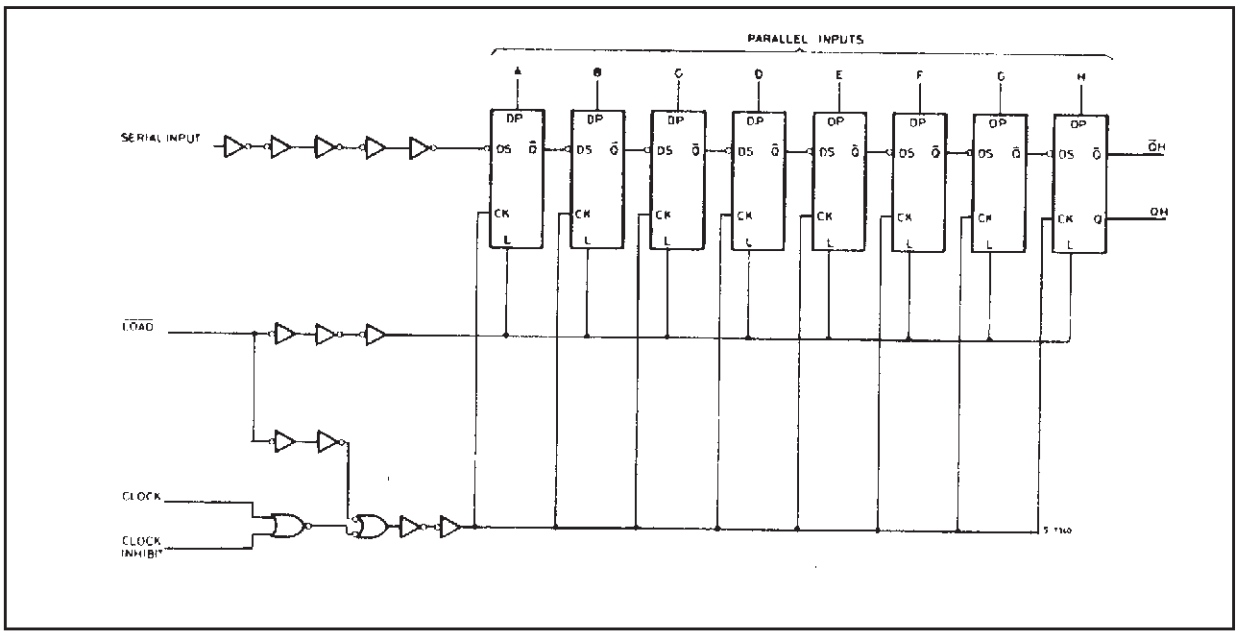
TRUTH TABLE

INPUTS					INTERNAL OUTPUTS		OUTPUT
$\overline{S/L}$	CLOCK INH	CLOCK	SERIAL IN	A ..... H	QA	QB	QH
L	X	X	X	a ..... h	a	b	h
H	L	⌐	H	X	H	QA_n	QG_n
H	L	⌐	L	X	L	QA_n	QG_n
H	⌐	L	H	X	H	QA_n	QG_n
H	⌐	L	L	X	L	QA_n	QG_n
H	X	H	X	X	NO CHANGE		
H	H	X	X	X	NO CHANGE		

a.....h: The level of steady input voltage at inputs a through respectively

QAn - QGn: The level of QA - QG, respectively before the most recent transition of the clock.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500(*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Rating are those value beyond which damage to the device may occour. Functional operation under these condition is not implied
(*) 500mW at 65 °C; derate to 300mW by 10mW/°C from 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperqture		-40 to 85	°C
dt/dv	Input Rise and Fall Time	V_{CC} = 2.0V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	ns
		V_{CC} = 6.0V	0 to 400	ns

DC SPECIFICATION

Symbol	Parameter	Test Condition		Value					Unit
		V_{CC} (V)		T_A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0		1.5			1.5		V
		4.5		3.15			3.15		
		6.0		4.2			4.2		
V_{IL}	Low Level Input Voltage	3.0				0.5		0.5	V
		4.5				1.35		1.35	
		5.5				1.8		1.8	
V_{OH}	High Level Ouput Voltage	2.0	I_O=-20 µA	1.9	2.0		1.9		V
		4.5	I_O=-20 µA	4.4	4.5		4.4		
		6.0	I_O=-20 µA	5.9	6.0		5.9		
		4.5	I_O=-4 mA	4.18	4.31		4.13		
		6.0	I_O=-5.2 mA	5.68	5.8		5.63		
V_{OL}	Low Level Output Voltage	2.0	I_O=20 µA		0.0	0.1		0.1	V
		4.5	I_O=20 µA		0.0	0.1		0.1	
		6.0	I_O=20 µA		0.0	0.1		0.1	
		4.5	I_O=4 mA		0.17	0.26		0.33	
		6.0	I_O=5.2 mA		0.18	0.26		0.33	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND			± 0.1		± 1	µA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND			4		40	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6ns)

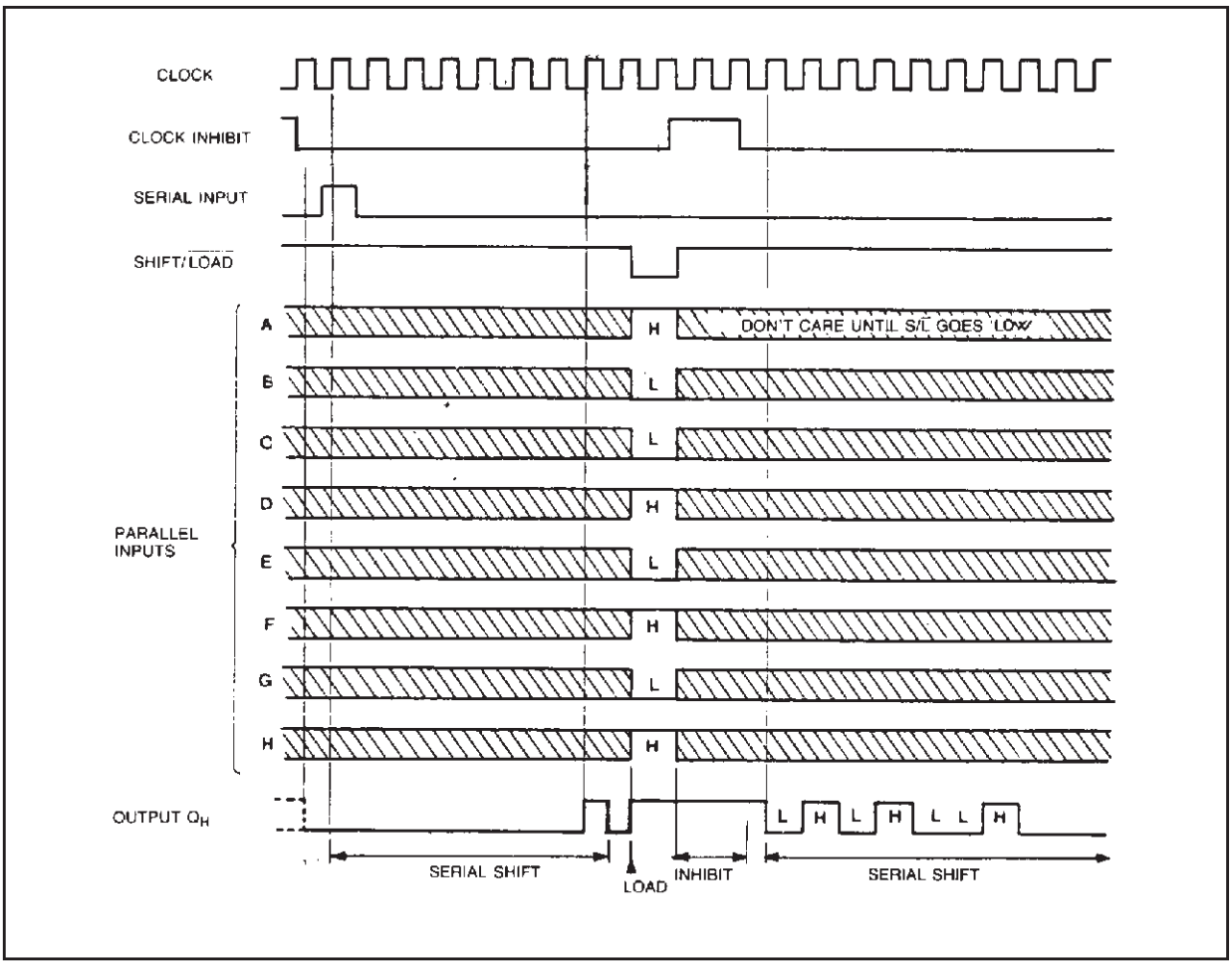
Symbol	Parameter	Test Condition		Value					Unit
		V_{CC} (V)		T_A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
t_{PLH} t_{PHL}	Propagation Delay Time (CK - QH, $\overline{QH}$)	2.0			55	150		190	ns
		4.5			18	30		38	
		6.0			15	26		33	
t_{PLH} t_{PHL}	Propagation Delay Time (S/$\overline{L}$ - QH, $\overline{QH}$)	2.0			65	165		205	ns
		4.5			21	33		41	
		6.0			18	28		35	
t_{PLH} t_{PHL}	Propagation Delay Time (H - QH, $\overline{QH}$)	2.0			55	135		170	ns
		4.5			17	27		34	
		6.0			14	23		29	
f_{MAX}	Maximum Clock Frequency	2.0		7.4	15		6.0		MHz
		4.5		37	60		30		
		6.0		44	71		35		
$t_{(W)H}$ $t_{(W)L}$	Minimum Pulse Width (CK)	2.0			24	75		95	ns
		4.5			6	15		19	
		6.0			5	13		16	
$t_{(W)L}$	Minimum Pulse Width (S/$\overline{L}$)	2.0			32	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
t_s	Minimum Set-up Time (PI - S/$\overline{L}$) (SI - CK) (S/$\overline{L}$ - CK)	2.0			24	75		95	ns
		4.5			6	15		19	
		6.0			5	13		16	
t_h	Minimum Set-up Time (S/$\overline{L}$ - PI) (CK - SI) (CK - S/$\overline{L}$)	2.0				0		0	ns
		4.5				0		0	
		6.0				0		0	
t_{REM}	Minimum Removal Time (CK - CKINH)	2.0			20	75		95	ns
		4.5			5	15		19	
		6.0			4	13		16	

CAPACITANCE CHARACTERISTICS

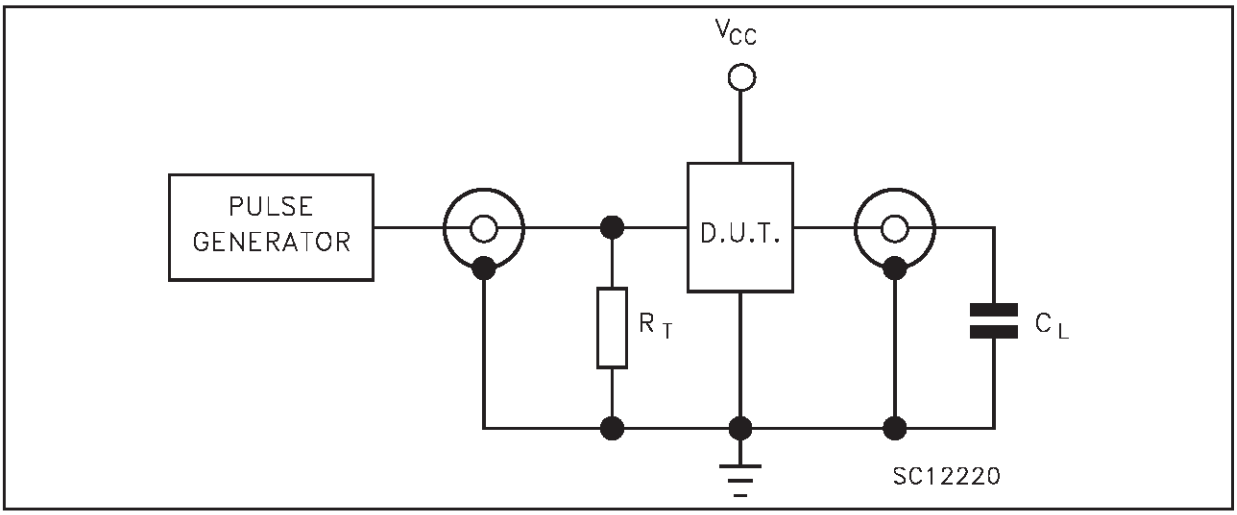
Symbol	Parameter	Test Condition		Value					Unit
		V_{CC} (V)		T_A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
C_{IN}	Input Capacitance	5.0			5		10		pF
C_{PD}	Power Dissipation Capacitance (note 1)	5.0			55				pF

1) C_{PD} is defined as the value of the IC's internal equivqlent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average current cqn be obtqined by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$

TIMING CHART

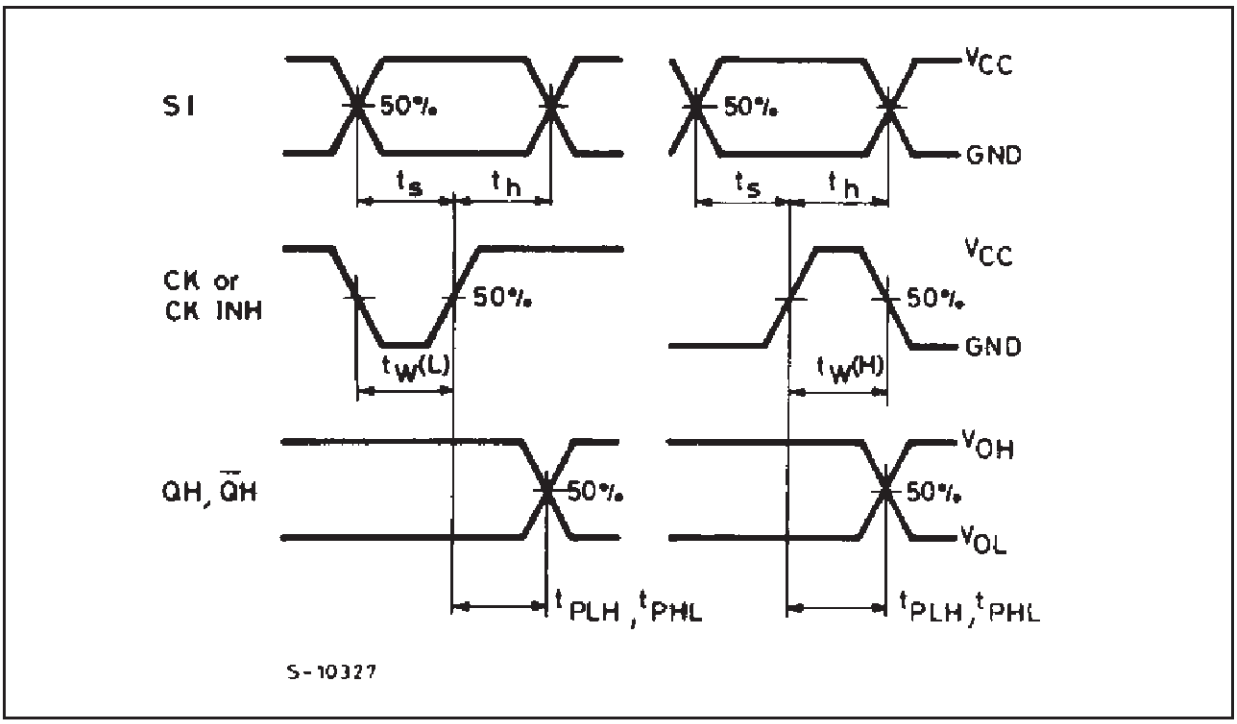


TEST CIRCUIT

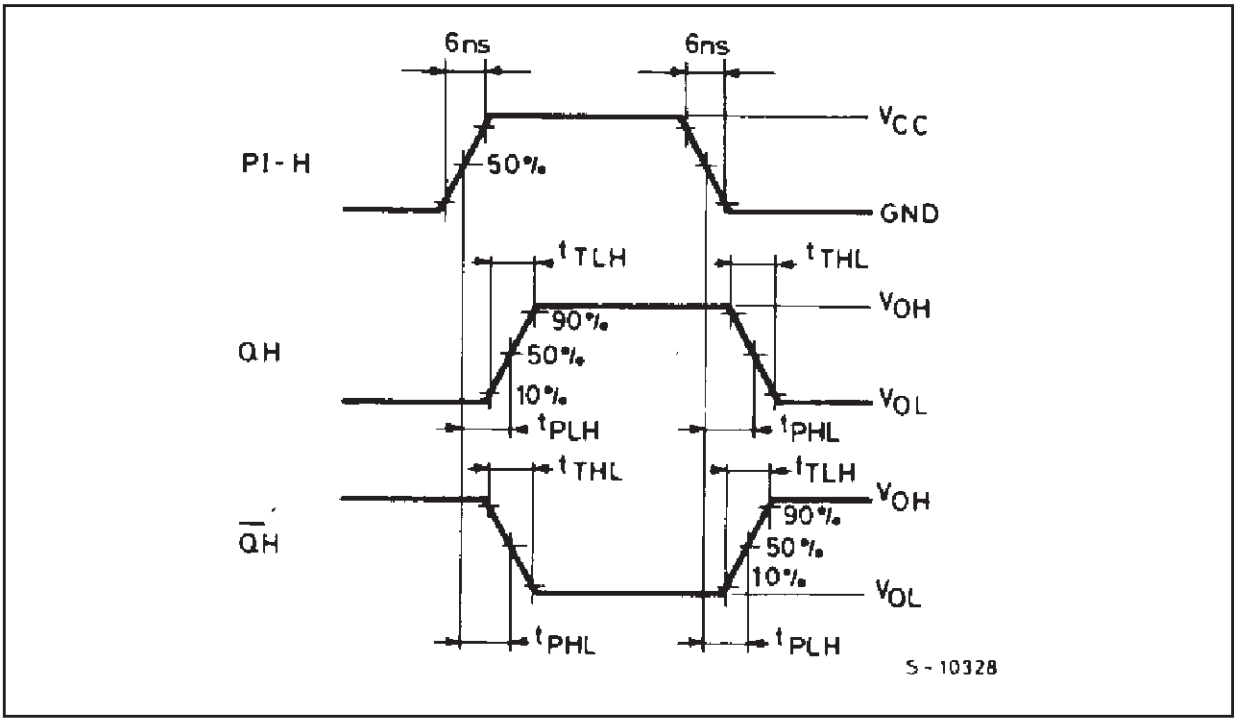


C_L = 50pF or equivalent (includes jig and probe capacitance)
R_T = Z_{OUT} of pulse generator (typically 50Ω)

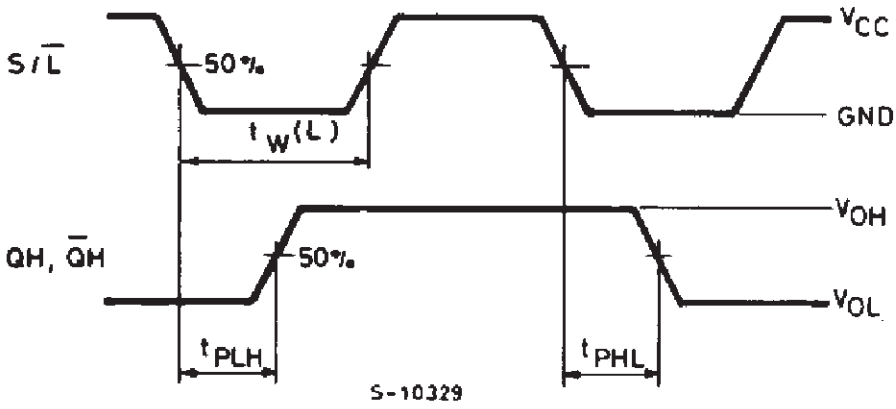
WAVEFORM 1: SERIAL MODE PROPAGATION DELAY (f=1MHz; 50% duty cycle)



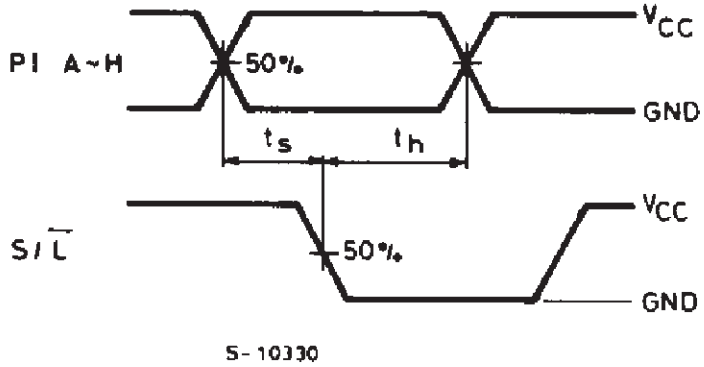
WAVEFORM 2: PARALLEL MODE PROPAGATION DELAY (f=1MHz; 50% duty cycle)



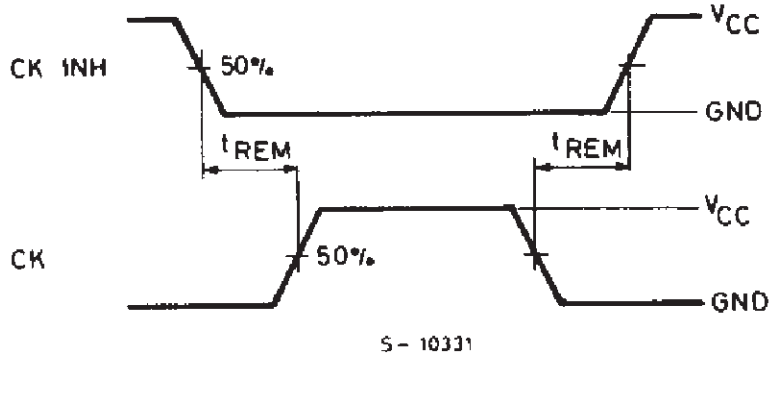
WAVEFORM 3: PARALLEL MODE PROPAGATION DELAY (f=1MHz; 50% duty cycle)



WAVEFORM 4: PARALLEL MODE PROPAGATION DELAY (f=1MHz; 50% duty cycle)

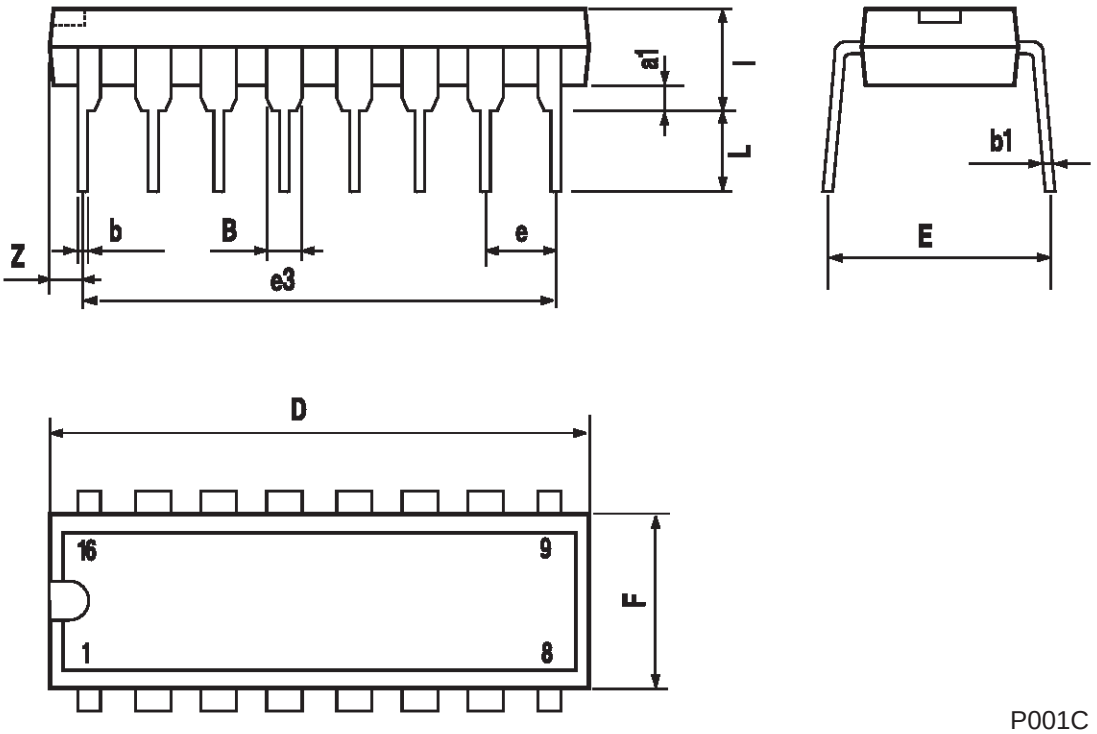


WAVEFORM 5: PARALLEL MODE PROPAGATION DELAY (f=1MHz; 50% duty cycle)



Plastic DIP-16 (0.25) MECHANICAL DATA

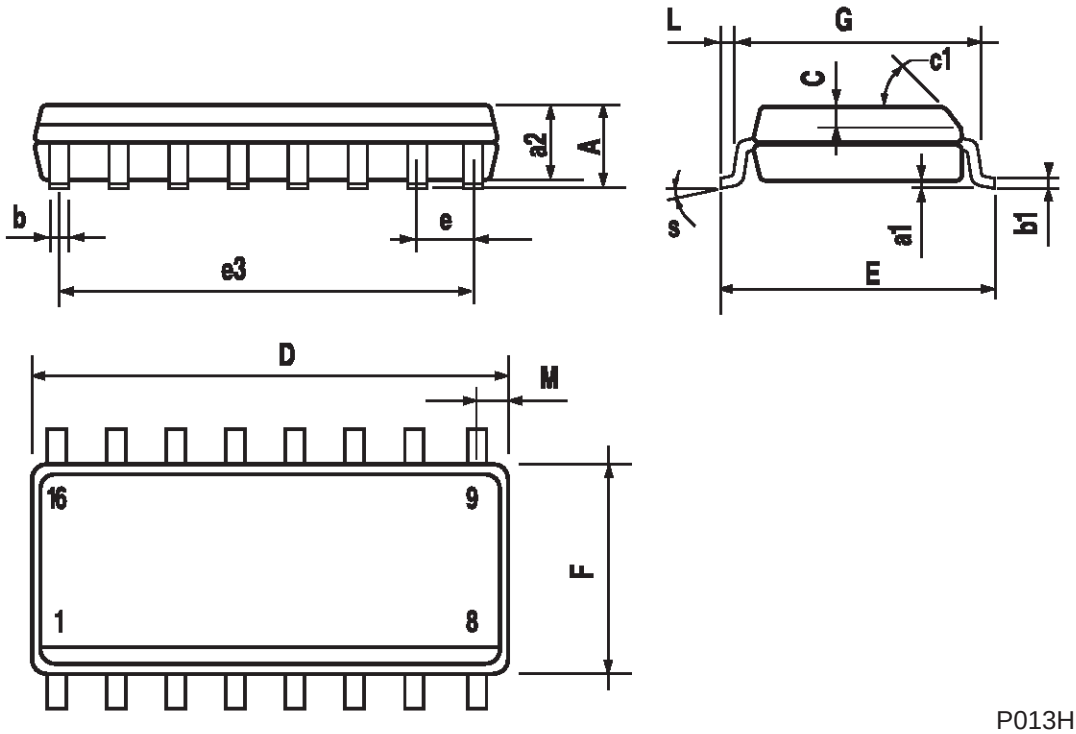
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



P001C

SO-16 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.004		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45 (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8 (max.)					



P013H

TSSOP16 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.1			0.433
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.85	0.9	0.95	0.335	0.354	0.374
b	0.19		0.30	0.0075		0.0118
c	0.09		0.20	0.0035		0.0079
D	4.9	5	5.1	0.193	0.197	0.201
E	6.25	6.4	6.5	0.246	0.252	0.256
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0^o	4^o	8^o	0^o	4^o	8^o
L	0.50	0.60	0.70	0.020	0.024	0.028