



74ACT16541

16-BIT BUS BUFFER WITH 3-STATE OUTPUTS (NON INVERTED)

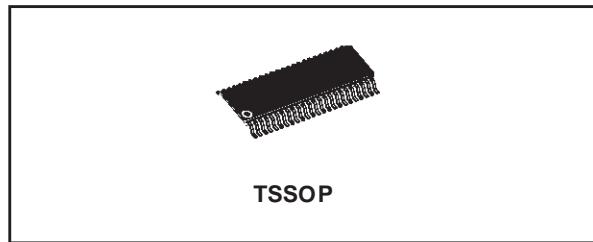
- HIGH SPEED: $t_{PD} = 4.8\text{ns}$ (TYP.) at $V_{CC} = 5\text{V}$
- LOW POWER DISSIPATION:
 $I_{CC} = 8\mu\text{A}$ (MAX.) at $T_A=25^\circ\text{C}$
- COMPATIBLE WITH TTL OUTPUTS
 $V_{IH} = 2\text{V}$ (MIN.), $V_{IL} = 0.8\text{V}$ (MAX.)
- 50Ω TRANSMISSION LINE DRIVING CAPABILITY
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 24\text{mA}$ (MIN)
- OPERATING VOLTAGE RANGE:
 V_{CC} (OPR) = 4.5V to 5.5V
- IMPROVED LATCH-UP IMMUNITY

DESCRIPTION

The ACT16541 is an advanced high-speed CMOS 16-BIT BUS BUFFER (3-STATE) fabricated with sub-micron silicon gate and double-layer metal wiring C²MOS technology.

This device is designed to interface directly High Speed CMOS systems with TTL and NMOS components.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

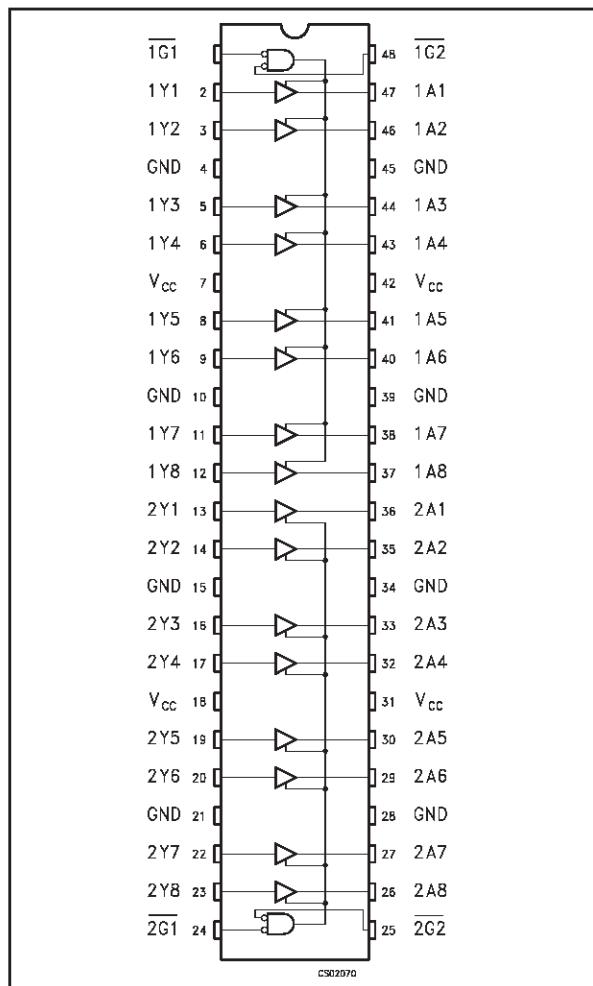


TSSOP

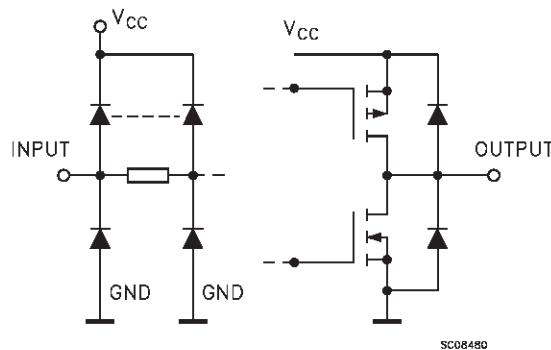
ORDER CODES

PACKAGE	TUBE	T & R
TSSOP		74ACT16373TTR

PIN CONNECTION



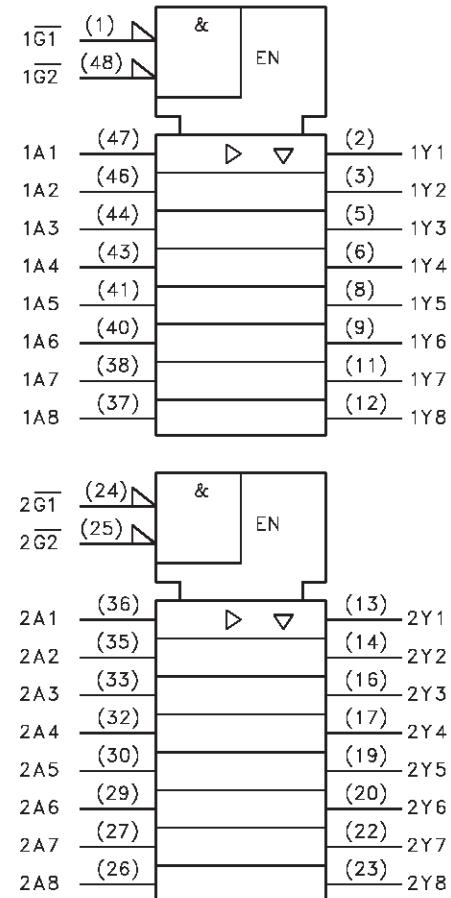
INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME QND FUNCTION
1, 48	1G1, 1G2	Output Enable Inputs
2, 3, 5, 6, 8, 9, 11, 12	1Y1 to 1Y8	Data Outputs
13, 14, 16, 17, 19, 20, 22, 23	2Y1 to 2Y8	Data Outputs
24, 25	2G1, 2G2	Output Enable Inputs
36, 35, 33, 32, 30, 29, 27, 26	2A1 to 2A8	Data Outputs
47, 46, 44, 43, 41, 40, 38, 37	1A1 to 1A8	Data Outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V _{CC}	Positive Supply Voltage

IEC LOGIC SYMBOLS



TRUTH TABLE

INPUTS			OUTPUT
$\overline{G1}$	$\overline{G2}$	A _n	Y _n
H	X	X	Z
X	H	X	Z
L	L	H	H
L	L	L	L

X: "H" or "L"
Z: High Impedance

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
V_O	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 400	mA
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature	-40 to 85	°C
dt/dv	Input Rise and Fall Time $V_{CC} = 4.5$ to 5.5V (note 1)	8	ns/V

1) V_{IN} from 0.8V to 2.0V

DC SPECIFICATION

Symbol	Parameter	Test Condition		Value					Unit	
		V _{CC} (V)		T _A = 25 °C			-40 to 85 °C			
				Min.	Typ.	Max.	Min.	Max.		
V _{IH}	High Level Input Voltage	4.5	V _O = 0.1 V or V _{CC} -0.1V	2.0			2.0		V	
		5.5		2.0			2.0			
V _{IL}	Low Level Input Voltage	4.5	V _O = 0.1 V or V _{CC} -0.1V			0.8		0.8	V	
		5.5				0.8		0.8		
V _{OH}	High Level Output Voltage	4.5	I _O =-50 μA	4.4	4.49		4.4		V	
		5.5	I _O =-50 μA	5.4	5.49		5.4			
		4.5	I _O =-24 mA	3.94			3.8			
		5.5	I _O =-24 mA	4.94			4.8			
V _{OL}	Low Level Output Voltage	4.5	I _O =50 μA		0.001	0.1		0.1	V	
		5.5	I _O =50 μA		0.001	0.1		0.1		
		4.5	I _O =24 mA			0.36		0.44		
		5.5	I _O =24 mA			0.36		0.44		
I _I	Input Leakage Current	5.5	V _I = V _{CC} or GND			± 0.1		± 1	μA	
I _{OZ}	High Impedance Output Leakage Current	5.5	V _I = V _{IH} or V _{IL} V _O = V _{CC} or GND			± 0.5		± 5	μA	
I _{CCT}	Max I _{CC} /Input	5.5	V _I = V _{CC} - 2.1V			0.5		1	mA	
I _{CC}	Quiescent Supply Current	5.5	V _I = V _{CC} or GND			8		80	μA	
I _{OLD}	Dynamic Output Current (note 1, 2)	5.5	V _{OLD} = 1.65 V max					75	mA	
I _{OHD}			V _{OHD} = 3.85 V min					-75	mA	

1) Maximum test duration 2ms, one output loaded at time

2) Incident wave switching is guaranteed on transmission lines with impedances as low as 50Ω

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, R_L = 500 Ω, Input t_r = t_f = 3ns)

Symbol	Parameter	Test Condition		Value					Unit	
		V _{CC} (V)		T _A = 25 °C			-40 to 85 °C			
				Min.	Typ.	Max.	Min.	Max.		
t _{PLH}	Propagation Delay Time	5.0 ^(*)							ns	
t _{PHL}										
t _{PZL}	Output Enable Time	5.0 ^(*)							ns	
t _{PZH}										
t _{PLZ}	Output Disable Time	5.0 ^(*)							ns	
t _{PHZ}										

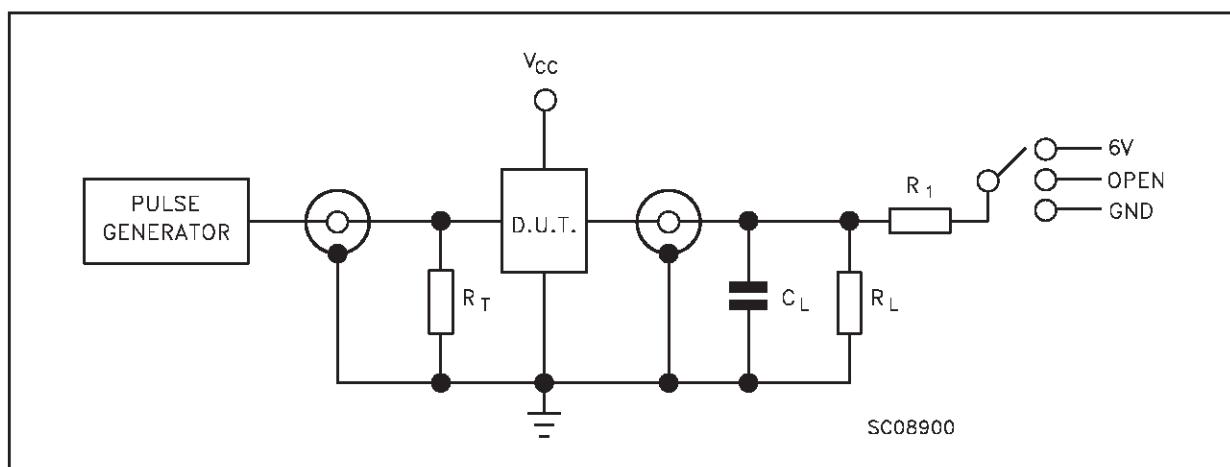
(*) Voltage range is 5.0V ± 0.5V

CAPACITANCE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value					Unit	
		V_{CC} (V)		$T_A = 25^\circ C$			$-40 \text{ to } 85^\circ C$			
				Min.	Typ.	Max.	Min.	Max.		
C_{IN}	Input Capacitance	5.0							pF	
C_{OUT}	Output Capacitance	5.0							pF	
C_{PD}	Power Dissipation Capacitance (note 1)	5.0							pF	

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average current can be obtained by the following equation. $I_{CC(\text{opr})} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/16$ (per circuit)

TEST CIRCUIT



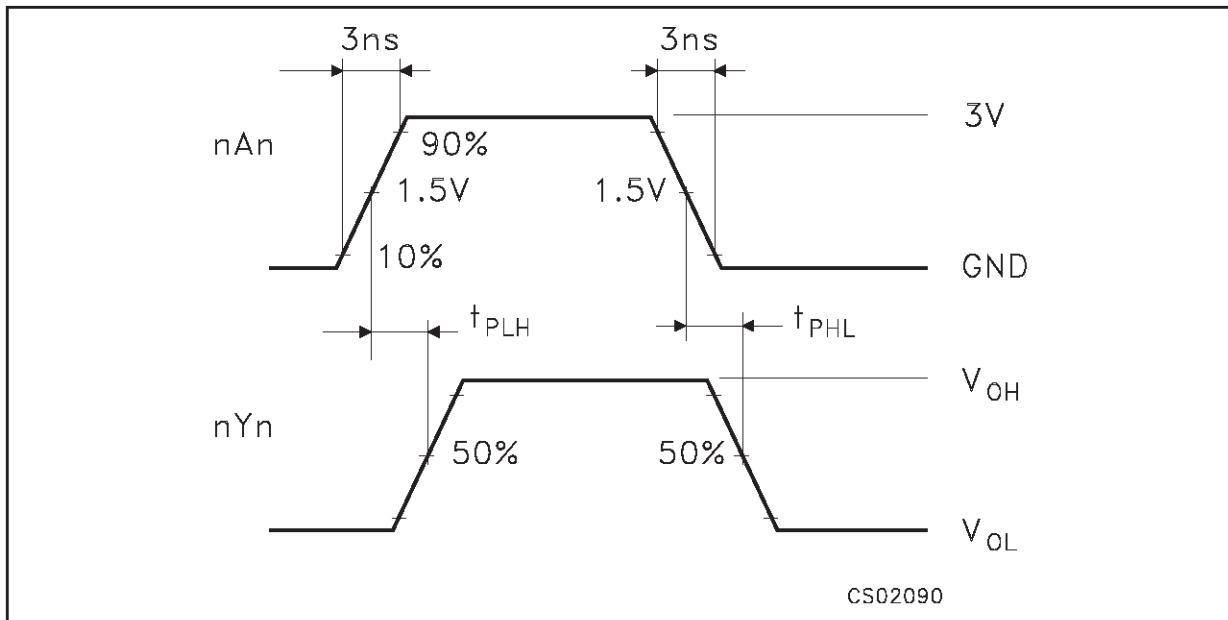
Test	Switch
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	$2V_{CC}$
t_{PZH}, t_{PHZ}	GND

$C_L = 50\text{pF}$ or equivalent (includes jig and probe capacitance)

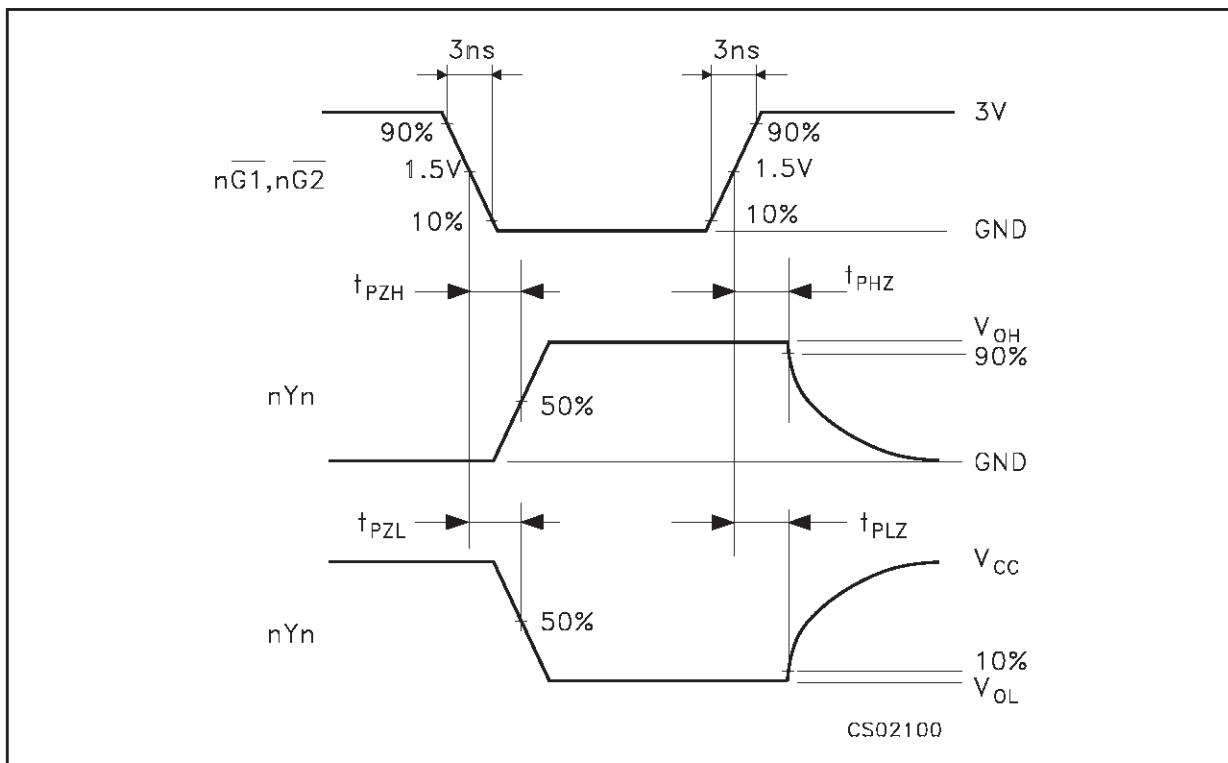
$R_L = R_1 = 500\Omega$ or equivalent

$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

WAVEFORM 1: PROPAGATION DELAYS (f=1MHz; 50% duty cycle)

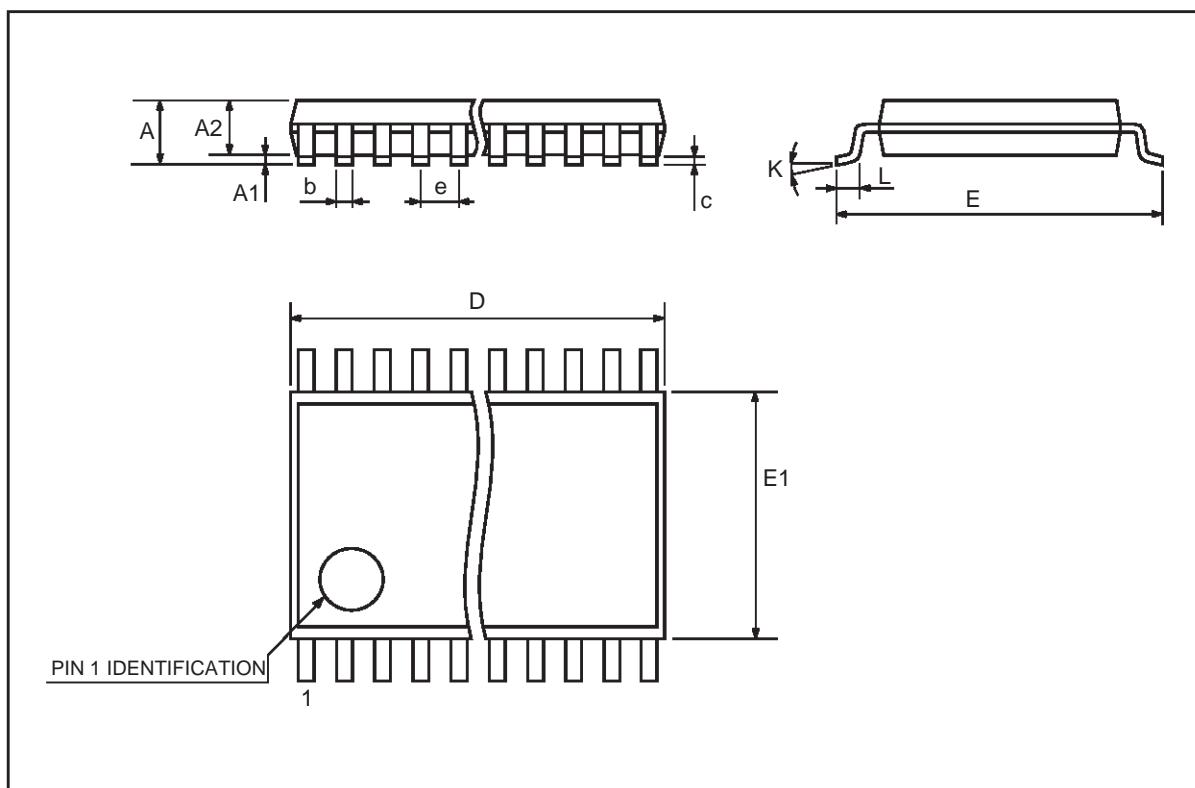


WAVEFORM 2: OUTPUT ENABLE AND DISABLE TIMES (f=1MHz; 50% duty cycle)



TSSOP48 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.1			0.433
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.85	0.9	0.95	0.335	0.354	0.374
b	0.17		0.27	0.0067		0.011
c	0.09		0.20	0.0035		0.0079
D	12.4	12.5	12.6	0.408	0.492	0.496
E	7.95	8.1	8.25	0.313	0.319	0.325
E1	6.0	6.1	6.2	0.236	0.240	0.244
e		0.5 BSC			0.0197 BSC	
K	0°	4°	8°	0°	4°	8°
L	0.50	0.60	0.70	0.020	0.024	0.028



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