



STB160NF02L

N-CHANNEL 20V - 0.0018 Ω - 160A D²PAK

STripFET™ POWER MOSFET

TARGET DATA

TYPE	V _{DS}	R _{DS(on)}	I _D
STB160NF02L	20 V	<0.0027 Ω	160 A

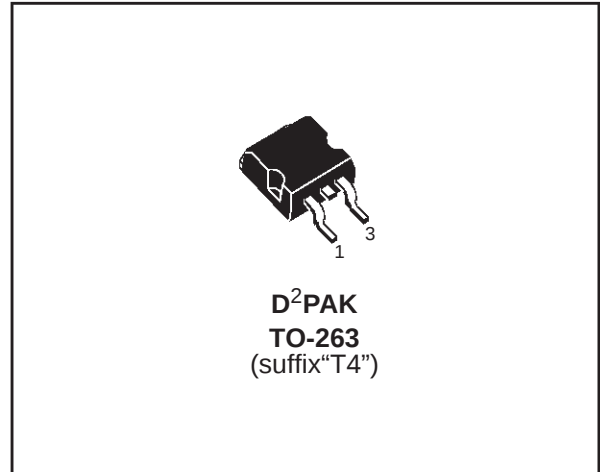
- TYPICAL R_{DS(on)} = 0.0018 Ω
- LOW THRESHOLD DRIVE
- 100% AVALANCHE TESTED
- LOGIC LEVEL DEVICE
- FOR THROUGH-HOLE VERSION CONTACT SALES OFFICE

DESCRIPTION

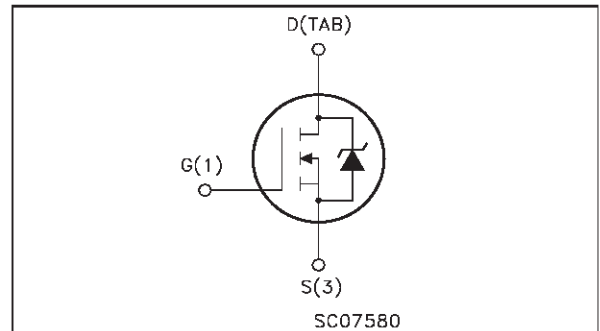
This Power Mosfet is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- MOTOR CONTROL, AUDIO AMPLIFIERS
- DC-DC & DC-AC CONVERTERS
- SOLENOID AND RELAY DRIVERS



INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	20	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 k Ω)	20	V
V _{GS}	Gate- source Voltage	±15	V
I _D	Drain Current (continuous) at T _C = 25°C	160	A
I _D	Drain Current (continuous) at T _C = 100°C	113	A
I _{DM} (•)	Drain Current (pulsed)	640	A
P _{tot}	Total Dissipation at T _C = 25°C	210	W
	Derating Factor	1.43	W/°C
E _{AS} (1)	Single Pulse Avalanche Energy	1.2	J
T _{stg}	Storage Temperature	-60 to 175	°C
T _j	Max. Operating Junction Temperature	175	°C

(•) Pulse width limited by safe operating area.

(1) Starting T_J = 25 °C, I_D = 80A, V_{DD} = 50V

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THERMAL DATA

$R_{thj-case}$	Thermal Resistance Junction-case Max	Max	0.7	°C/W
$R_{thj-amb}$	Thermal Resistance Junction-ambient Max	Max	62.5	°C/W
$R_{thc-sink}$	Thermal Resistance Case-sink Typ	Max	0.1	°C/W
T_j	Maximum Lead Temperature For Soldering Purpose		300	°C

ELECTRICAL CHARACTERISTICS ($T_{case} = 25\text{ °C}$ unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ $V_{GS} = 0$	20			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}, T_C = 125\text{ °C}$			1 10	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 15\text{ V}$			± 100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ $I_D = 250\text{ }\mu\text{A}$	1			V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10\text{ V}$ $I_D = 80\text{ A}$ $V_{GS} = 5\text{ V}$ $I_D = 40\text{ A}$		0.0018 0.0038	0.0027 0.0064	Ω Ω
$I_{D(on)}$	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $V_{GS} = 10\text{ V}$	160			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $I_D = 15\text{ A}$		50		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitances	$V_{DS} = 15\text{ V}$ $f = 1\text{ MHz}$ $V_{GS} = 0$		5200 3100 460		pF pF pF

ELECTRICAL CHARACTERISTICS (continued)**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	$V_{DD} = 10\text{ V}$ $I_D = 80\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 4.5\text{ V}$ (see test circuit, Figure 3)		TBD TBD		ns ns
Q_g	Total Gate Charge	$V_{DD} = 16\text{ V}$ $I_D = 160\text{ A}$ $V_{GS} = 4.5\text{ V}$		TBD		nC
Q_{gs}	Gate-Source Charge			TBD		nC
Q_{gd}	Gate-Drain Charge			TBD		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	$V_{DD} = 10\text{ V}$ $I_D = 80\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 4.5\text{ V}$ (Resistive Load, see fig.3)		TBD TBD		ns ns
$t_{d(off)}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	$V_{clamp} = 16\text{ V}$ $I_D = 160\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 4.5\text{ V}$ (Inductive Load, see fig.5)		TBD TBD TBD		ns ns ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				160	A
$I_{SDM} (*)$	Source-drain Current (pulsed)				640	A
$V_{SD} (*)$	Forward On Voltage	$I_{SD} = 160\text{ A}$ $V_{GS} = 0$			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 160\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 15\text{ V}$ $T_J = 150\text{ }^\circ\text{C}$ (see test circuit, Figure 5)		TBD TBD TBD		ns nC A

(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

(•) Pulse width limited by safe operating area.

Fig. 1: Unclamped Inductive Load Test Circuit

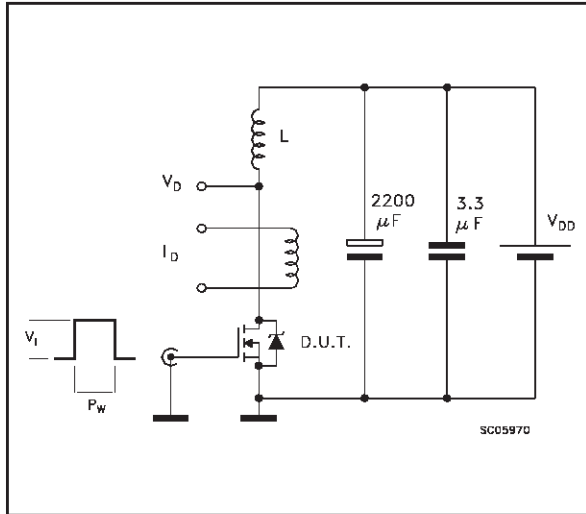


Fig. 2: Unclamped Inductive Waveform

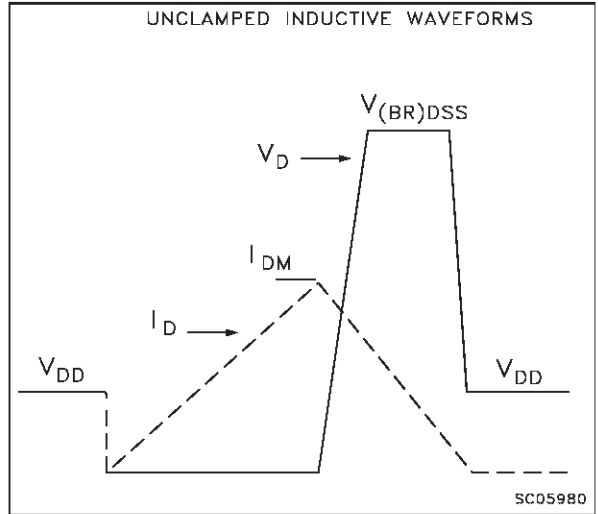


Fig. 3: Switching Times Test Circuits For Resistive Load

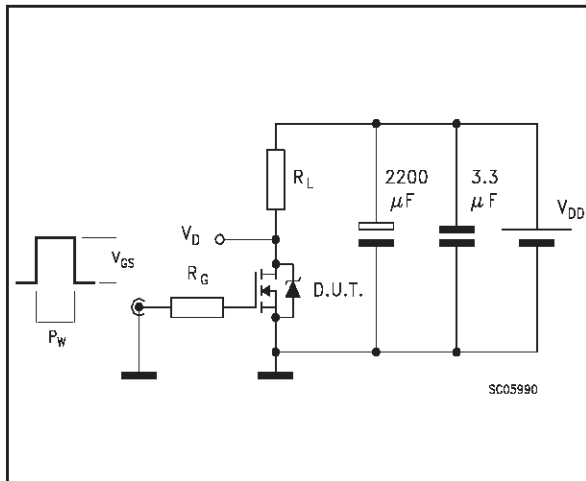


Fig. 4: Gate Charge test Circuit

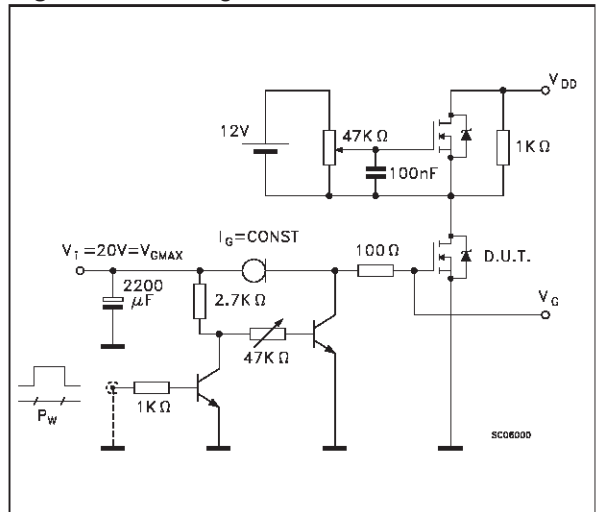
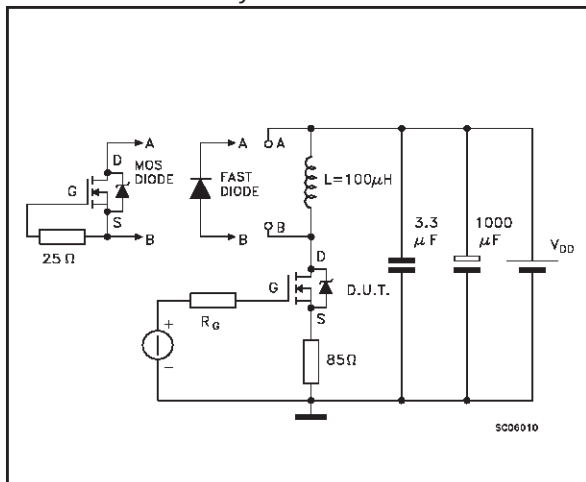
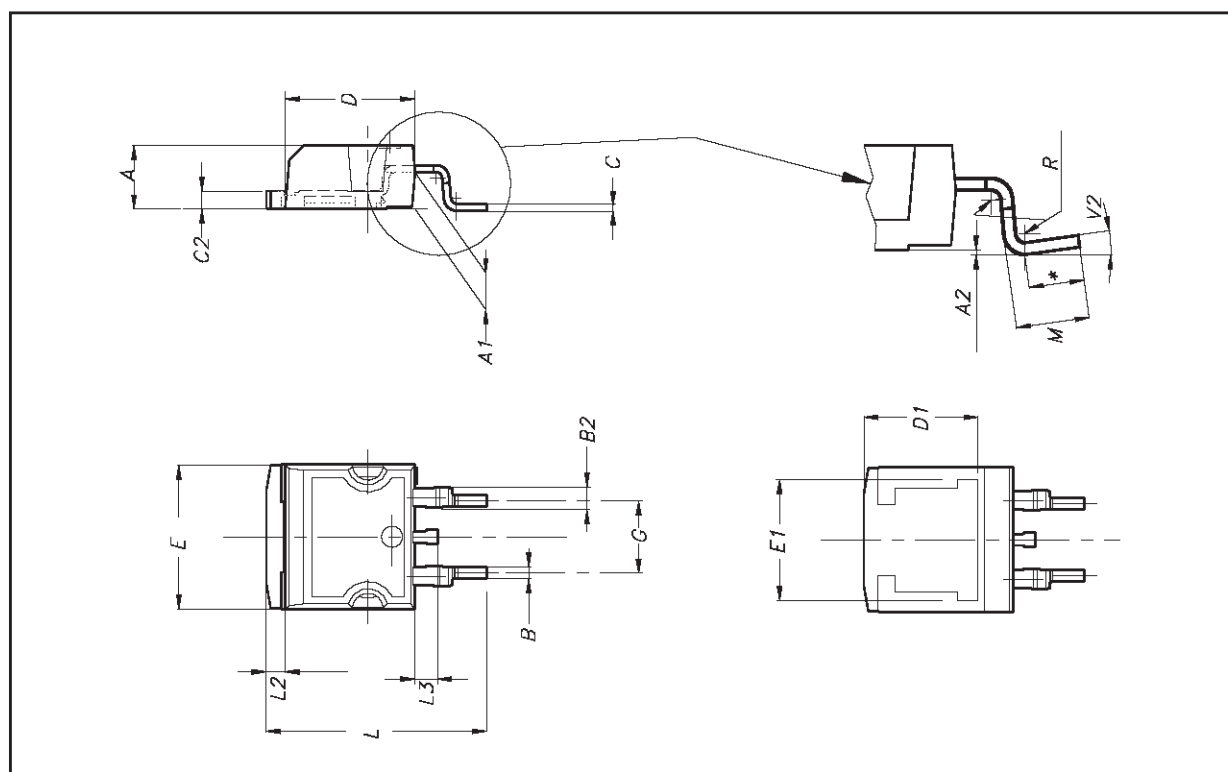


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



D²PAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		8°			



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