74ACT16374

16-BIT D-TYPE FLIP-FLOP
WITH 3-STATE OUTPUTS (NON INVERTED)

- HIGH SPEED:
  f_{MAX} = 270MHz (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION:
  I_{CC} = 8μA(MAX.) at T_A=25°C
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2V (MIN.), V_{IL} = 0.8V (MAX.)
- 50Ω TRANSMISSION LINE DRIVING
  CAPABILITY
- SYMMETRICAL OUTPUT IMPEDANCE:
  $|I_{OH}|$ = I_{OL} = 24mA (MIN)
- OPERATING VOLTAGE RANGE:
  V_{CC} (OPR) = 4.5V to 5.5V
- IMPROVED LATCH-UP IMMUNITY

DESCRIPTION

The ACT16374 is an advanced high-speed CMOS 16-BIT D-TYPE FLIP-FLOP (3-STATE) fabricated with sub-micron silicon gate and double-layer metal wiring C^{2}MOS tecnology.

This 16 bit D-Type Flip-Flop is controlled by two clock inputs (CK) and two output enable inputs ($\overline{OE}$). The device can be used as two 8-bit flip-flops or one 16-bit flip-flop.

On the positive transition of the clock, the Q outputs will be set to the logic state that were setup at the D inputs.

While the ($\overline{OE}$) input is low, the outputs will be in a normal logic state (high or low logic level) and while high level the outputs will be in a high impedance state.

The output control does not affect the internal operation of flip-flops; that is, the old data can be retained or the new data can be entered even while the outputs are off.
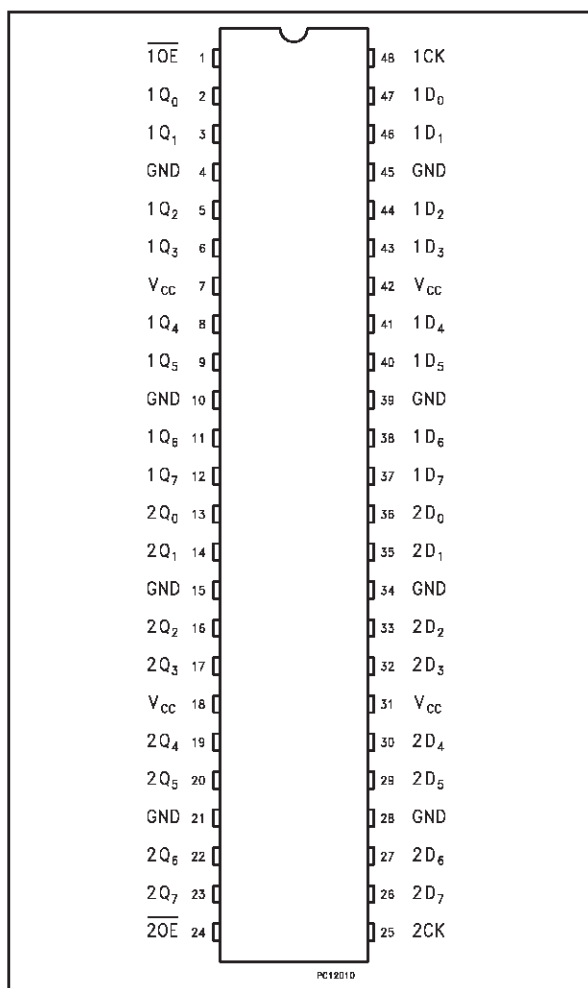
All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.
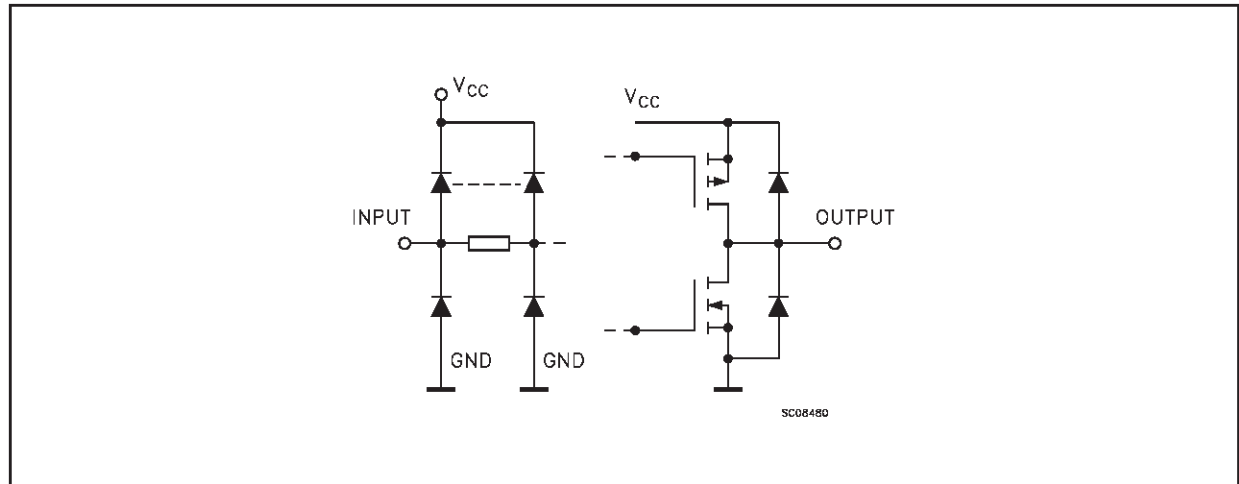

TSSOP

ORDER CODES

PACKAGE	TUBE	T & R
TSSOP		74ACT16374TTR

PIN CONNECTION

$\overline{1OE}$	1	48	1CK
$1Q_0$	2	47	$1D_0$
$1Q_1$	3	46	$1D_1$
GND	4	45	GND
$1Q_2$	5	44	$1D_2$
$1Q_3$	6	43	$1D_3$
V_{CC}	7	42	V_{CC}
$1Q_4$	8	41	$1D_4$
$1Q_5$	9	40	$1D_5$
GND	10	39	GND
$1Q_6$	11	38	$1D_6$
$1Q_7$	12	37	$1D_7$
$2Q_0$	13	36	$2D_0$
$2Q_1$	14	35	$2D_1$
GND	15	34	GND
$2Q_2$	16	33	$2D_2$
$2Q_3$	17	32	$2D_3$
V_{CC}	18	31	V_{CC}
$2Q_4$	19	30	$2D_4$
$2Q_5$	20	29	$2D_5$
GND	21	28	GND
$2Q_6$	22	27	$2D_6$
$2Q_7$	23	26	$2D_7$
$\overline{2OE}$	24	25	2CK

PC12010

INPUT AND OUTPUT EQUIVALENT CIRCUIT

SC08480

PIN DESCRIPTION

| PIN No	SYMBOL	NAME AND FUNCTION
1	1$\overline{OE}$	3 State Output Enable Input (Active LOW)
2, 3, 5, 6, 8, 9, 11, 12	1Q0 to 1Q7	3-State Outputs
13, 14, 16, 17, 19, 20, 22, 23	2Q0 to 2Q7	3-State Outputs
24	2$\overline{OE}$	3 State Output Enable Input (Active LOW)
25	2CK	Clock Input (LOW-to-HIGH Edge Trigger)
36, 35, 33, 32, 30, 29, 27, 26	2D0 to 2D7	Data Inputs
47, 46, 44, 43, 41, 40, 38, 37	1D0 to 1D7	Data Inputs
48	1CK	Clock Input (LOW-to-HIGH Edge Trigger)
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V$_{CC}$	Positive Supply Voltage

TRUTH TABLE

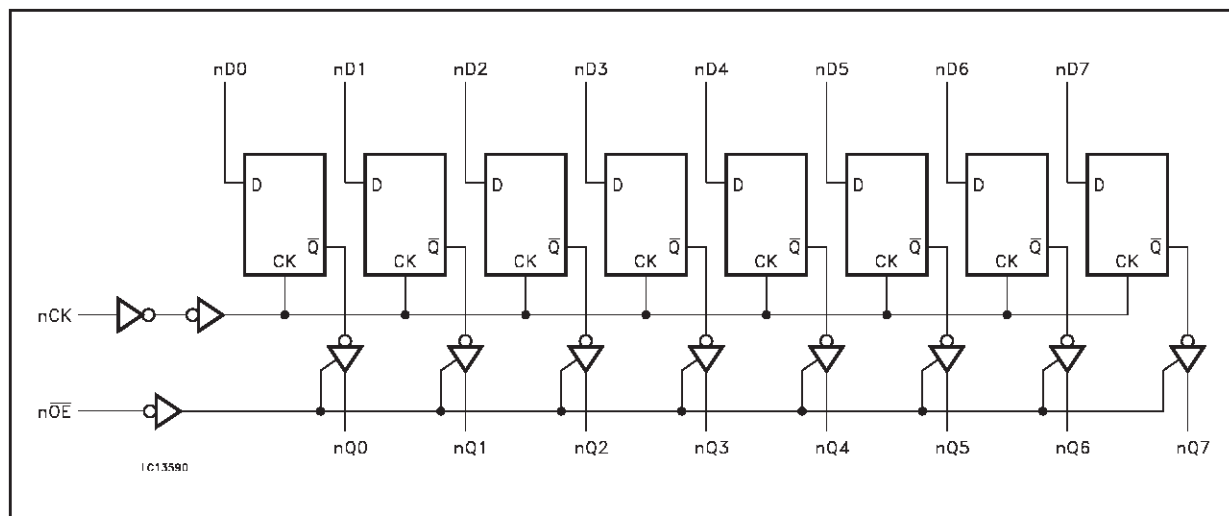| INPUTS			OUTPUTS
$\overline{OE}$	CK	D	Q
H	X	X	Z
L	⎍	X	NO CHANGE*
L	⎍	L	L
L	⎍	H	H

X: "H" or "L"
Z: High Impedance
* Q outputs are latched at the time when the LE input is taken low logic level.

IEC LOGIC SYMBOLS

LC13581
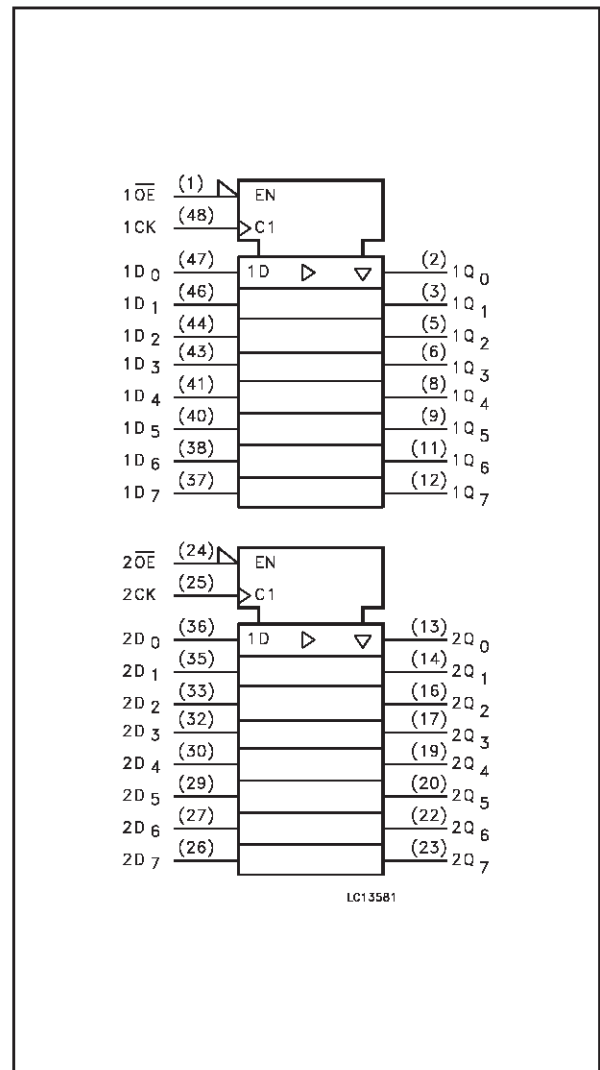
LOGIC DIAGRAM

This logic diagram has not to be used to estimate propagation delays

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 400	mA
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature	-40 to 85	°C
dt/dv	Input Rise and Fall Time V_{CC} = 4.5 to 5.5V (note 1)	8	ns/V

1) V_{IN} from 0.8V to 2.0V

DC SPECIFICATION

Symbol	Parameter	Test Condition V_{CC} (V)	Test Condition	Value T_A = 25 °C Min.	Typ.	Max.	-40 to 85 °C Min.	Max.	Unit
V_{IH}	High Level Input Voltage	4.5	V_O = 0.1 V or V_{CC}-0.1V	2.0			2.0		V
		5.5		2.0			2.0		
V_{IL}	Low Level Input Voltage	4.5	V_O = 0.1 V or V_{CC}-0.1V			0.8		0.8	V
		5.5				0.8		0.8	
V_{OH}	High Level Ouput Voltage	4.5	I_O=-50 µA	4.4	4.49		4.4		V
		5.5	I_O=-50 µA	5.4	5.49		5.4		
		4.5	I_O=-24 mA	3.94			3.8		
		5.5	I_O=-24 mA	4.94			4.8		
V_{OL}	Low Level Output Voltage	4.5	I_O=50 µA		0.001	0.1		0.1	V
		5.5	I_O=50 µA		0.001	0.1		0.1	
		4.5	I_O=24 mA			0.36		0.44	
		5.5	I_O=24 mA			0.36		0.44	
I_I	Input Leakage Current	5.5	V_I = V_{CC} or GND			± 0.1		± 1	µA
I_{OZ}	High Impedance Output Leakage Current	5.5	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND			± 0.5		± 5	µA
I_{CCT}	Max I_{CC}/Input	5.5	V_I = V_{CC} - 2.1V			0.5		1	mA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND			8		80	µA
I_{OLD}	Dynamic Output Current (note 1, 2)	5.5	V_{OLD} = 1.65 V max					75	mA
I_{OHD}			V_{OHD} = 3.85 V min					-75	mA

1) Maximum test duration 2ms, one output loaded at time
2) Incident wave switching is guaranteed on transmission lines with impedances as low as 50Ω

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, R_L = 500 Ω, Input t_r = t_f = 3ns)

| Symbol	Parameter	Test Condition		Value					Unit
		V_{CC} (V)		T_A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay Time CK to Q	5.0(*)			4.3	6.3		7.6	ns
t_{PHL}					4.5	6.7		8.1	
t_{PZL}	Output Enable Time	5.0(*)			5.7	8.5		10.3	ns
t_{PZH}					4.8	7.2		9.0	
t_{PLZ}	Output Disable Time	5.0(*)			5.5	8.0		9.1	ns
t_{PHZ}					4.7	6.7		8.1	
t_W	CLOCK Pulse Width HIGH or LOW	5.0(*)		2.5	1.9		2.9		ns
t_s	Setup Time D to CK, HIGH or LOW	5.0(*)		1.6	<1.0		1.8		ns
t_h	Hold Time D to CK, HIGH or LOW	5.0(*)		0.3	-0.8		1.0		ns
f_{MAX}	Maximum Clock Frequency	5.0(*)		100	120		60		MHz

(*) Voltage range is 5.0V $\pm$ 0.5V

CAPACITANCE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value					Unit
		V_{CC} (V)		T_A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
C_{IN}	Input Capacitance	5.0			3.6				pF
C_{OUT}	Output Capacitance	5.0			11				pF
C_{PD}	Power Dissipation Capacitance (note 1)	5.0			25				pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/16$ (per circuit)
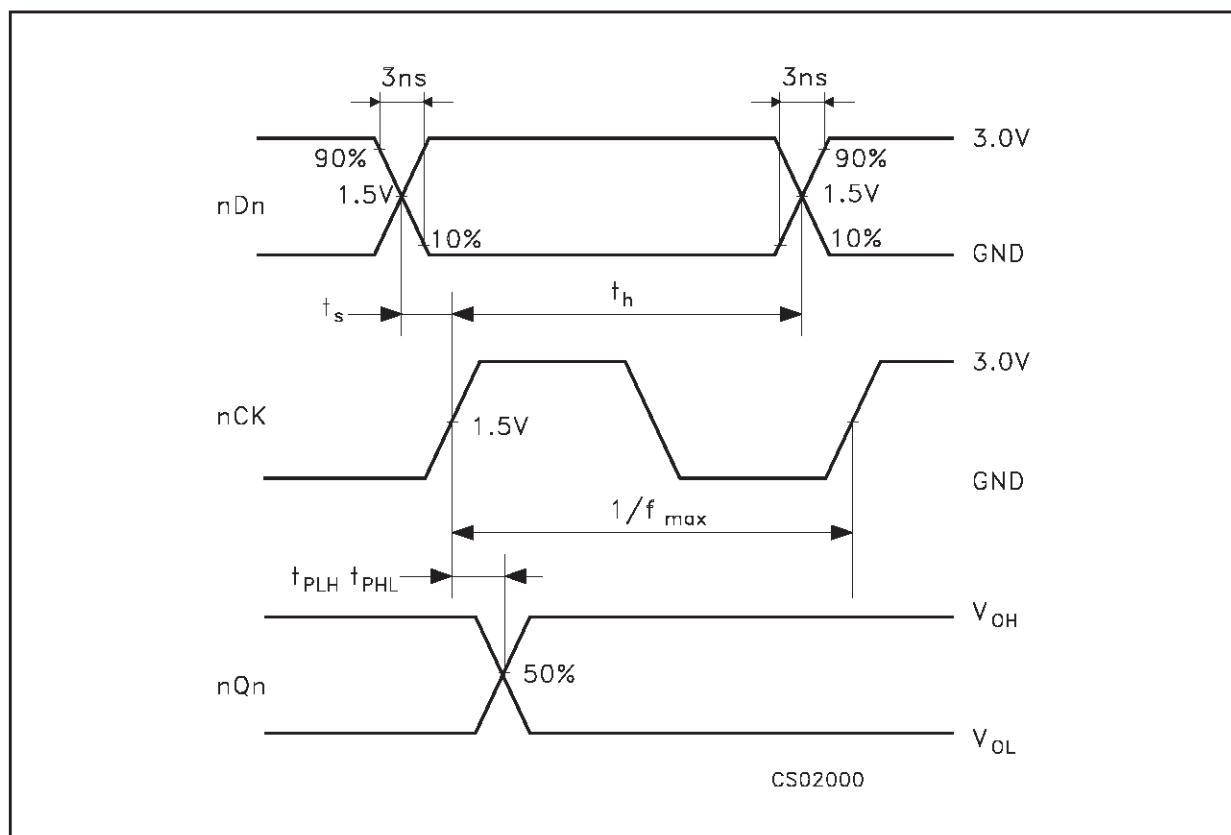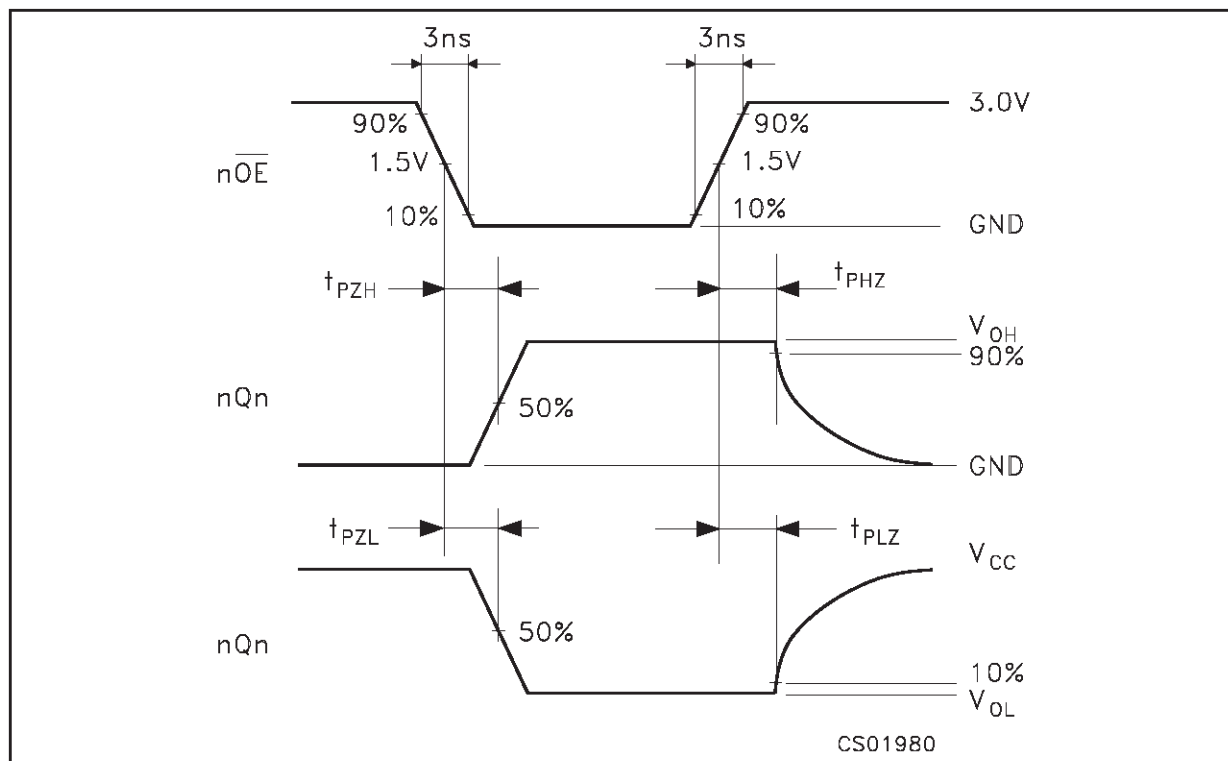
TEST CIRCUIT

SC08900
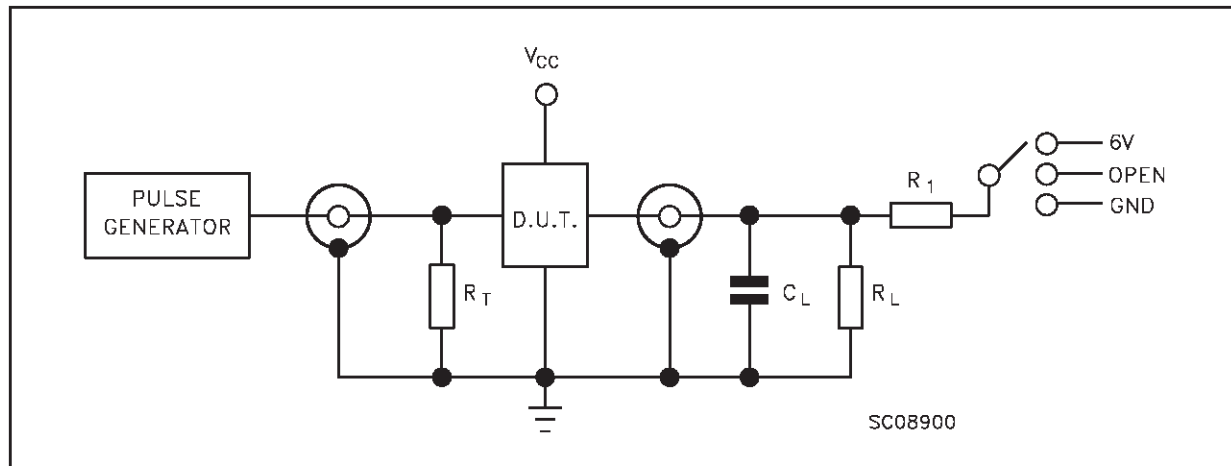
Test	Switch
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	$2V_{CC}$
t_{PZH}, t_{PHZ}	GND

C_L = 50pF or equivalent (includes jig and probe capacitance)
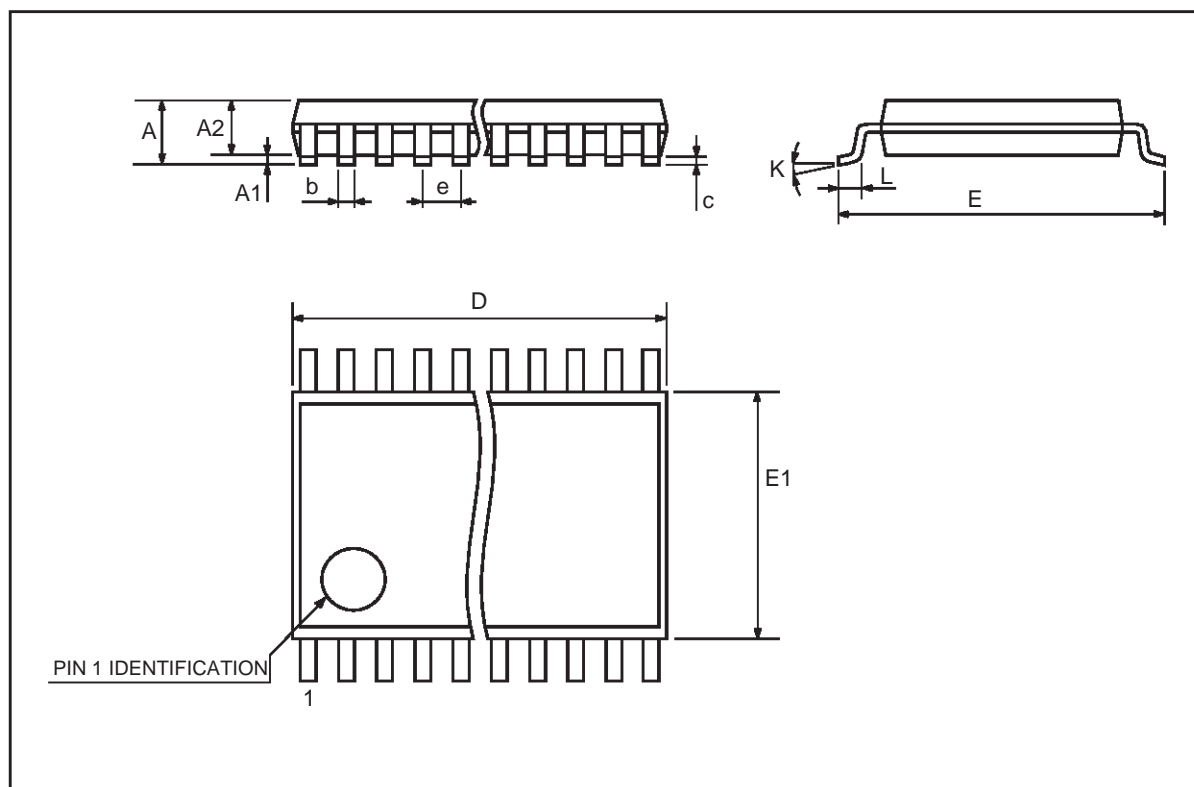$R_L = R_1 = 500\Omega$ or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

WAVEFORM 1: PROPAGATION DELAYS, SETUP AND HOLD TIMES (f=1MHz; 50% duty cycle)

CS02000

WAVEFORM 2: OUTPUT ENABLE AND DISABLE TIMES (f=1MHz; 50% duty cycle)

CS01980

WAVEFORM 3: CLOCK PULSE WIDTHS (f=1MHz; 50% duty cycle)

CS02010
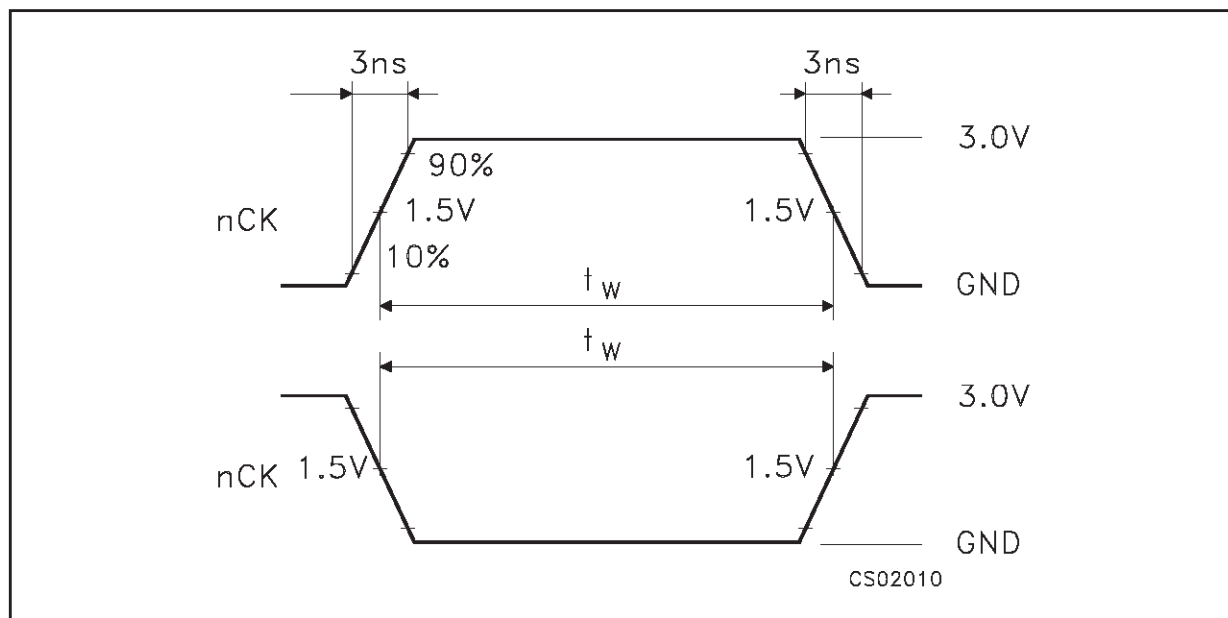
TSSOP48 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.1			0.433
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.85	0.9	0.95	0.335	0.354	0.374
b	0.17		0.27	0.0067		0.011
c	0.09		0.20	0.0035		0.0079
D	12.4	12.5	12.6	0.408	0.492	0.496
E	7.95	8.1	8.25	0.313	0.319	0.325
E1	6.0	6.1	6.2	0.236	0.240	0.244
e		0.5 BSC			0.0197 BSC	
K	0°	4°	8°	0°	4°	8°
L	0.50	0.60	0.70	0.020	0.024	0.028

PIN 1 IDENTIFICATION