



STT3PF30L

P-CHANNEL 30V - 0.13Ω - 3A SOT23-6L

STripFET™ II POWER MOSFET

PRELIMINARY DATA

TYPE	V _{DS}	R _{DS(on)}	I _D
STT3PF30L	30 V	<0.165 Ω	3 A

- TYPICAL R_{DS(on)} = 0.13 Ω
- STANDARD OUTLINE FOR EASY AUTOMATED SURFACE MOUNT ASSEMBLY
- LOW THRESHOLD DRIVE

DESCRIPTION

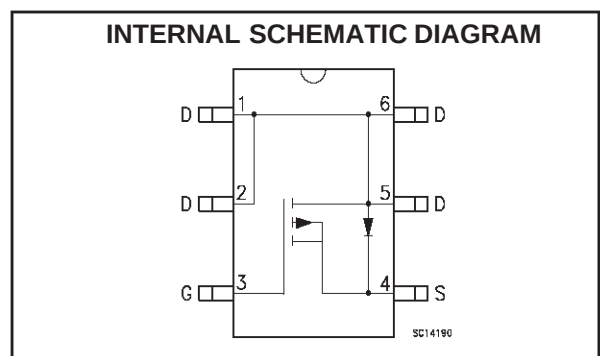
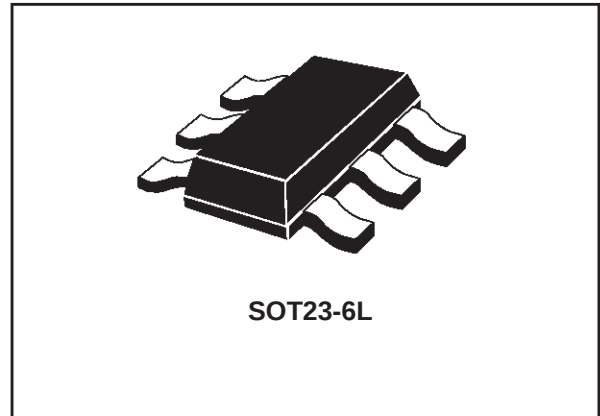
This Power Mosfet is the latest development of ST-Microelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

APPLICATIONS

- DC MOTOR DRIVE
- DC-DC CONVERTERS
- BATTERY MANAGEMENT IN NOMADIC EQUIPMENT
- POWER MANAGEMENT IN PORTABLE/DESKTOP PCs
- CELLULAR

MARKING

- STA3



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	30	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	30	V
V _{GS}	Gate- source Voltage	± 20	V
I _D	Drain Current (continuous) at T _C = 25°C	3	A
I _D	Drain Current (continuous) at T _C = 100°C	1.9	A
I _{DM} (●)	Drain Current (pulsed)	12	A
P _{TOT}	Total Dissipation at T _C = 25°C	1.6	W

(●) Pulse width limited by safe operating area

Note: For the P-CHANNEL MOSFET actual polarity of voltages and current has to be reversed

STT3PF30L

THERMAL DATA

Rthj-amb	(*) Thermal Resistance Junction-ambient Max	78	°C/W
Rthj-amb	(**) Thermal Resistance Junction-ambient Max	156	°C/W
T _j	Max. Operating Junction Temperature	150	°C
T _{stg}	Storage Temperature	–55 to 150	°C

(*) Mounted on a 1in² pad of 2oz Cu in FR-4 board

(**) Mounted on a minimum pad of 2oz Cu in FR-4 board

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0	30			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125 °C			1 10	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 20 V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	1	1.7	2.5	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10 V, I _D = 1.5 A V _{GS} = 4.5 V, I _D = 1.5 A		0.13 0.15	0.165 0.2	Ω Ω
I _{D(on)}	On State Drain Current	V _{DS} > I _{D(on)} × R _{DS(on)} max, V _{GS} = 10 V	3			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (1)	Forward Transconductance	V _{DS} > I _{D(on)} × R _{DS(on)} max, I _D = 1.5 A		3.5		S
C _{iss}	Input Capacitance	V _{DS} = 25 V, f = 1 MHz, V _{GS} = 0		510		pF
C _{oss}	Output Capacitance			170		pF
C _{rss}	Reverse Transfer Capacitance			55		pF

ELECTRICAL CHARACTERISTICS (CONTINUED)**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 15V, I_D = 1.5 A$		15		ns
t_r	Rise Time	$R_G = 4.7\Omega, V_{GS} = 4.5 V$ (see test circuit, Figure 3)		37		ns
Q_g	Total Gate Charge	$V_{DD} = 24 V, I_D = 3 A,$		5.5	7.5	nC
Q_{gs}	Gate-Source Charge	$V_{GS} = 5 V$		1.7		nC
Q_{gd}	Gate-Drain Charge			1.8		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off-Delay Time	$V_{DD} = 15 V, I_D = 1.5 A,$		15		ns
t_f	Fall Time	$R_G = 4.7\Omega, V_{GS} = 4.5 V$ (see test circuit, Figure 3)		29		ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				3	A
$I_{SDM} (1)$	Source-drain Current (pulsed)				12	A
$V_{SD} (2)$	Forward On Voltage	$I_{SD} = 3 A, V_{GS} = 0$			1.2	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 3, di/dt = 100A/\mu s,$ $V_{DD} = 15 V, T_j = 150^\circ C$ (see test circuit, Figure 5)		18.3		ns
Q_{rr}	Reverse Recovery Charge			12.35		nC
I_{RRM}	Reverse Recovery Current			1.33		A

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

Fig. 1: Unclamped Inductive Load Test Circuit

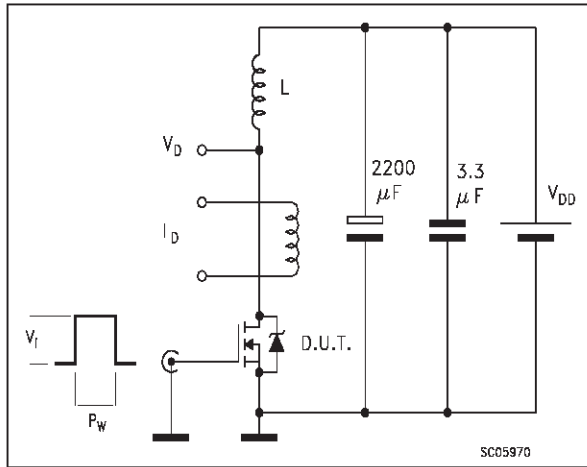


Fig. 2: Unclamped Inductive Waveform

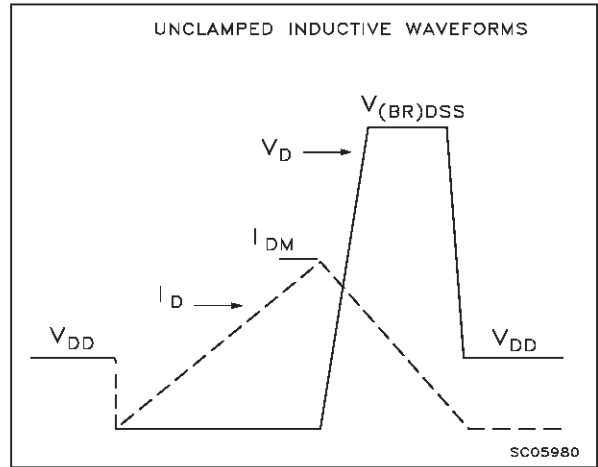


Fig. 3: Switching Times Test Circuit For Resistive Load

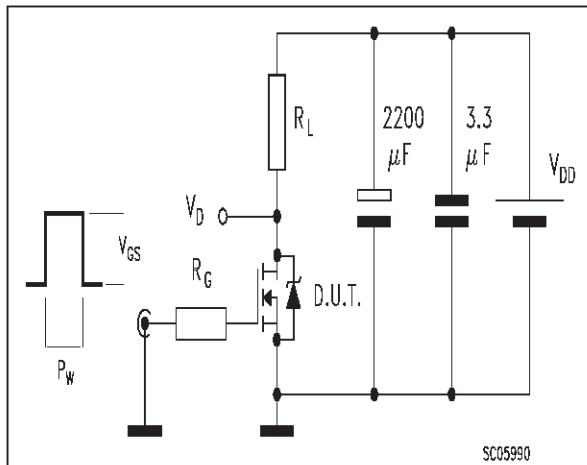


Fig. 4: Gate Charge test Circuit

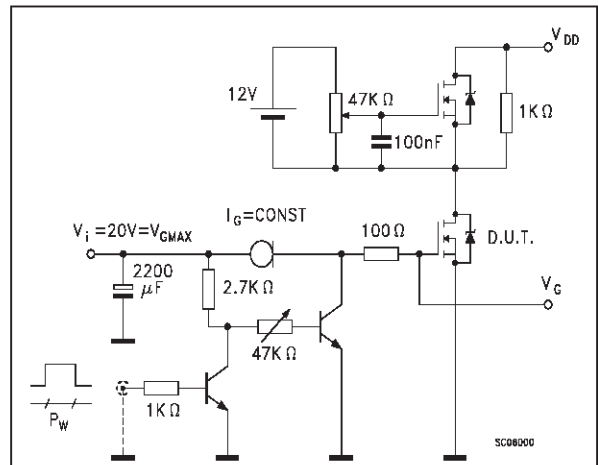
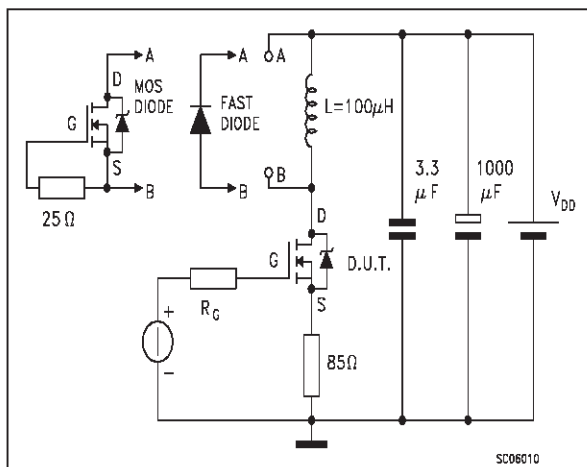
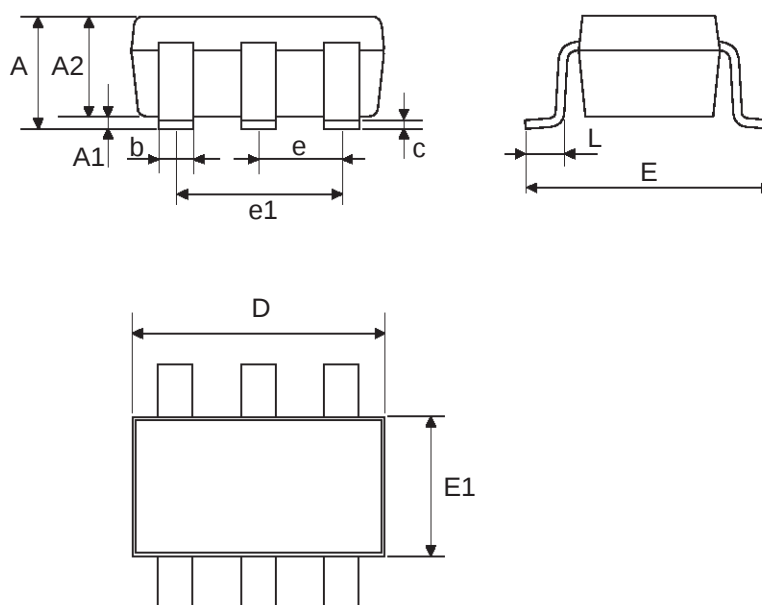


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TSOP-6 MECHANICAL DATA

DIM.	mm			mils		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	0.90		1.45	0.035		0.057
A1	0.00		0.15	0.000		0.006
A2	0.90		1.30	0.035		0.051
b	0.25		0.50	0.010		0.020
C	0.09		0.20	0.004		0.008
D	2.80		3.10	0.110		0.122
E	2.60		3.00	0.102		0.118
E1	1.50		1.75	0.059		0.069
L	0.35		0.55	0.014		0.022
e		0.95			0.037	
e1		1.90			0.075	



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specification mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a trademark of STMicroelectronics

© 2000 STMicroelectronics – Printed in Italy – All Rights Reserved

STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco -
Singapore - Spain - Sweden - Switzerland - United Kingdom - U.S.A.

<http://www.st.com>