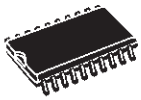
74LVC244A

LOW VOLTAGE CMOS QUAD BUS BUFFERS (3-STATE) ADVANCED PERFORMANCE

PRELIMINARY DATA

- 5V TOLERANT INPUTS
- HIGH SPEED: t_{PD} = 4.2ns (MAX.) at V_{CC} = 3V
- POWER DOWN PROTECTION ON INPUTS AND OUTPUTS
- SYMMETRICAL OUTPUT IMPEDANCE: $|I_{OH}| = I_{OL}$ = 24mA (MIN) at V_{CC} = 3V
- PCI BUS LEVELS GUARANTEED AT 24 mA
- BALANCED PROPAGATION DELAYS: $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE: V_{CC}(OPR) = 1.65V to 3.6V (1.2V Data Retention)
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 244
- LATCH-UP PERFORMANCE EXCEEDS 500mA (JESD 17)
- ESD PERFORMANCE: HBM > 2000V (MIL STD 883 method 3015); MM > 200V



SOP

TSSOP

ORDER CODES

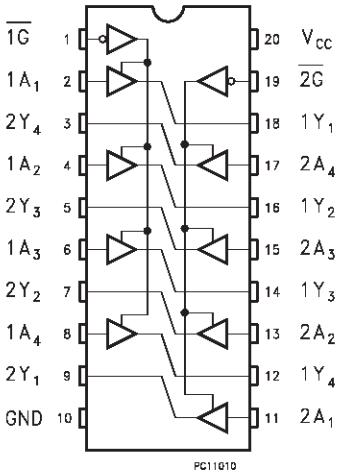
PACKAGE	TUBE	T & R
SOP	74LVC244AM	74LVC244AMTR
TSSOP		74LVC244ATTR

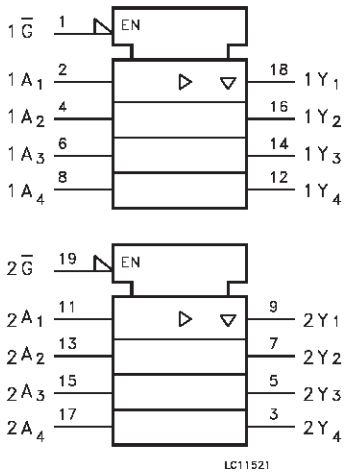
DESCRIPTION

The 74LVC244A is a low voltage CMOS OCTAL BUS BUFFER (3-STATE) fabricated with sub-micron silicon gate and double-layer metal wiring C^2MOS tecnology. It is ideal for 1.65 to 3.6 V_{CC} operations and low power and low noise applications.

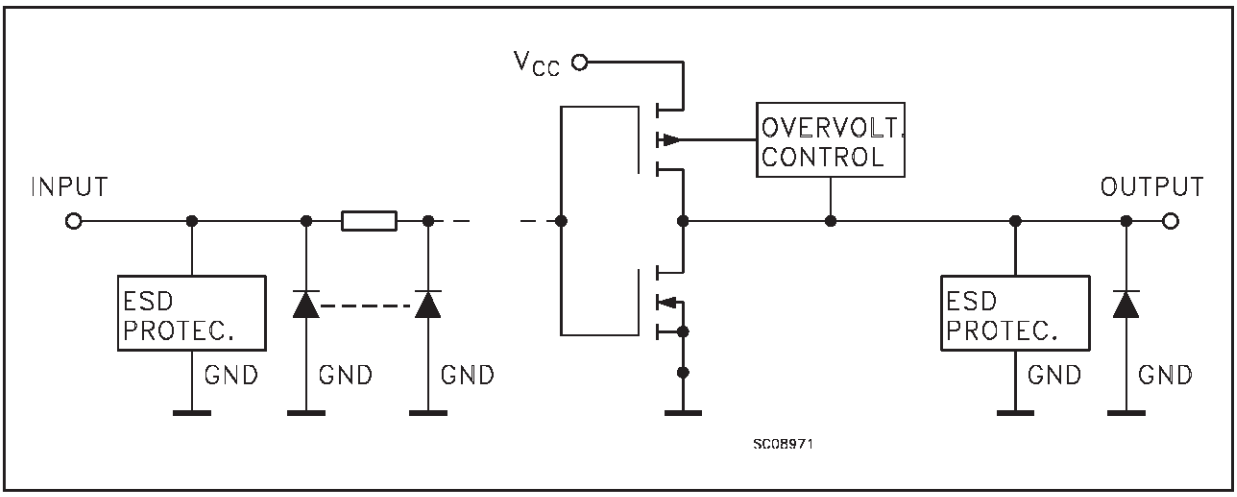
It can be interfaced to 5V signal environment for inputs in mixed 3.3/5V system.
$\overline{G}$ control output governs four BUS BUFFERs.
Thise device is designed to be used with 3 state memory address drivers, etc.
It has more speed performance at 3.3V than 5V AC/ACT family, combined with a lower power consumption.
All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS





INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME QND FUNCTION
1	$\overline{1G}$	Output Enable Input
2, 4, 6, 8	1A1 to 1A4	Data Inputs
9, 7, 5, 3	2Y1 to 2Y4	Data Outputs
11, 13, 15, 17	2A1 to 2A4	Data Inputs
18, 16, 14, 12	1Y1 to 1Y4	Data Outputs
19	$\overline{2G}$	Output Enable Input
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

TRUTH TABLE

INPUTS		OUTPUT
$\overline{G}$	An	Yn
L	L	H
L	H	L
H	X	Z

X=Don't care; Z=High Impedance

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7.0	V
V_I	DC Input Voltage	-0.5 to +7.0	V
V_O	DC Output Voltage (V_{CC} = 0V)	-0.5 to +7.0	V
V_O	DC Output Voltage (High or Low State) (note 1)	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	- 50	mA
I_{OK}	DC Output Diode Current (note 2)	- 50	mA
I_O	DC Output Current	± 50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current per Supply Pin	± 100	mA
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Rating are those value beyond which damage to the device may occour. Functional operation under these condition is not implied

1) I_O absolute maximum rating must be observed

2) V_O < GND, V_O > V_{CC}

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (note 1)	1.65 to 3.6	V
V_I	Input Voltage	0 to 5.5	V
V_O	Output Voltage (V_{CC} = 0V)	0 to 5.5	V
V_O	Output Voltage (High or Low State)	0 to V_{CC}	V
I_{OH}, I_{OL}	High or Low Level Output Current (V_{CC} = 3.0 to 3.6V)	± 24	mA
I_{OH}, I_{OL}	High or Low Level Output Current (V_{CC} = 2.7 to 3.0V)	± 12	mA
I_{OH}, I_{OL}	High or Low Level Output Current (V_{CC} = 2.3 to 2.7V)	± 8	mA
I_{OH}, I_{OL}	High or Low Level Output Current (V_{CC} = 1.65 to 2.3V)	± 4	mA
T_{op}	Operating Temperqture	-40 to 85	°C
dt/dv	Input Rise and Fall Time (note 2)	0 to 10	ns/V

1) Truth Table guaranteed: 1.2V to 3.6V

2) V_{IN} from 0.8V to 2V at V_{CC} = 3.0V

DC SPECIFICATION

Symbol	Parameter	Test Condition		Value		Unit
		V_{CC} (V)		-40 to 85 °C		
				Min.	Max.	
V_{IH}	High Level Input Voltage	1.65 to 1.95		0.65V_{CC}		V
		2.3 to 2.7		1.7		
		2.7 to 3.6		2		
V_{IL}	Low Level Input Voltage	1.65 to 1.95			0.35V_{CC}	V
		2.3 to 2.7			0.7	
		2.7 to 3.6			0.8	
V_{OH}	High Level Ouput Voltage	1.65 to 3.6	I_O=-100 µA	V_{CC}-0.2		V
		1.65	I_O=-4 mA	1.2		
		2.3	I_O=-8 mA	1.7		
		2.7	I_O=-12 mA	2.2		
		3.0	I_O=-18 mA	2.4		
		3.0	I_O=-24 mA	2.2		
V_{OL}	Low Level Output Voltage	1.65 to 3.6	I_O=100 µA		0.2	V
		1.65	I_O=4 mA		0.45	
		2.3	I_O=8 mA		0.7	
		2.7	I_O=12 mA		0.4	
		3.0	I_O=24 mA		0.55	
I_I	Input Leakage Current	3.6	V_I = 0 to 5.5V		± 5	µA
I_{off}	Power Off Leakage Current	0	V_I or V_O = 5.5V		100	µA
I_{OZ}	High Impedance Output Leakage Current	3.6	V_I = V_{IH} orV_{IL} V_O = 0 to 5.5V		± 5	µA
I_{CC}	Quiescent Supply Current	3.6	V_I = V_{CC} or GND		10	µA
			V_I or V_O = 3.6 to 5.5V		± 10	
ΔI_{CC}	I_{CC} incr. per Input	2.7 to 3.6	V_{IH} = V_{CC}-0.6V		500	µA

DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition		Value			Unit
		V_{CC} (V)		T_A = 25 °C			
				Min.	Typ.	Max.	
V_{OLP}	Dynamic Low Level Quiet Output (note 1)	3.3	C_L = 50pF V_{IL} = 0V, V_{IH} = 3.3V		0.8		V
V_{OLV}					-0.8		

1) Number of output defined as "n". Measured with "n-1" outputs switching from HIGH to LOW or LOW to HIGH. The remaining outputs is measured in the LOW state.

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition				Value		Unit
		V_{CC} (V)	C_L (pF)	R_L (Ω)	$t_s = t_r$ (ns)	-40 to 85 °C		
						Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time	1.65 to 1.95	30	1000	2.0		9.0	ns
		2.3 to 2.7	30	500	2.0		7.9	
		2.7	50	500	2.5	1.5	6.9	
		3.0 to 3.6	50	500	2.5	1	5.9	
t_{PZL} t_{PZH}	Output Enable Time	1.65 to 1.95	30	1000	2.0		11	
		2.3 to 2.7	30	500	2.0		9.6	
		2.7	50	500	2.5	1	8.6	
		3.0 to 3.6	50	500	2.5	1	7.6	
t_{PLZ} t_{PHZ}	Output Disable Time	1.65 to 1.95	30	1000	2.0		9.0	
		2.3 to 2.7	30	500	2.0		7.8	
		2.7	50	500	2.5	2	6.8	
		3.0 to 3.6	50	500	2.5	2	6.5	
t_{OSLH} t_{OSHL}	Output To Output Skew Time (note1, 2)	2.7 to 3.6					1	ns

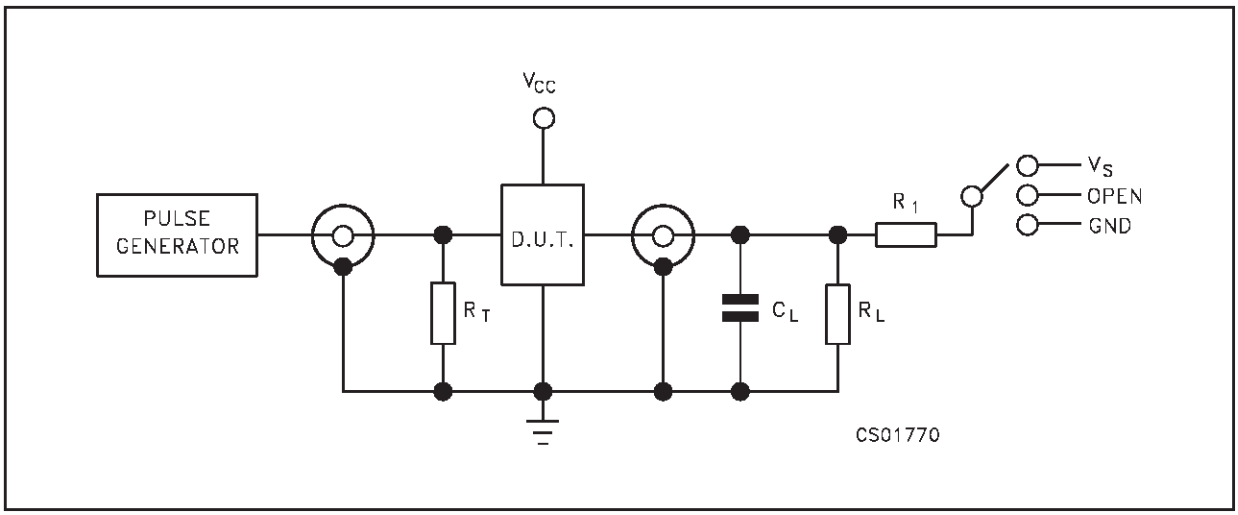
1) Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW ($t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$
2) Parameter guaranteed by design

CAPACITANCE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value			Unit
		V_{CC} (V)		T_A = 25 °C			
				Min.	Typ.	Max.	
C_{IN}	Input Capacitance				4		pF
C_{PD}	Power Dissipation Capacitance (note 1)	1.8	f_{IN} = 10MHz		28		pF
		2.5			30		
		3.3			34		

1) C_{PD} is defined as the value of the IC's internal equivqlent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average current cqn be obtqined by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/n$ (per circuit)

TEST CIRCUIT

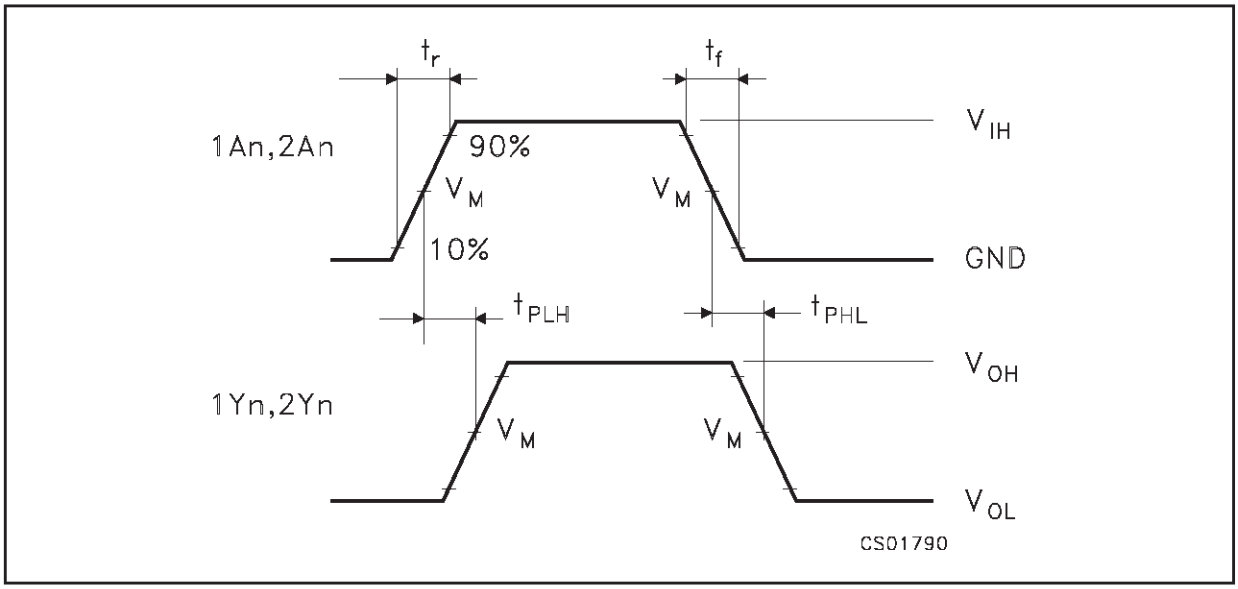


$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

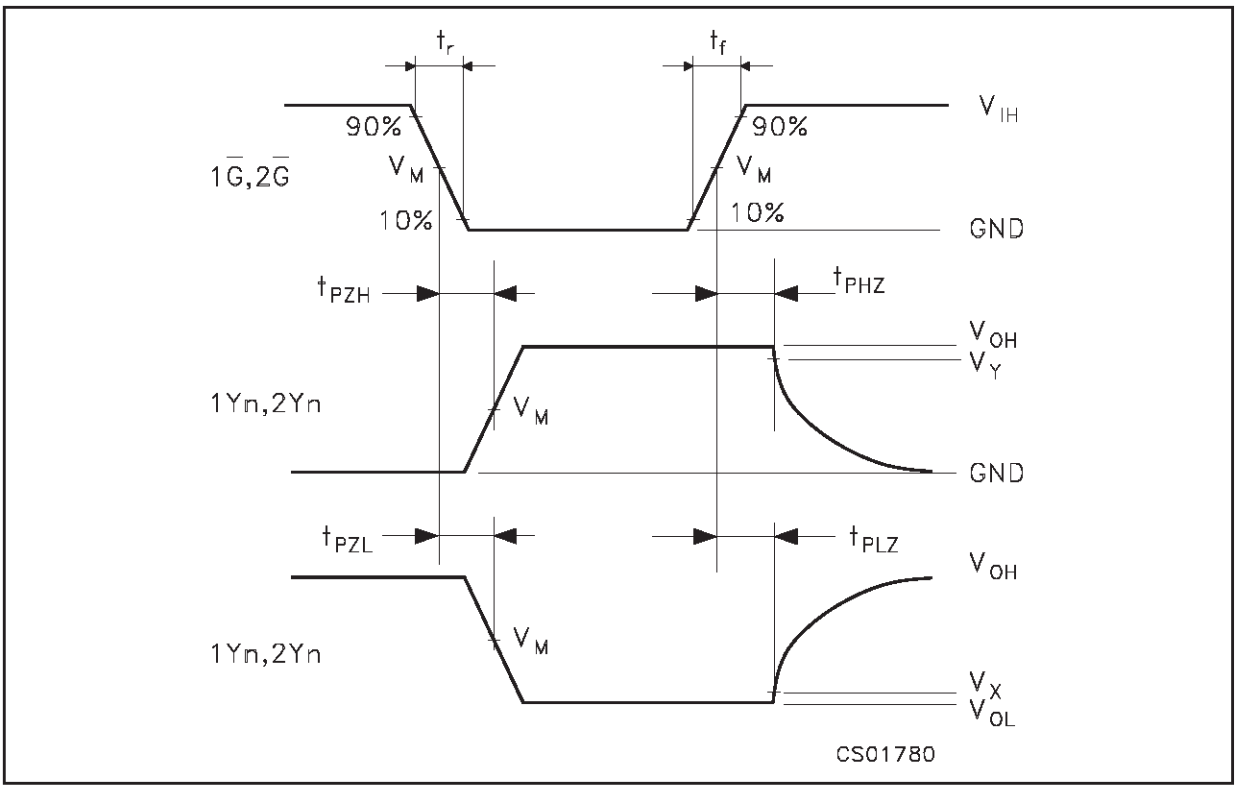
TEST CIRCUIT AND WAVEFORM SYMBOL VALUE

Symbol	V_{CC}			
	1.65 to 1.95V	**2.3 to 2.7V**	**2.7V**	**3.0 to 3.6V**
C_L	30pF	30pF	50pF	50pF
$R_L = R_1$	1000Ω	500Ω	500Ω	500Ω
V_S	2 x V_{CC}	2 x V_{CC}	6V	7V
V_{IH}	V_{CC}	V_{CC}	2.7V	3.0V
V_M	$V_{CC}/2$	$V_{CC}/2$	1.5V	1.5V
V_{OH}	V_{CC}	V_{CC}	3.0V	3.5V
$t_r = t_f$	<2.0ns	<2.0ns	<2.5ns	<2.5ns

WAVEFORM 1: PROPAGATION DELAYS (f=1MHz; 50% duty cycle)

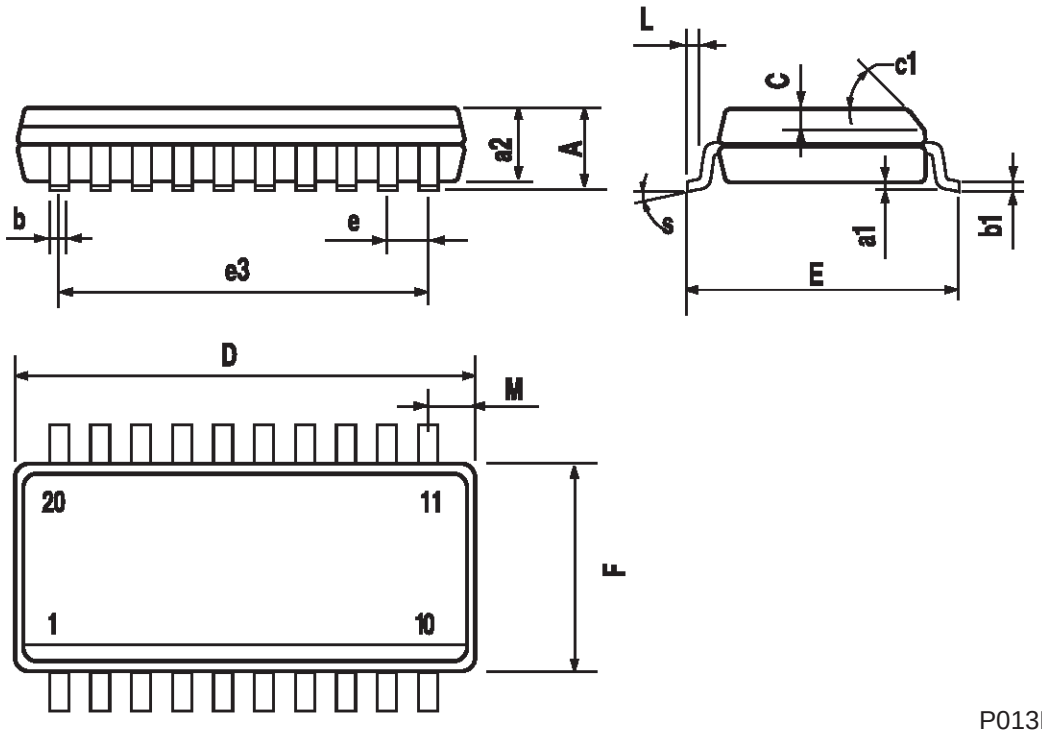


WAVEFORM 2: OUTPUT ENABLE AND DISABLE TIME (f=1MHz; 50% duty cycle)



SO-20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.10		0.20	0.004		0.007
a2			2.45			0.096
b	0.35		0.49	0.013		0.019
b1	0.23		0.32	0.009		0.012
C		0.50			0.020	
c1	45 (typ.)					
D	12.60		13.00	0.496		0.512
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.40		7.60	0.291		0.299
L	0.50		1.27	0.19		0.050
M			0.75			0.029
S	8 (max.)					



P013L

TSSOP20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.1			0.433
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.85	0.9	0.95	0.335	0.354	0.374
b	0.19		0.30	0.0075		0.0118
c	0.09		0.2	0.0035		0.0079
D	6.4	6.5	6.6	0.252	0.256	0.260
E	6.25	6.4	6.5	0.246	0.252	0.256
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0^o	4^o	8^o	0^o	4^o	8^o
L	0.50	0.60	0.70	0.020	0.024	0.028