VND810

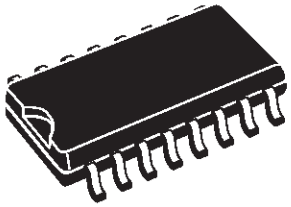
DOUBLE CHANNEL HIGH SIDE DRIVER

PRELIMINARY DATA

TYPE	$R_{DS(on)}$	I_{OUT}	V_{CC}
VND810	160 mΩ (*)	3.5 A (*)	36 V

(*) Per each channel

- CMOS COMPATIBLE INPUTS
- OPEN DRAIN STATUS OUTPUTS
- ON STATE OPEN LOAD DETECTION
- OFF STATE OPEN LOAD DETECTION
- SHORTED LOAD PROTECTION
- UNDERVOLTAGE AND OVERVOLTAGE SHUTDOWN
- PROTECTION AGAINST LOSS OF GROUND
- VERY LOW STAND-BY CURRENT
- REVERSE BATTERY PROTECTION (**)

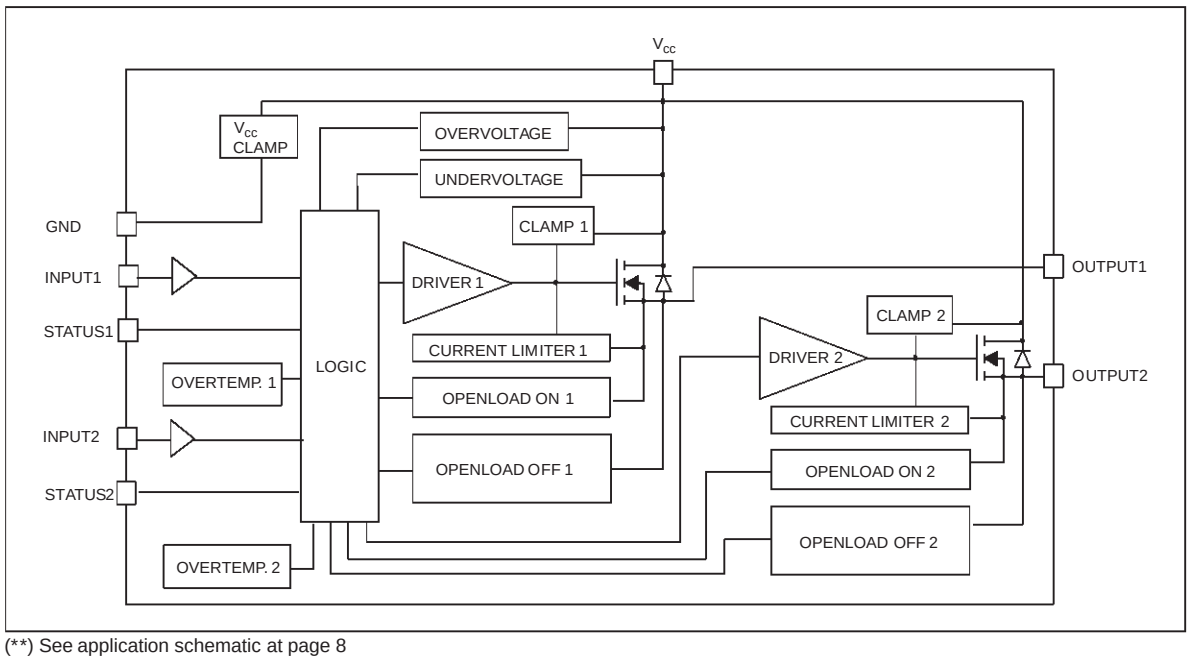


SO-16

DESCRIPTION

The VND810 is a monolithic device designed in STMicroelectronics VIPower M0-3 Technology, intended for driving any kind of load with one side connected to ground.
Active V_{CC} pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table). Active current limitation combined with thermal shutdown and automatic restart protects the device against overload. The device detects open load condition both in on and off state. Output shorted to V_{CC} is detected in the off state. Device automatically turns off in case of ground pin disconnection.

BLOCK DIAGRAM

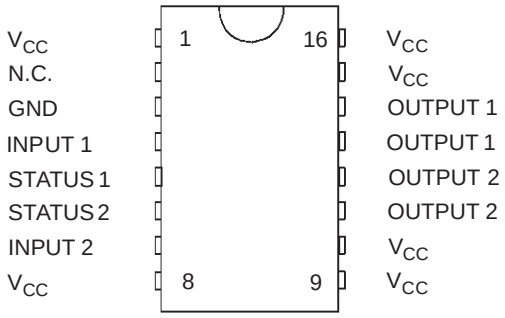


(**) See application schematic at page 8

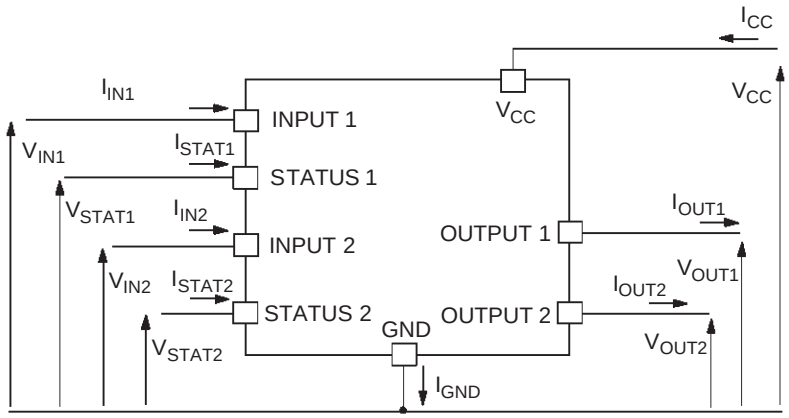
ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	41	V
- V_{CC}	Reverse DC Supply Voltage	- 0.3	V
- I_{GND}	DC Reverse Ground Pin Current	- 200	mA
I_{OUT}	DC Output Current	Internally Limited	A
- I_{OUT}	Reverse DC Output Current	- 6	A
I_{IN}	DC Input Current	+/- 10	mA
I_{stat}	DC Status Current	+/- 10	mA
V_{ESD}	Electrostatic Discharge (R=1.5KΩ; C=100pF)	2000	V
P_{tot}	Power Dissipation T_C=25°C	8.3	W
T_j	Junction Operating Temperature	Internally Limited	°C
T_c	Case Operating Temperature	- 40 to 150	°C
T_{stg}	Storage Temperature	- 55 to 150	°C

CONNECTION DIAGRAM (TOP VIEW)



CURRENT AND VOLTAGE CONVENTIONS



THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{thj\text{-}lead}$	Thermal Resistance Junction-lead	15	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	60 (*)	°C/W

(*) When mounted on a standard single-sided FR-4 board with 50mm^2 of Cu (at least 35µm thick) connected to all V_{CC} pins.

ELECTRICAL CHARACTERISTICS (8V<V_{CC}<36V; -40°C< T_j <150°C, unless otherwise specified)

(Per each channel)

POWER OUTPUTS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{CC} (**)	Operating Supply Voltage		5.5	13	36	V
V_{USD} (**)	Under Voltage Shut-down		3	4	5.5	V
V_{OV} (**)	Overvoltage Shut-down		36	42	48	V
R_{ON}	On State Resistance	I_{OUT}=1A; T_j=25°C			160	mΩ
		I_{OUT}=1A; V_{CC}>8V			320	mΩ
I_S (**)	Supply Current	Off State; V_{CC}=13V; V_{IN}=V_{OUT}=0V		12	40	µA
		Off State; V_{CC}=13V; V_{IN}=V_{OUT}=0V; T_j=25°C		12	25	µA
		On State; V_{CC}=13V; V_{IN}=5V; I_{OUT}=0A		5	7	mA
$I_{L(off1)}$	Off State Output Current	V_{IN}=V_{OUT}=0V	0		50	µA
$I_{L(off2)}$	Off State Output Current	V_{IN}=0V; V_{OUT}=3.5V	-75		0	µA

(**) Per device

SWITCHING (V_{CC}=13V)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-on Delay Time	R_L=13Ω from V_{IN} rising edge to V_{OUT}=1.3V		30		µs
$t_{d(off)}$	Turn-off Delay Time	R_L=13Ω from V_{IN} falling edge to V_{OUT}=11.7V		30		µs
$dV_{OUT}/dt_{(on)}$	Turn-on Voltage Slope	R_L=13Ω from V_{OUT}=1.3V to V_{OUT}=10.4V		0.2		V/µs
$dV_{OUT}/dt_{(off)}$	Turn-off Voltage Slope	R_L=13Ω from V_{OUT}=11.7V to V_{OUT}=1.3V		0.2		V/µs

LOGIC INPUT

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IL}	Input Low Level				1.25	V
I_{IL}	Low Level Input Current	V_{IN} = 1.25V	1			µA
V_{IH}	Input High Level		3.25			V
I_{IH}	High Level Input Current	V_{IN} = 3.25V			10	µA
$V_{I(hyst)}$	Input Hysteresis Voltage		0.5			V
V_{ICL}	Input Clamp Voltage	I_{IN} = 1mA	6	6.8	8	V
		I_{IN} = -1mA		-0.7		V

ELECTRICAL CHARACTERISTICS (continued)

STATUS PIN

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{STAT}	Status Low Output Voltage	I_{STAT}= 1.6 mA			0.5	V
I_{LSTAT}	Status Leakage Current	Normal Operation; V_{STAT}= 5V			10	µA
C_{STAT}	Status Pin Input Capacitance	Normal Operation; V_{STAT}= 5V			100	pF
V_{SCL}	Status Clamp Voltage	I_{STAT}= 1mA I_{STAT}= - 1mA	6	6.8 -0.7	8	V V

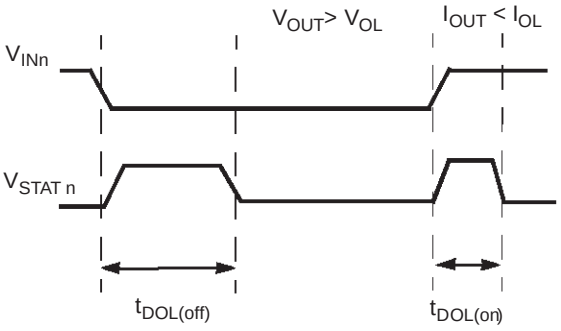
PROTECTIONS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
T_{TSD}	Shut-down Temperature		150	175	200	°C
T_R	Reset Temperature		135			°C
T_{hyst}	Thermal Hysteresis		7	15		°C
t_{SDL}	Status Delay in Overload Conditions	T_j>T_{TSD}			20	µs
I_{lim}	Current limitation	 5.5V<V_{CC}<36V	3.5	5	7.5 7.5	A A
V_{demag}	Turn-off Output Clamp Voltage	I_{OUT}=1A; L=6mH	V_{CC}-41	V_{CC}-48	V_{CC}-55	V

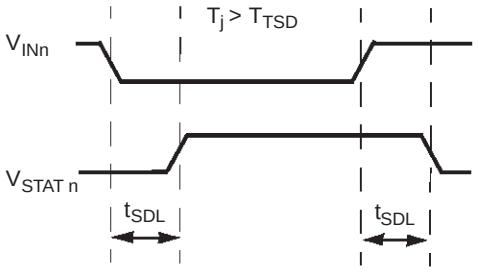
OPENLOAD DETECTION

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{OL}	Openload ON State Detection Threshold	V_{IN}=5V	20	40	80	mA
$t_{DOL(on)}$	Openload ON State Detection Delay	I_{OUT}=0A			200	µs
V_{OL}	Openload OFF State Voltage Detection Threshold	V_{IN}=0V	1.5	2.5	3.5	V
$t_{DOL(off)}$	Openload Detection Delay at Turn Off				1000	µs

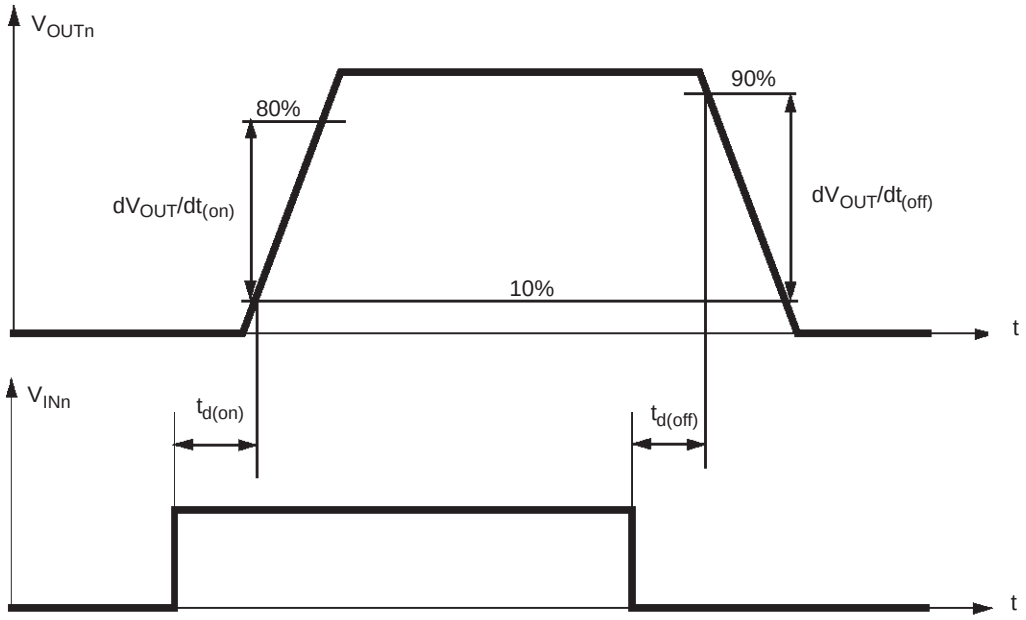
OPEN LOAD STATUS TIMING (with external pull-up)



OVERTEMP STATUS TIMING



Switching time Waveforms



TRUTH TABLE

CONDITIONS	$INPUT_n$	$OUTPUT_n$	$STATUS_n$
Normal Operation	L H	L H	H H
Current Limitation	L H	L X	H H
Overtemperature	L H	L L	H L
Undervoltage	L H	L L	X X
Overvoltage	L H	L L	H H
Output Voltage > V_{OLn}	L H	H H	L H
Output Current < I_{OLn}	L H	L H	H L

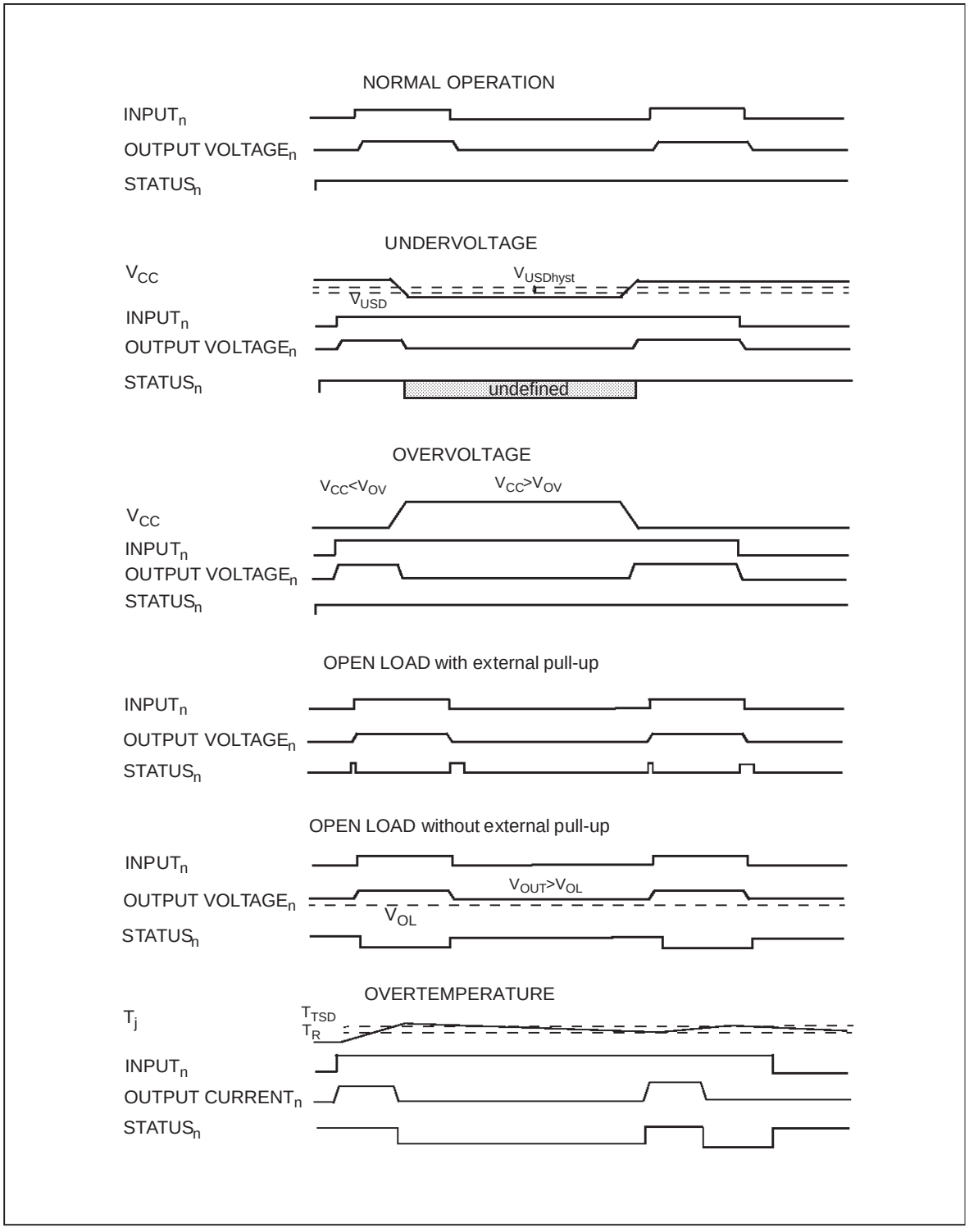
ELECTRICAL TRANSIENT REQUIREMENTS ON V_{CC} PIN

ISO T/R 7637/1 Test Pulse	TEST LEVELS				
	I	II	III	IV	Delays and Impedance
1	-25 V	-50 V	-75 V	-100 V	2 ms 10 Ω
2	+25 V	+50 V	+75 V	+100 V	0.2 ms 10 Ω
3a	-25 V	-50 V	-100 V	-150 V	0.1 µs 50 Ω
3b	+25 V	+50 V	+75 V	+100 V	0.1 µs 50 Ω
4	-4 V	-5 V	-6 V	-7 V	100 ms, 0.01 Ω
5	+26.5 V	+46.5 V	+66.5 V	+86.5 V	400 ms, 2 Ω

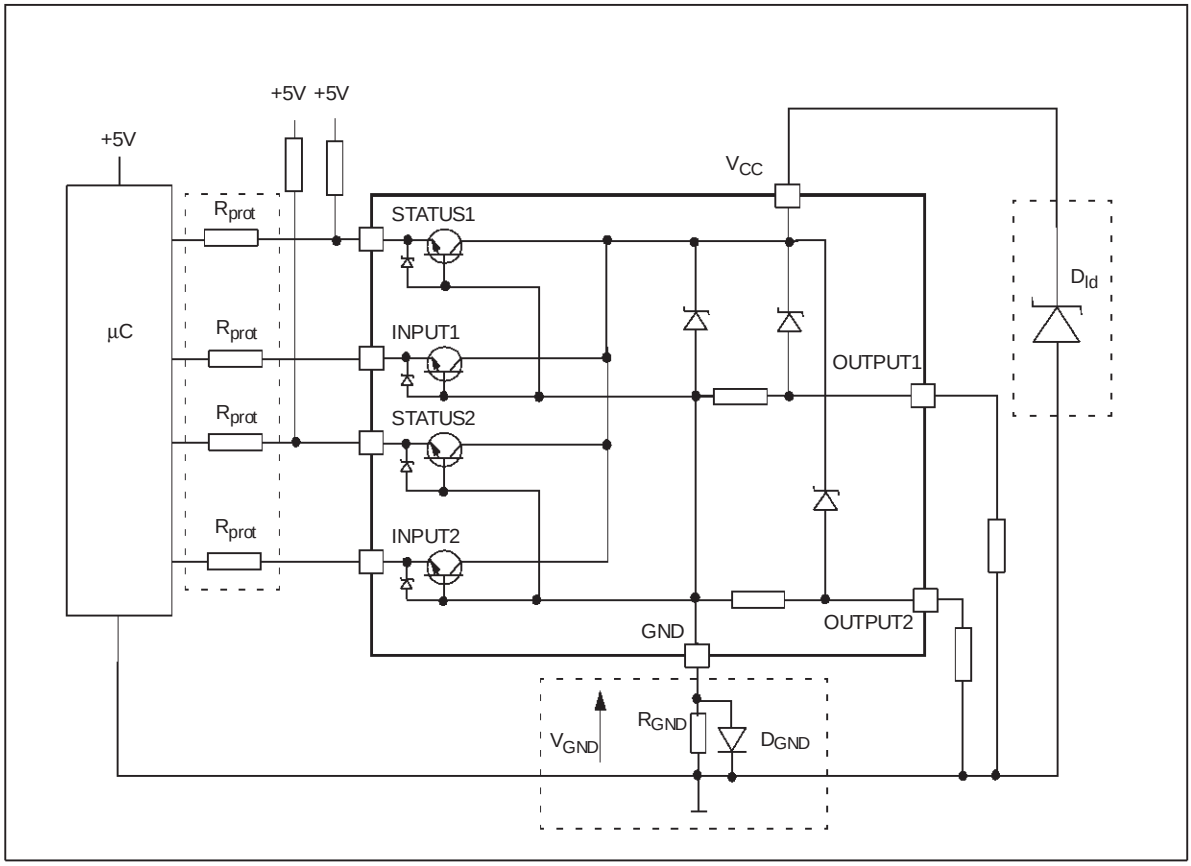
ISO T/R 7637/1 Test Pulse	TEST LEVELS RESULTS			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

CLASS	CONTENTS
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device is not performed as designed after exposure and cannot be returned to proper operation without replacing the device.

Figure1: Waveforms



APPLICATION SCHEMATIC



GND PROTECTION NETWORK AGAINST REVERSE BATTERY

Solution 1: Resistor in the ground line (R_{GND} only). This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

1) $R_{GND} \leq 600mV / I_{S(on)max}$.

2) $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device's datasheet.

Power Dissipation in R_{GND} (when V_{CC}<0: during reverse battery situations) is:

$P_D = (-V_{CC})^2/R_{GND}$

This resistor can be shared amongst several different HSD. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not common with the device ground then the R_{GND} will produce a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same R_{GND}.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then the ST suggests to utilize Solution 2 (see below).

Solution 2: A diode (D_{GND}) in the ground line.

A resistor (R_{GND}=1kΩ) should be inserted in parallel to D_{GND} if the device will be driving an inductive load.

This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network will produce a shift (j 600mV) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

LOAD DUMP PROTECTION

D_{Id} is necessary (Transil or MOV) if the load dump peak voltage exceeds V_{CC} max DC rating. The same applies if the device will be subject to transients on the V_{CC} line that are greater than the ones shown in the ISO T/R 7637/1 table.

µC I/Os PROTECTION:

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the µC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of µC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of µC I/Os.

$$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C}-V_{IH}-V_{GND}) / I_{IHmax}$$

Calculation example:

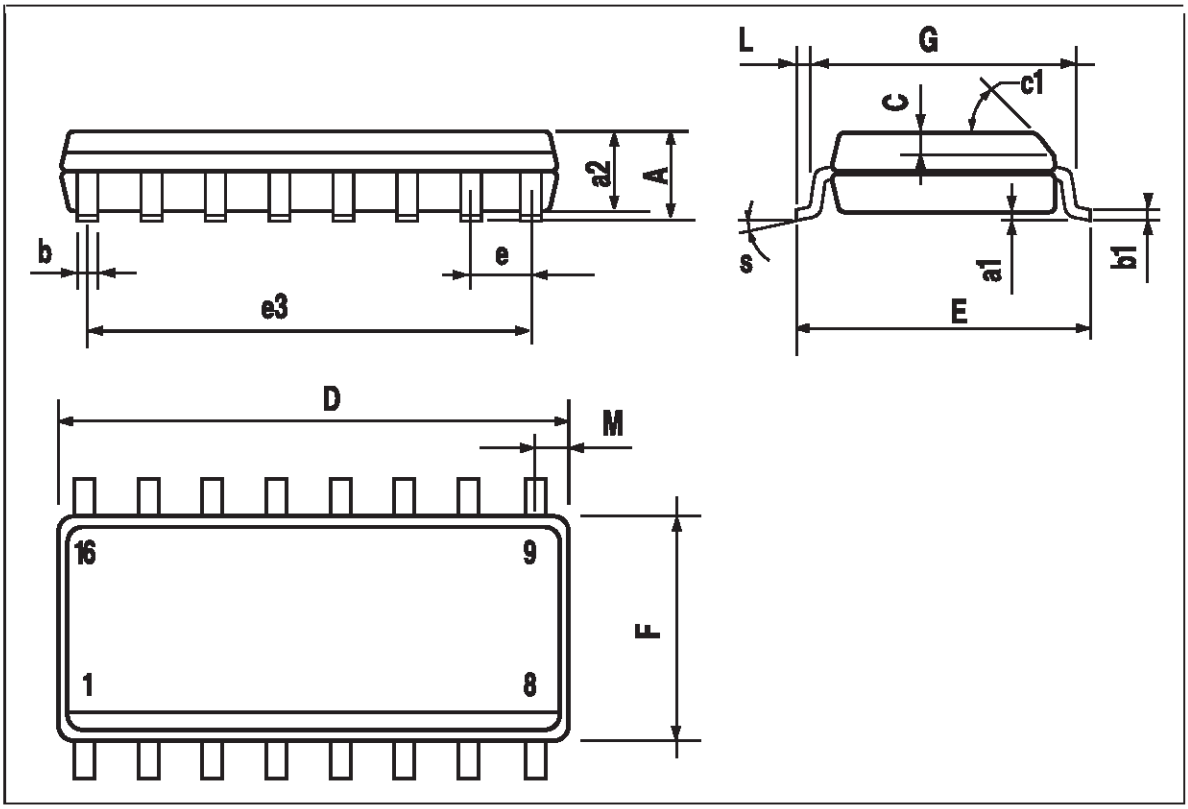
For V_{CCpeak}= - 100V and $I_{latchup} \geq$ 20mA; $V_{OH\mu C} \geq$ 4.5V

$5k\Omega \leq R_{prot} \leq 65k\Omega$.

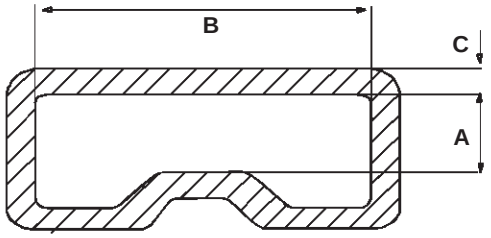
Recommended R_{prot} value is 10kΩ.

SO-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.004		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		1.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



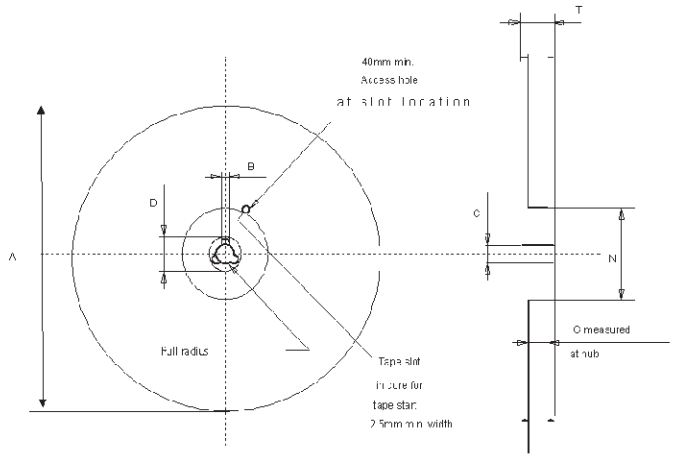
SO-16 TUBE SHIPMENT (no suffix)



Base Q.ty	50
Bulk Q.ty	1000
Tube length (± 0.5)	532
A	3.2
B	6
C (± 0.1)	0.6

All dimensions are in mm.

TAPE AND REEL SHIPMENT (suffix "13TR")



REEL DIMENSIONS

Base Q.ty	1000
Bulk Q.ty	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	16.4
N (min)	60
T (max)	22.4

All dimensions are in mm.

TAPE DIMENSIONS

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Tape width	**W**	16
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	8
Hole Diameter	**D (± 0.1/-0)**	1.5
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.05)**	7.5
Compartment Depth	**K (max)**	6.5
Hole Spacing	**P1 (± 0.1)**	2

All dimensions are in mm.