



VNA7NV04D

“OMNIFET II”: FULLY AUTOPROTECTED POWER MOSFETS

TARGET SPECIFICATION

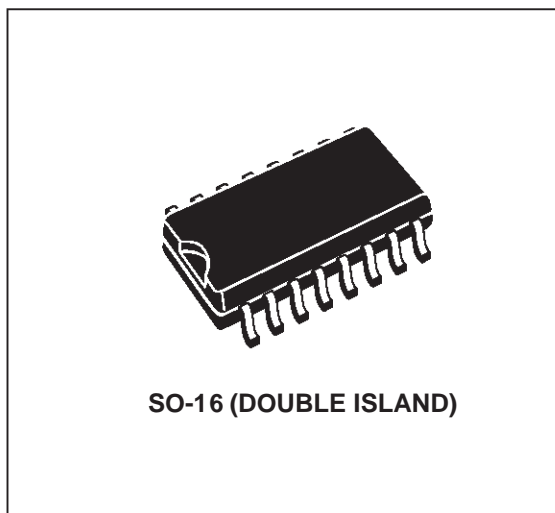
TYPE	$R_{DS(on)}$	I_{lim}	V_{clamp}
VNA7NV04D	60 mΩ (*)	6 A (*)	40 V (*)

(*) Per each device

- LINEAR CURRENT LIMITATION
- THERMAL SHUT DOWN
- SHORT CIRCUIT PROTECTIONS
- INTEGRATED CLAMP
- LOW CURRENT DRAWN FROM INPUT PINS
- DIAGNOSTIC FEEDBACK THROUGH INPUT PINS
- ESD PROTECTION
- DIRECT ACCESS TO THE GATE OF EACH POWER MOSFET (ANALOG DRIVING)
- COMPATIBLE WITH STANDARD POWER MOSFETS

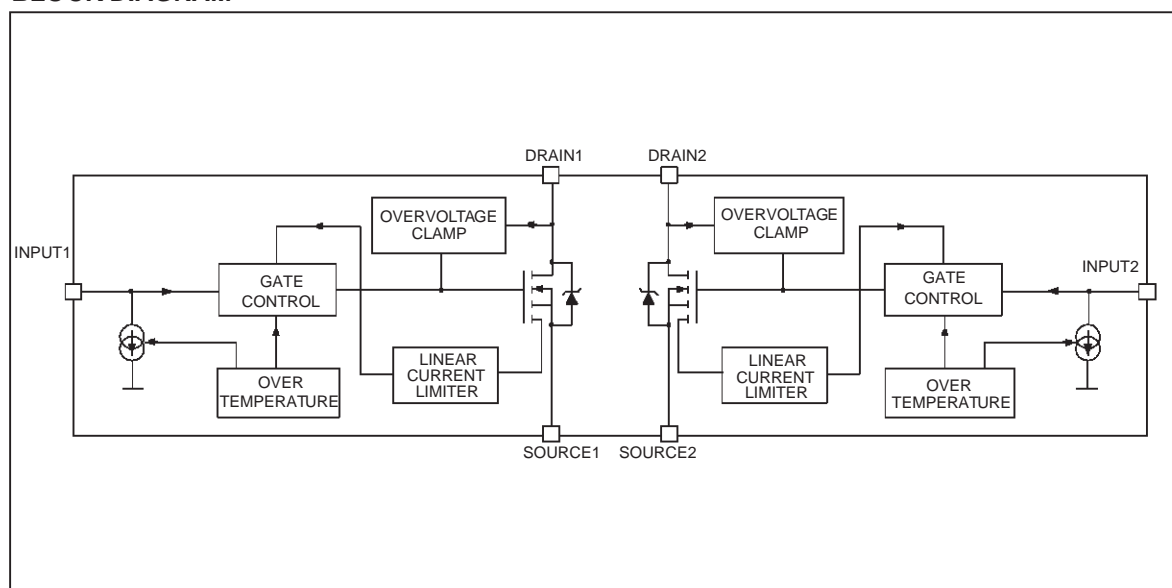
DESCRIPTION

The VNA7NV04D is a device formed by two monolithic OMNIFET II chips housed in a standard SO-16 package with double island. The OMNIFET II are designed in STMicroelectronics VIPower M0 Technology; they are intended for replacement of standard Power



MOSFETS from DC up to 50KHz applications. Built in thermal shutdown, linear current limitation and overvoltage clamp protect the chips in harsh environments. Fault feedback can be detected by monitoring the voltage at the input pins.

BLOCK DIAGRAM



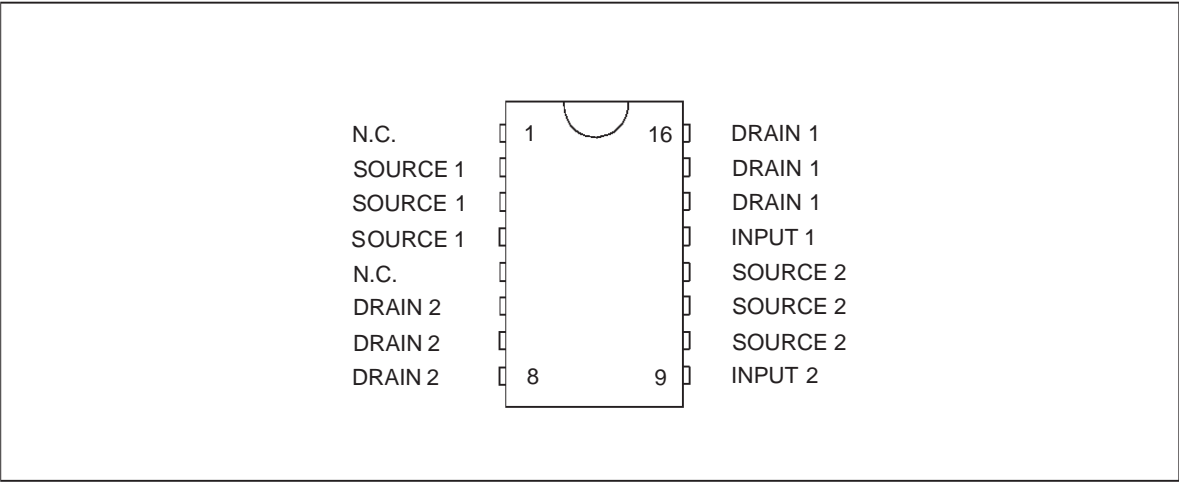
VNA7NV04D

ABSOLUTE MAXIMUM RATING

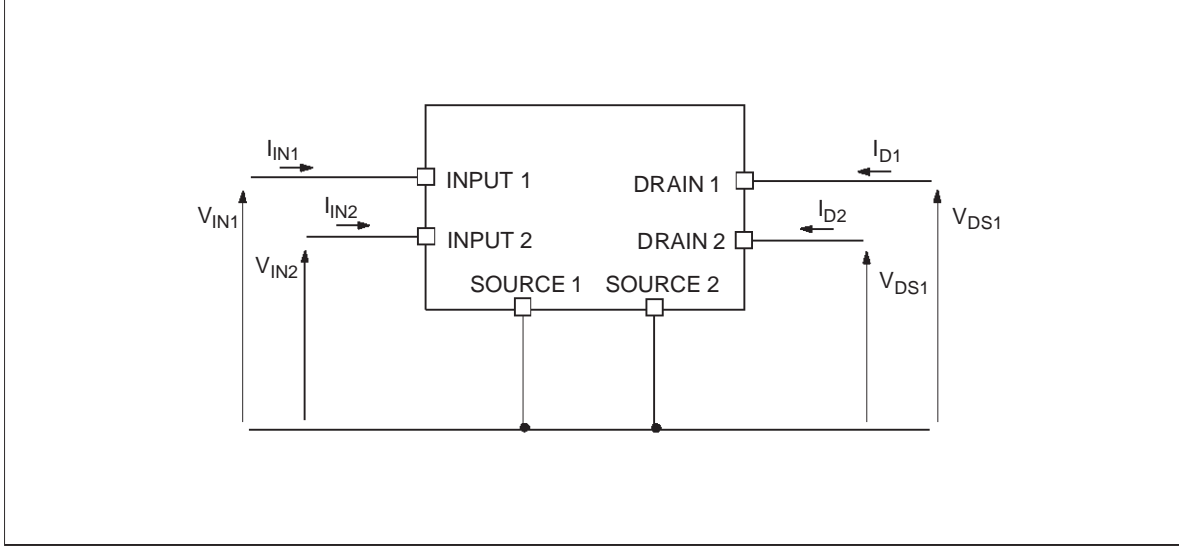
(per each device)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage ($V_{IN}=0V$)	Internally clamped	V
V_{IN}	Input Voltage	Internally clamped	V
I_{IN}	Input Current	+/- 20	mA
I_D	Drain Current	Internally Limited	A
I_R	Reverse DC Output Current	- 12	A
V_{ESD}	Electrostatic Discharge ($R=1.5K\Omega$; $C=100pF$)	4000	V
P_{tot}	Total Dissipation at $T_c=25^{\circ}C$	TBD	W
T_j	Operating Junction Temperature	Internally Limited	$^{\circ}C$
T_c	Case Operating Temperature	Internally Limited	$^{\circ}C$
T_{stg}	Storage Temperature	-55 to 150	$^{\circ}C$

CONNECTION DIAGRAM (TOP VIEW)



CURRENT AND VOLTAGE CONVENTIONS



THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal Resistance Junction-case	Max 13	°C/W
$R_{thj-amb}$	Thermal Resistance Junction-ambient	Max TBD	°C/W

ELECTRICAL CHARACTERISTICS (per each device) $-40^{\circ}\text{C} < T_j < 150^{\circ}\text{C}$, unless otherwise specified
OFF

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{CLAMP}	Drain-source Clamp Voltage	$V_{IN}=0\text{V}$; $I_D=3.5\text{A}$	40	45	50	V
V_{CLTH}	Drain-source Clamp Threshold Voltage	$V_{IN}=0\text{V}$; $I_D=2\text{mA}$	36			V
V_{INTH}	Input Threshold Voltage	$V_{DS}=V_{IN}$; $I_D=1\text{mA}$	0.5		2.5	V
I_{ISS}	Supply Current from Input Pin	$V_{DS}=0\text{V}$; $V_{IN}=5\text{V}$		100	250	μA
V_{INCL}	Input-Source Clamp Voltage	$I_{IN}=1\text{mA}$ $I_{IN}=-1\text{mA}$	6.5 -1.0	7.4	8.5 -0.3	V
I_{DSS}	Zero Input Voltage Drain Current ($V_{IN}=0\text{V}$)	$V_{DS}=13\text{V}$; $V_{IN}=0\text{V}$; $T_j=25^{\circ}\text{C}$ $V_{DS}=25\text{V}$; $V_{IN}=0\text{V}$			50 150	μA

ON

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{IN}=5\text{V}$; $I_D=3.5\text{A}$; $T_j=25^{\circ}\text{C}$ $V_{IN}=5\text{V}$; $I_D=3.5\text{A}$			60 120	m Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$g_{fs}^{(*)}$	Forward Transconductance	$V_{DD}=13\text{V}$; $I_D=3.5\text{A}$		10		S
C_{OSS}	Output Capacitance	$V_{DS}=13\text{V}$; $f=1\text{MHz}$; $V_{IN}=0\text{V}$		230		pF

SWITCHING

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=15\text{V}$; $I_D=3.5\text{A}$ $V_{gen}=5\text{V}$; $R_{gen}=10\Omega$ (see figure 1)		40	TBD	ns
t_r	Rise Time			100	TBD	ns
$t_{d(off)}$	Turn-off Delay Time			250	TBD	ns
t_f	Fall Time			90	TBD	ns
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=15\text{V}$; $I_D=3.5\text{A}$ $V_{gen}=5\text{V}$; $R_{gen}=1000\Omega$ (see figure 1)		0.6	TBD	μs
t_r	Rise Time			4.7	TBD	μs
$t_{d(off)}$	Turn-off Delay Time			7.6	TBD	μs
t_f	Fall Time			4.6	TBD	μs
$(di/dt)_{on}$	Turn-on Current Slope	$V_{DD}=15\text{V}$; $I_D=3.5\text{A}$ $V_{gen}=5\text{V}$; $R_{gen}=0\Omega$		28		A/ μs
Q_i	Total Input Charge	$V_{DD}=12\text{V}$; $I_D=3.5\text{A}$; $V_{IN}=5\text{V}$ (see figure 5)		TBD		nC

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ELECTRICAL CHARACTERISTICS (continued) ($T_j=25^{\circ}\text{C}$, unless otherwise specified)

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{SD} (*)$	Forward On Voltage	$I_{SD}=3.5\text{A}$; $V_{IN}=0\text{V}$		0.8		V
t_{rr}	Reverse Recovery Time	$I_{SD}=3.5\text{A}$; $dI/dt=20\text{A}/\mu\text{s}$		TBD		ns
Q_{rr}	Reverse Recovery Charge	$V_{DD}=30\text{V}$		TBD		μC
I_{RRM}	Reverse Recovery Current	(see test circuit, figure 2)		TBD		A

PROTECTIONS ($-40^{\circ}\text{C} < T_j < 125^{\circ}\text{C}$, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{lim}	Drain Current Limit	$V_{IN}=6.5\text{V}$; $V_{DS}=13\text{V}$	6	9	12	A
t_{dlim}	Step Response Current Limit	$V_{IN}=6.5\text{V}$; $V_{DS}=13\text{V}$		20	TBD	μs
T_{jsh}	Overtemperature Shutdown		150	175		$^{\circ}\text{C}$
T_{jrs}	Overtemperature Reset		135			$^{\circ}\text{C}$
I_{gf}	Fault Sink Current	$V_{IN}=5\text{V}$; $V_{DS}=13\text{V}$; $T_j=T_{jsh}$		15		mA
E_{as}	Single Pulse Avalanche Energy	starting $T_j=25^{\circ}\text{C}$; $V_{DD}=24\text{V}$ $V_{IN}=5\text{V}$; $R_{gen}=TBD$; $L=TBD$ (see figures 3 & 4)	200			mJ

(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

PROTECTION FEATURES (per each device)

During normal operation, the INPUT pin is electrically connected to the gate of the internal power MOSFET through a low impedance path.

The device then behaves like a standard power MOSFET and can be used as a switch from DC up to 50KHz. The only difference from the user's standpoint is that a small DC current I_{SS} (typ. 100 μ A) flows into the INPUT pin in order to supply the internal circuitry.

The device integrates:

- OVERVOLTAGE CLAMP PROTECTION:

internally set at 45V, along with the rugged avalanche characteristics of the Power MOSFET stage give this device unrivalled ruggedness and energy handling capability. This feature is mainly important when driving inductive loads.

- LINEAR CURRENT LIMITER CIRCUIT:

limits the drain current I_D to I_{lim} whatever the INPUT pin voltages. When the current limiter is active, the device operates in the linear region, so power dissipation may exceed the capability of the heatsink. Both case and junction temperatures increase, and if this phase lasts long enough, junction temperature may reach the overtemperature threshold T_{jsh} .

- OVERTEMPERATURE AND SHORT CIRCUIT PROTECTION:

these are based on sensing the chip temperature and are not dependent on the input voltage. The location of the sensing element on the chip in the power stage area ensures fast, accurate detection of the junction temperature. Overtemperature cutout occurs in the range 150 to 190 °C, a typical value being 170 °C. The device is automatically restarted when the chip temperature falls of about 15°C below shut-down temperature.

- STATUS FEEDBACK:

in the case of an overtemperature fault condition ($T_j > T_{jsh}$), the device tries to sink a diagnostic current I_{gf} through the INPUT pin in order to indicate fault condition. If driven from a low impedance source, this current may be used in order to warn the control circuit of a device shutdown. If the drive impedance is high enough so that the INPUT pin driver is not able to supply the current I_{gf} , the INPUT pin will fall to 0V. **This will not however affect the device operation: no requirement is put on the current capability of the INPUT pin driver except to be able to supply the normal operation drive current I_{SS} .**

Additional features of this device are ESD protection according to the Human Body model and the ability to be driven from a TTL Logic circuit.

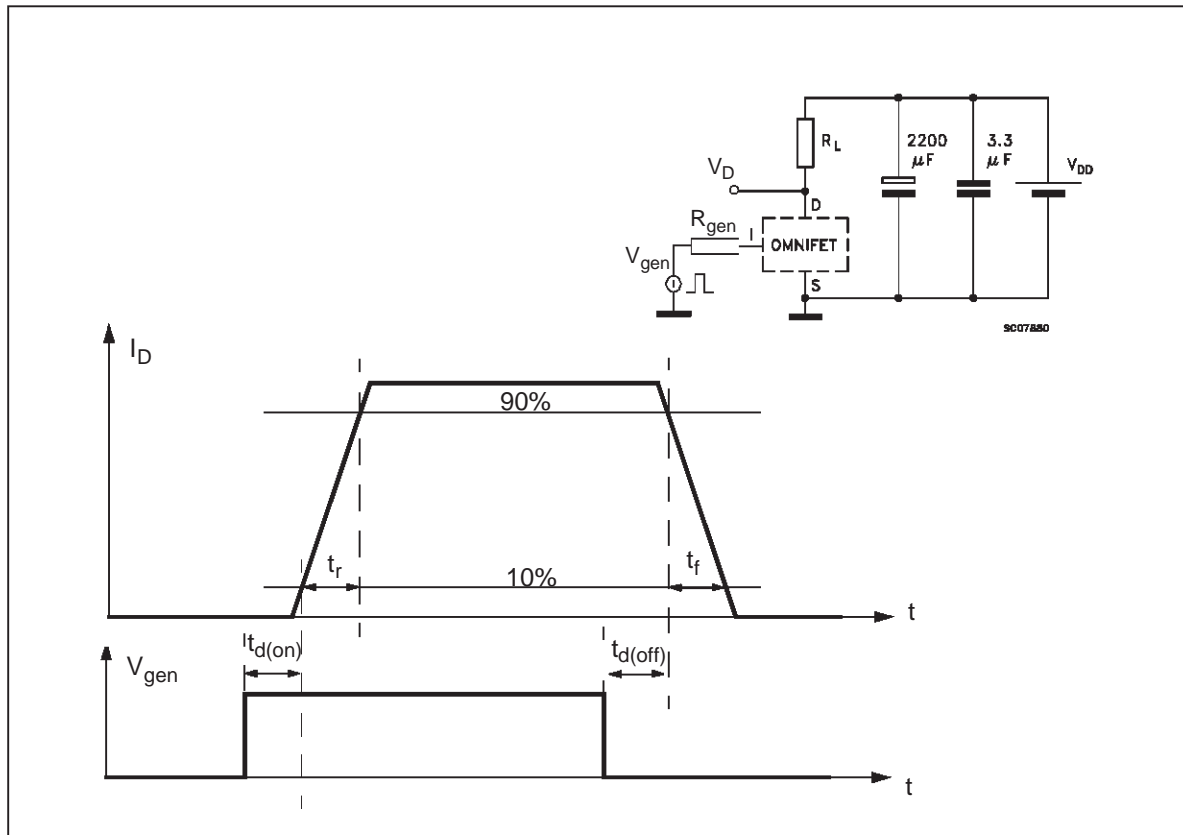
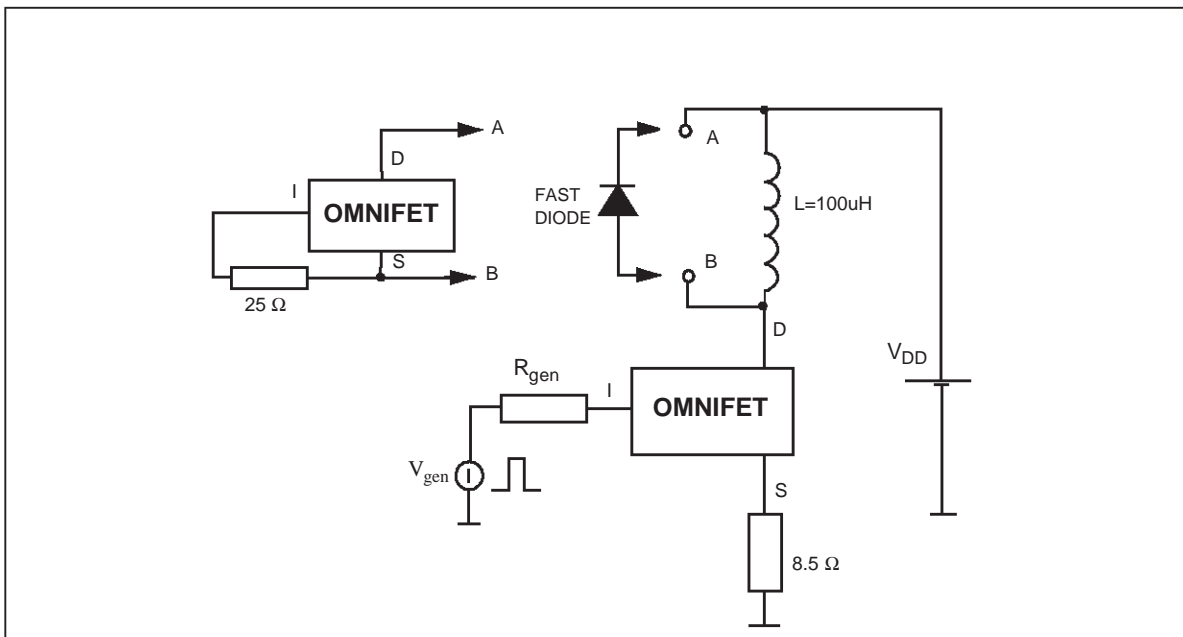
Fig.1: Switching Time Test Circuit for Resistive Load (per single chip)**Fig.2:** Test Circuit for Diode Recovery Times (per single chip)

Fig. 3: Unclamped Inductive Load Test Circuits
(per single chip)

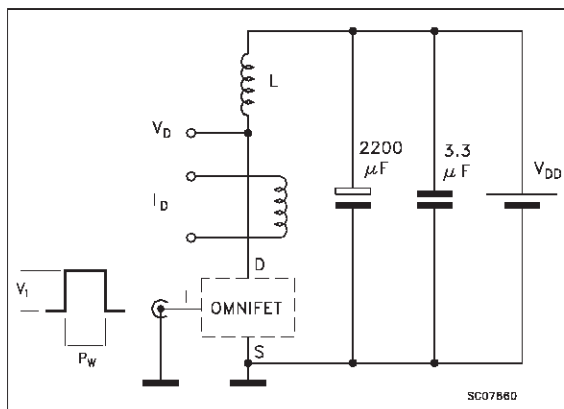


Fig. 4: Unclamped Inductive Waveforms
(per single chip)

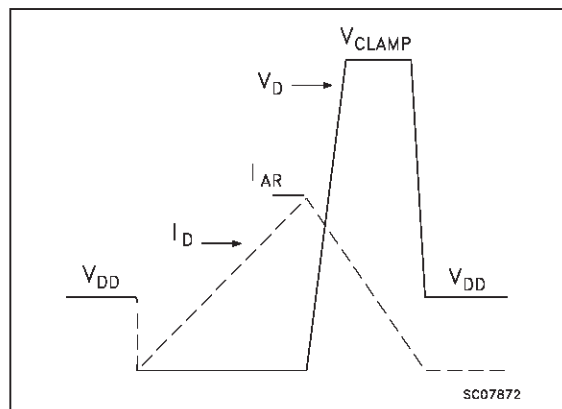
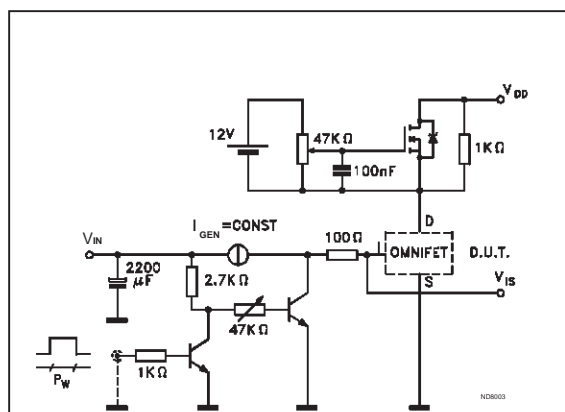
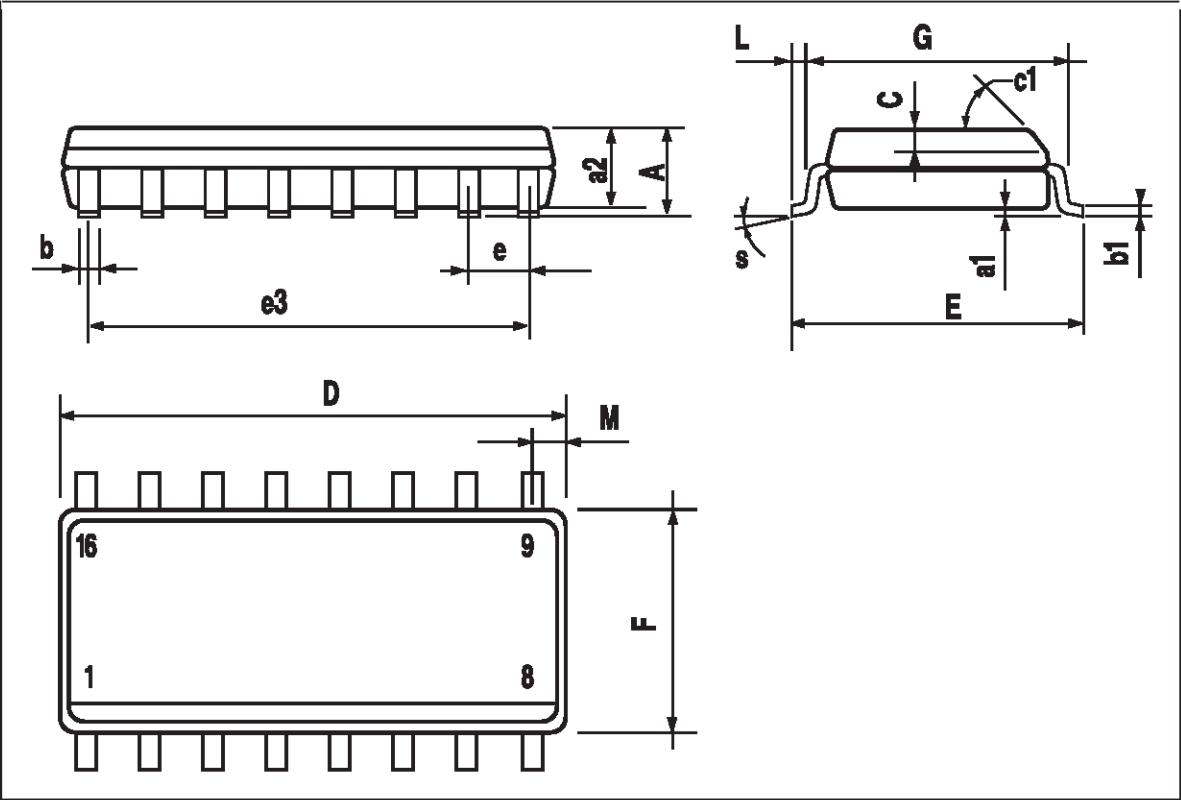


Fig. 5: Input Charge Test Circuit
(per single chip)

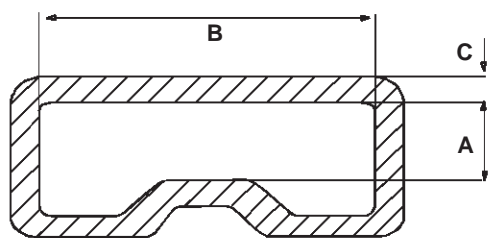


SO-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.004		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
F	3.8		4.0	0.149		1.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



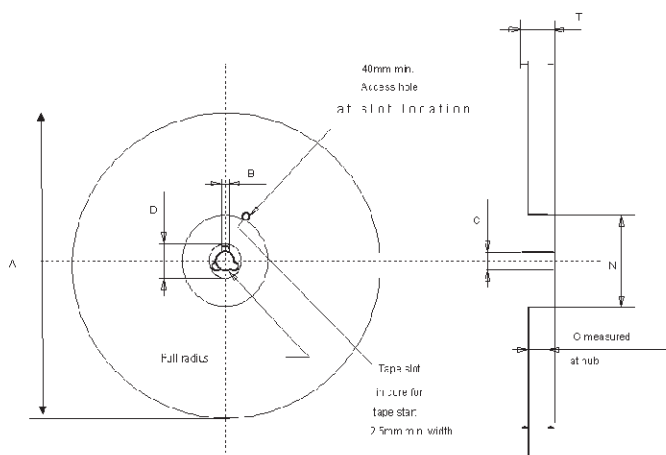
SO-16 TUBE SHIPMENT (no suffix)



Base Q.ty	50
Bulk Q.ty	1000
Tube length (± 0.5)	532
A	3.2
B	6
C (± 0.1)	0.6

All dimensions are in mm.

TAPE AND REEL SHIPMENT (suffix "13TR")



REEL DIMENSIONS

Base Q.ty	1000
Bulk Q.ty	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / - 0)	16.4
N (min)	60
T (max)	22.4

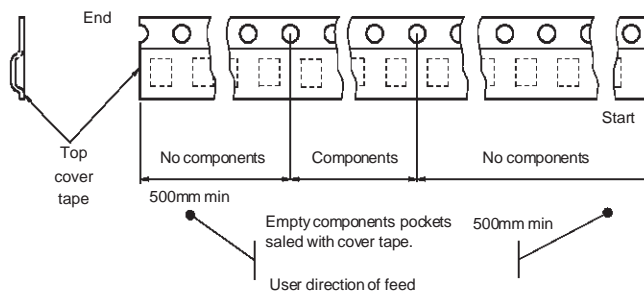
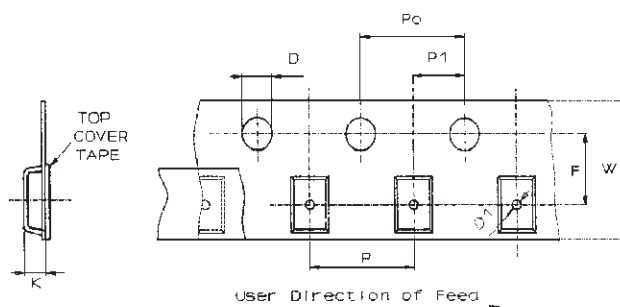
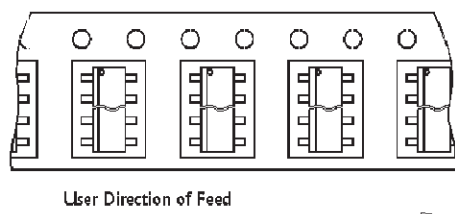
All dimensions are in mm.

TAPE DIMENSIONS

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Tape width	W	16
Tape Hole Spacing	P0 (± 0.1)	4
Component Spacing	P	8
Hole Diameter	D ($\pm 0.1/-0$)	1.5
Hole Diameter	D1 (min)	1.5
Hole Position	F (± 0.05)	7.5
Compartment Depth	K (max)	6.5
Hole Spacing	P1 (± 0.1)	2

All dimensions are in mm.



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