STPC® ATLAS

X86 PC Compatible Information Appliance System-on-Chip

PRODUCT PREVIEW

- POWERFUL x86 PROCESSOR
- 64-BIT SDRAM UMA CONTROLLER
- GRAPHICS CONTROLLER
  - VGA & SVGA CRT CONTROLLER
  - 135MHz RAMDAC
  - ENHANCED 2D GRAPHICS ENGINE
- VIDEO INPUT PORT
- VIDEO PIPELINE
  - UP-SCALER
  - VIDEO COLOUR SPACE CONVERTER
  - CHROMA & COLOUR KEY SUPPORT
- TFT DISPLAY CONTROLLER
- PCI 2.1 COMPLIANT MASTER / SLAVE/ ARBITER
- ISA MASTER / SLAVE CONTROLLER
- 16-BIT LOCAL BUS INTERFACE
- PCMCIA INTERFACE CONTROLLER
- Ultra DMA-33 IDE CONTROLLER
- 2 USB HOST HUB INTERFACES
- I/O FEATURES
  - PC/AT+ KEYBOARD CONTROLLER
  - PS/2 MOUSE CONTROLLER
  - 2 SERIAL PORTS
  - 1 PARALLEL PORT
  - 16 GENERAL PURPOSE I/Os
  - I C INTERFACE
- INTEGRATED PERIPHERAL CONTROLLER
  - DMA CONTROLLER
  - INTERRUPT CONTROLLER
  - TIMER / COUNTERS
- POWER MANAGEMENT UNIT
- WATCHDOG
- JTAG IEEE1149.1

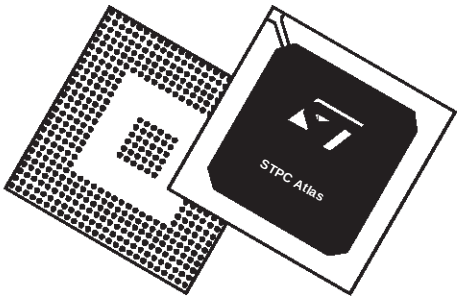

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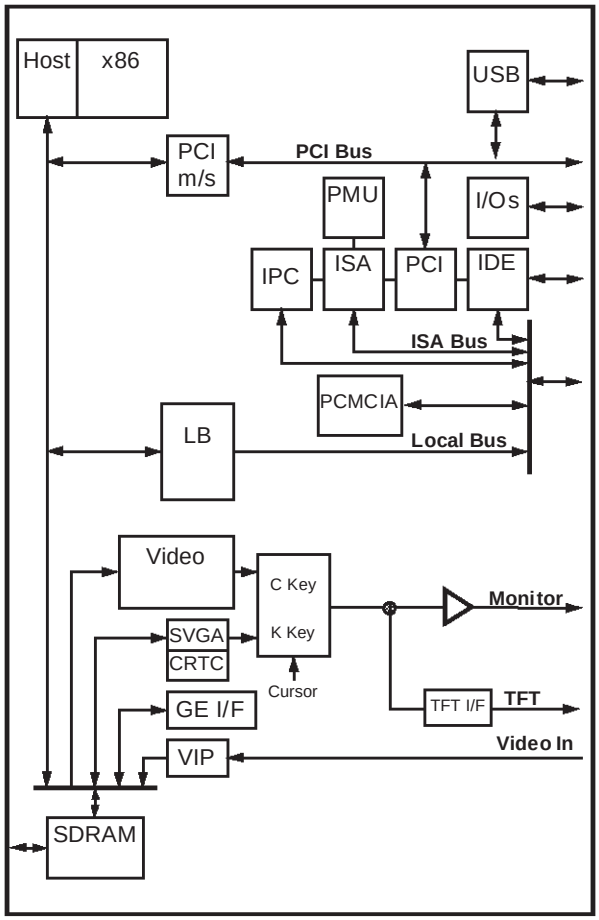
Figure 0-1. Logic Diagram



Issue 1.0

DESCRIPTION

The STPC Atlas integrates a standard 5th generation x86 core along with a powerful UMA graphics/video chipset, support logic including PCI, ISA, Local Bus, USB, UIDE controllers and combines them with standard I/O interfaces to provide a single PC compatible subsystem on a single device, suitable for all kinds of terminal and industrial appliances.

- **X86 Processor core**
- Fully static 32-bit 5-stage pipeline, x86 processor fully PC compatible.
- Can access up to 4GB of external memory.
- 8Kbyte unified instruction and data cache with write back and write through capability.
- Parallel processing integral floating point unit, with automatic power down.
- Runs up to 100MHz (X1) or 133 MHz (X2).
- Fully static design for dynamic clock control.
- Low power and system management modes.
- Optimized design for 2.5V operation.

- **SDRAM Controller**
- 64-bit data bus.
- Up to 100MHz SDRAM clock speed.
- Integrated system memory, graphic frame memory and video frame memory.
- Supports 8MB up to 128 MB system memory.
- Supports 16-Mbit, 64-Mbit and 128-Mbit SDRAMs.
- Supports 8, 16, 32, 64, and 128 MB DIMMs.
- Supports buffered, non buffered, and registered DIMMs
- 4-line write buffers for CPU to DRAM and PCI to DRAM cycles.
- 4-line read prefetch buffers for PCI masters.
- Programmable latency
- Programmable timing for SDRAM parameters.
- Supports -8, -10, -12, -13, -15 memory parts
- Supports memory hole between 1MB and 8MB for PCI/ISA busses.
- 32-bit access, Autoprecharge & Power-down are not supported.

- **Enhanced 2D Graphics Controller**
- Supports pixel depths of 8, 16, 24 and 32 bit.
- Full BitBLT implementation for all 256 raster operations defined for Windows.
- Supports 4 transparent BLT modes - Bitmap Transparency, Pattern Transparency, Source Transparency and Destination Transparency.
- Hardware clipping
- Fast line draw engine with anti-aliasing.
- Fast triangle fill engine.
- Supports 4-bit alpha blended font for anti-aliased text display.
- Complete double buffered registers for pipelined operation.
- 64-bit wide pipelined architecture running at 100 MHz. Hardware clipping

- **CRT Controller**
- Integrated 135MHz triple RAMDAC allowing for 1280 x 1024 x 75Hz display.
- 8-, 16-, 24-bit pixels.
- Interlaced or non-interlaced output.

- **Video Input port**
- Accepts video inputs in CCIR 601/656 mode.
- Optional 2:1 decimator
- Stores captured video in off setting area of the onboard frame buffer.
- HSYNC and B/T generation or lock onto external video timing source.

- **Video Pipeline**
- Two-tap interpolative horizontal filter.
- Two-tap interpolative vertical filter.
- Color space conversion (RGB to YUV and YUV to RGB).
- Programmable window size.
- Chroma and color keying for integrated video overlay.

DESCRIPTION

- **TFT Interface**
- Programmable panel size up to 1024 by 1024 pixels.
- Support for VGA and SVGA active matrix TFT flat panels with 9, 12, 18-bit interface (1 pixel per clock).
- Support for XGA and SXGA active matrix TFT flat panels with 2 x 9-bit interface (2 pixels per clock).
- Programmable image positionning.
- Programmable blank space insertion in text mode.
- Programmable horizontal and vertical image expansion in graphic mode.
- Two fully programmable PWM (Pulse Width Modulator) signals to adjust the flat panel brightness and contrast.
- Supports **PanelLink**TM high speed serial transmitter externally for high resolution panel interface.

- **PCI Controller**
- Compliant with PCI 2.1 specification.
- Integrated PCI arbitration interface. Up to 3 masters can connect directly. External logic allows for greater than 3 masters.
- Translation of PCI cycles to ISA bus.
- Translation of ISA master initiated cycle to PCI.
- Support for burst read/write from PCI master.
- PCI clock is 1/2, 1/3 or 1/4 CPU bus clock.

- **ISA master/slave**
- Generates the ISA clock from either 14.318MHz oscillator clock or PCI clock
- Supports programmable extra wait state for ISA cycles
- Supports I/O recovery time for back to back I/O cycles.
- Fast Gate A20 and Fast reset.
- Supports the single ROM that C, D, or E. blocks shares with F block BIOS ROM.
- Supports flash ROM.
- Supports ISA hidden refresh.
- Buffered DMA & ISA master cycles to reduce bandwidth utilization of the PCI and Host bus.

- **Local Bus interface**
- Multiplexed with ISA/DMA interface.
- Low latency asynchronous bus
- 16-bit data bus with word steering capability.
- Programmable timing (Host clock granularity)
- 4 Programmable Flash Chip Select.
- 8 Programmable I/O Chip Select.
- I/O device timing (setup & recovery time) programmable
- Supports 32-bit Flash burst.
- 2-level hardware key protection for Flash boot block protection.
- Supports 2 banks of 32MB flash devices with boot block shadowed to 0x000F0000.
- Reallocatable Memory space Windows

- **Ultra DMA-33 IDE Interface**
- Compatible with EIDE (ATA-2).
- Backward compatibility with IDE (ATA-1).
- Supports up to 4 IDE devices
- Supports PIO and Bus Master IDE
- Supports up to Mode 5 Timings
- Concurrent channel operation (PIO & DMA modes) - 4 x 32-Bit Buffer FIFO per channel
- Support for 11.1/16.6 MB/s, I/O Channel Ready PIO data transfers.
- Supports 13.3/16.6/33 MB/s DMA data transfers
- Bus Master with scatter/gather capability
- Multi-word DMA support for fast IDE drives
- Individual drive timing for all four IDE devices
- Supports both legacy & native IDE modes
- Supports hard drives larger than 528MB
- Support for CD-ROM and tape peripherals

- **Integrated Peripheral Controller**
- 2X8237/AT compatible 7-channel DMA controller.
- 2X8259/AT compatible interrupt Controller. 16 interrupt inputs - ISA and PCI.
- Three 8254 compatible Timer/Counters.
- Co-processor error support logic.
- Supports external RTC (Not in Local Bus Mode).

- **PCMCIA interface**
- Support one PCMCIA 2.0 / JEIDA 4.1 68-pin standard PC Card Socket.
- Power Management support.
- Support PCMCIA/ATA specifications.
- Support I/O PC Card with pulse-mode interrupts.
- Provides an ExCA™ implementation to PCMCIA 2.0 / JEIDA 4.1 standards.

- **USB Interface**
- USB 1.1 compatible.
- Open HCI 1.0 compliant.
- User configurable RootHub.
- Support for both LowSpeed and HighSpeed USB devices.
- No bi-directionnal or Tri-state busses.
- No level sensitive latches.
- System Management Interrupt pin support
- Hooks for legacy device support.

- **Keyboard interface**
- Fully PC/AT+ compatible

- **Mouse interface**
- Fully PS/2 compatible

- **Serial interface**
- 15540 compatible
- Programmable word length, stop bits, parity.
- 16-bit programmable baud rate generator.
- Interrupt generator.
- Loop-back mode.
- 8-bit scratch register.
- Two 16-bit FIFOs.
- Two DMA handshake lines.

Parallel port
- All IEEE Standard 1284 protocols supported: Compatibility, Nibble, Byte, EPP, and ECP modes.
- 16 bytes FIFO for ECP.

- **Power Management**
- Four power saving modes: On, Doze, Standby, Suspend.
- Programmable system activity detector
- Supports Intel & Cyrix SMM and APM.
- Supports STOPCLK.
- Supports IO trap & restart.
- Independent peripheral time-out timer to monitor hard disk, serial & parallel port.
- 128K SM_RAM address space from 0xA0000 to 0xB0000

- **JTAG**
- Boundary Scan compatible IEEE1149.1.
- Scan Chain control.
- Bypass register compatible IEEE1149.1.
- ID register compatible IEEE1149.1.
- RAM BIST control.

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