



PC Compatible Embeded Microprocessor

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- PBGA388

The diagram illustrates a computer system architecture. At the top left, a box labeled "Host" contains "x86". Below it, a vertical line represents the system bus. To the right of this line, a box labeled "PCI m/s" is connected to the bus. Further right, a horizontal line represents the "PCI Bus", which connects to a "PMU" (Power Management Unit) and a series of peripheral devices: "IPC", "ISA", "PCI", and "IDE". Below the "PCI Bus", a horizontal line represents the "ISA Bus", which connects to the "ISA" and "IDE" devices. To the left of the "PCI m/s" box, a box labeled "LB" (Local Bus) is connected to the system bus. Below the "LB" box, a horizontal line represents the "Local Bus", which connects to the "IPC", "ISA", and "IDE" devices. Below the "Local Bus", a box labeled "Video" is connected to the system bus. To the right of the "Video" box, a box labeled "C Key" is connected to the system bus. Below the "C Key" box, a box labeled "K Key" is connected to the system bus. Below the "K Key" box, a box labeled "Cursor" is connected to the system bus. Below the "Cursor" box, a box labeled "TVO" (Television Out) is connected to the system bus. Below the "TVO" box, a box labeled "Encoder" is connected to the system bus. Below the "Encoder" box, a box labeled "TV" is connected to the system bus. Below the "TV" box, a box labeled "Monitor" is connected to the system bus. Below the "Monitor" box, a box labeled "SDRAM" (Static Random Access Memory) is connected to the system bus. The system bus is represented by a vertical line with multiple horizontal connections to the various components.

The STPC Consumer-S integrates a standard 5th generation x86 core, a Synchronous DRAM controller, a graphics subsystem, a video input port, video pipeline, and support logic including PCI, ISA, and IDE controllers to provide a single consumer orientated PC compatible subsystem on a single device.

The device is based on a tightly coupled Unified Memory Architecture (UMA), sharing the same memory array between the CPU main memory and the graphics and video frame buffers.

The STPC Consumer-S is packaged in a 388 Plastic Ball Grid Array (PBGA).

STPC CONSUMER-S OVERVIEW

■ **X86 Processor core**

- Fully static 32-bit 5-stage pipeline, x86 processor fully PC compatible.
- Can access up to 4GB of external memory.
- 8Kbyte unified instruction and data cache with write back and write through capability.
- Parallel processing integral floating point unit, with automatic power down.
- Fully static design for dynamic clock control.
- Low power and system management modes.

■ **SDRAM Controller**

- 64-bit data bus.
- Up to 66MHz SDRAM clock speed.
- Integrated system memory, graphic frame memory and video frame memory.
- Supports 2MB up to 128 MB memory.
- Supports 8MB, 16M, and 32MB DIMMS.
- Supports buffered, non buffered, and registered DIMMS.
- 4-line write buffers for CPU to DRAM and PCI to DRAM cycles.
- 4-line read prefetch buffers for PCI masters.
- Programmable latency
- Programmable timing for DRAM parameters.
- Supports -8, -10 memory parts
- Supports 1MB up to 8MB memory hole.
- 32-bit accesses not supported.
- Autoprecharge not supported.
- Power down not supported.
- FPM and EDO not supported.
- Supports 16M-bit full page mode SDRAMs (1M x 16, 2M x 8 & 4M x 4)

■ **Graphics Controller**

- 64-bit windows accelerator.
- Compatibility to VGA & SVGA standards.
- Hardware acceleration for text, bitblts, transparent blts and fills.
- Up to 64 x 64 bit graphics hardware cursor.
- Up to 4MB long linear frame buffer.
- 8-, 16-, and 24-bit pixels.

■ **CRT Controller**

- Integrated 135MHz triple RAMDAC allowing for 1024 x 768 x 75Hz display.
- 8-, 16-, 24-bit pixels.
- Interlaced or non-interlaced output.

■ **Video Input port**

- Accepts video inputs in CCIR 601 mode.
- Optional 2:1 decimator
- Stores captured video in off setting area of the onboard frame buffer.
- Video pass through to the onchip PAL/NTSC encoder for full screen video images.
- HSYNC and B/T generation or lock onto external video timing source.

■ **Video Pipeline**

- Two-tap interpolative horizontal filter.
- Two-tap interpolative vertical filter.
- Color space conversion.
- Programmable window size.
- Chroma and color keying for integrated video overlay.

■ **TV Output**

- Programmable two tap filter with gamma correction or three tap flicker filter.
- Progressive to interlaced scan converter.
- NTSC-M, PAL-M, PAL-B,D,G,H,I, PAL-N easy programmable video outputs.
- CCIR601 encoding with programmable color subcarrier frequencies.
- Line skip/insert capability
- Interlaced or non-interlaced operation mode.
- 625 lines/50Hz or 525 lines/60Hz 8 bit multiplexed CB-Y-CR digital input.
- CVBS and R,G,B simultaneous analog outputs through 10-bit DACs.
- Cross color reduction by specific trap filtering on luma within CVBS flow.
- Power down mode available on each DAC.

■ PCI Controller

- Fully compliant with PCI 2.1 specification.
- Integrated PCI arbitration interface. Up to 3 masters can connect directly. External PAL allows for greater than 3 masters.
- Translation of PCI cycles to ISA bus.
- Translation of ISA master initiated cycle to PCI.
- Support for burst read/write from PCI master.
- PCI clock is 1/3 or 1/2 Host clock .

■ ISA master/slave controller

- Generates the ISA clock from either 14.318MHz oscillator clock or PCI clock
- Supports programmable extra wait state for ISA cycles
- Supports I/O recovery time for back to back I/O cycles.
- Fast Gate A20 and Fast reset.
- Supports the single ROM that C, D, or E. blocks shares with F block BIOS ROM.
- Supports flash ROM.
- Supports ISA hidden refresh.
- Buffered DMA & ISA master cycles to reduce bandwidth utilization of the PCI and Host bus. NSP compliant.

■ Integrated Peripheral Controller

- 2X8237/AT compatible 7-channel DMA controller.
- 2X8259/AT compatible interrupt Controller. 16 interrupt inputs - ISA and PCI.
- Three 8254 compatible Timer/Counters.
- Co-processor error support logic.
- Supports external RTC.

■ Local Bus interface

- Multiplexed with ISA interface.
- Low latency bus
- 22-bit address bus.
- 16-bit data bus with word steering capability.
- Programmable timing (Host clock granularity)
- 2 Programmable Flash Chip Select.
- 4 Programmable I/O Chip Select.
- Supports 32-bit Flash burst.
- 2-level hardware key protection for Flash boot block protection.
- Supports 2 banks of 8MB flash devices with boot block shadowed to 0x000F0000.

■ IDE Interface

- Supports PIO and Bus Master IDE
- Supports up to Mode 5 Timings
- Transfer Rates to 22 MBytes/sec
- Supports up to 4 IDE devices
- Concurrent channel operation (PIO & DMA modes) - 4 x 32-Bit Buffer FIFO per channel
- Support for PIO mode 3 & 4.
- Support for DMA mode 1 & 2.
- Bus Master with scatter/gather capability
- Multi-word DMA support for fast IDE drives
- Individual drive timing for all four IDE devices
- Supports both legacy & native IDE modes
- Supports hard drives larger than 528MB
- Support for CD-ROM and tape peripherals
- Backward compatibility with IDE (ATA-1).

■ Power Management

- Four power saving modes: On, Doze, Standby, Suspend.
- Programmable system activity detector
- Supports SMM.
- Supports STOPCLK.
- Supports IO trap & restart.
- Independent peripheral time-out timer to monitor hard disk, serial & parallel ports.
- Supports RTC, interrupts and DMAs wake-up

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