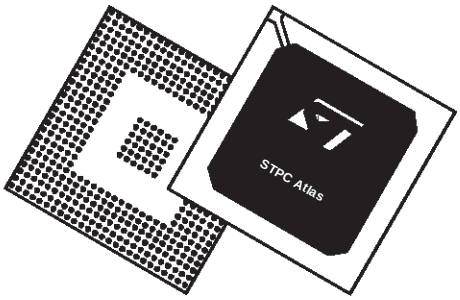
STPC® ATLAS

X86 PC Compatible Information Appliance System-on-Chip

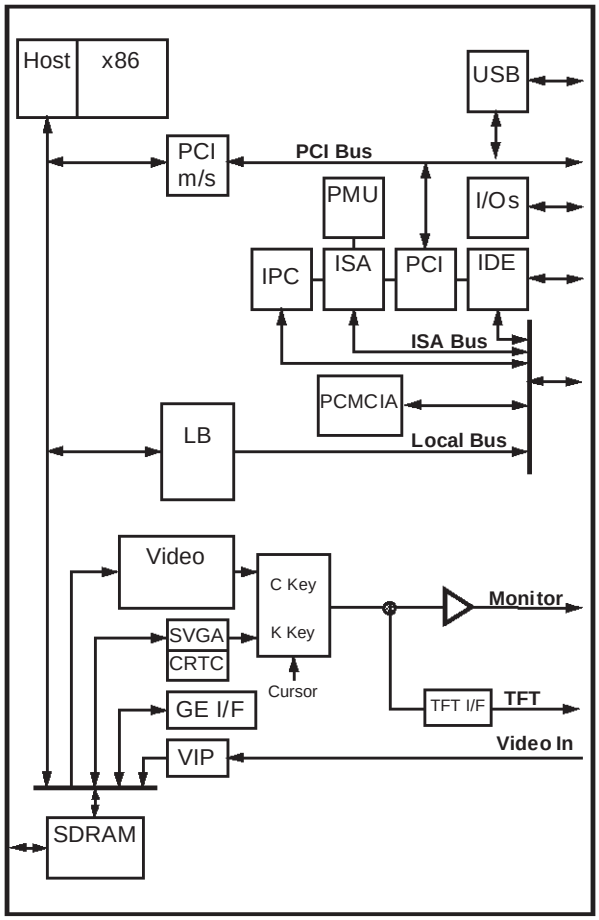
PRODUCT PREVIEW

- POWERFUL x86 PROCESSOR
- 64-BIT SDRAM UMA CONTROLLER
- GRAPHICS CONTROLLER
  - VGA & SVGA CRT CONTROLLER
  - 135MHz RAMDAC
  - ENHANCED 2D GRAPHICS ENGINE
- VIDEO INPUT PORT
- VIDEO PIPELINE
  - UP-SCALER
  - VIDEO COLOUR SPACE CONVERTER
  - CHROMA & COLOUR KEY SUPPORT
- TFT DISPLAY CONTROLLER
- PCI 2.1 COMPLIANT MASTER / SLAVE/ ARBITER
- ISA MASTER / SLAVE CONTROLLER
- 16-BIT LOCAL BUS INTERFACE
- PCMCIA INTERFACE CONTROLLER
- Ultra DMA-33 IDE CONTROLLER
- 2 USB HOST HUB INTERFACES
- I/O FEATURES
  - PC/AT+ KEYBOARD CONTROLLER
  - PS/2 MOUSE CONTROLLER
  - 2 SERIAL PORTS
  - 1 PARALLEL PORT
  - 16 GENERAL PURPOSE I/Os
  - I C INTERFACE
- INTEGRATED PERIPHERAL CONTROLLER
  - DMA CONTROLLER
  - INTERRUPT CONTROLLER
  - TIMER / COUNTERS
- POWER MANAGEMENT UNIT
- WATCHDOG
- JTAG IEEE1149.1



PBGA516

Figure 0-1. Logic Diagram



Release C

DESCRIPTION

The STPC Atlas integrates a standard 5th generation x86 core along with a powerful UMA graphics/video chipset, support logic including PCI, ISA, Local Bus, USB, UIDE controllers and combines them with standard I/O interfaces to provide a single PC compatible subsystem on a single device, suitable for all kinds of terminal and industrial appliances.

- **X86 Processor core**
- Fully static 32-bit 5-stage pipeline, x86 processor fully PC compatible.
- Can access up to 4GB of external memory.
- 8Kbyte unified instruction and data cache with write back and write through capability.
- Parallel processing integral floating point unit, with automatic power down.
- Runs up to 100MHz (X1) or 133 MHz (X2).
- Fully static design for dynamic clock control.
- Low power and system management modes.
- Optimized design for 2.5V operation.

- **SDRAM Controller**
- 64-bit data bus.
- Up to 100MHz SDRAM clock speed.
- Integrated system memory, graphic frame memory and video frame memory.
- Supports 8MB up to 128 MB system memory.
- Supports 16-Mbit, 64-Mbit and 128-Mbit SDRAMs.
- Supports 8, 16, 32, 64, and 128 MB DIMMs.
- Supports buffered, non buffered, and registered DIMMs
- 4-line write buffers for CPU to DRAM and PCI to DRAM cycles.
- 4-line read prefetch buffers for PCI masters.
- Programmable latency
- Programmable timing for SDRAM parameters.
- Supports -8, -10, -12, -13, -15 memory parts
- Supports memory hole between 1MB and 8MB for PCI/ISA busses.
- 32-bit access, Autoprecharge & Power-down are not supported.

- **Enhanced 2D Graphics Controller**
- Supports pixel depths of 8, 16, 24 and 32 bit.
- Full BitBLT implementation for all 256 raster operations defined for Windows.
- Supports 4 transparent BLT modes - Bitmap Transparency, Pattern Transparency, Source Transparency and Destination Transparency.
- Hardware clipping
- Fast line draw engine with anti-aliasing.
- Fast triangle fill engine.
- Supports 4-bit alpha blended font for anti-aliased text display.
- Complete double buffered registers for pipelined operation.
- 64-bit wide pipelined architecture running at 100 MHz. Hardware clipping

- **CRT Controller**
- Integrated 135MHz triple RAMDAC allowing for 1280 x 1024 x 75Hz display.
- 8-, 16-, 24-bit pixels.
- Interlaced or non-interlaced output.

- **Video Input port**
- Accepts video inputs in CCIR 601/656 mode.
- Optional 2:1 decimator
- Stores captured video in off setting area of the onboard frame buffer.
- HSYNC and B/T generation or lock onto external video timing source.

- **Video Pipeline**
- Two-tap interpolative horizontal filter.
- Two-tap interpolative vertical filter.
- Color space conversion (RGB to YUV and YUV to RGB).
- Programmable window size.
- Chroma and color keying for integrated video overlay.

DESCRIPTION

- **TFT Interface**
- Programmable panel size up to 1024 by 1024 pixels.
- Support for VGA and SVGA active matrix TFT flat panels with 9, 12, 18-bit interface (1 pixel per clock).
- Support for XGA and SXGA active matrix TFT flat panels with 2 x 9-bit interface (2 pixels per clock).
- Programmable image positionning.
- Programmable blank space insertion in text mode.
- Programmable horizontal and vertical image expansion in graphic mode.
- Two fully programmable PWM (Pulse Width Modulator) signals to adjust the flat panel brightness and contrast.
- Supports **PanelLink**TM high speed serial transmitter externally for high resolution panel interface.

- **PCI Controller**
- Compliant with PCI 2.1 specification.
- Integrated PCI arbitration interface. Up to 3 masters can connect directly. External logic allows for greater than 3 masters.
- Translation of PCI cycles to ISA bus.
- Translation of ISA master initiated cycle to PCI.
- Support for burst read/write from PCI master.
- PCI clock is 1/2, 1/3 or 1/4 CPU bus clock.

- **ISA master/slave**
- Generates the ISA clock from either 14.318MHz oscillator clock or PCI clock
- Supports programmable extra wait state for ISA cycles
- Supports I/O recovery time for back to back I/O cycles.
- Fast Gate A20 and Fast reset.
- Supports the single ROM that C, D, or E. blocks shares with F block BIOS ROM.
- Supports flash ROM.
- Supports ISA hidden refresh.
- Buffered DMA & ISA master cycles to reduce bandwidth utilization of the PCI and Host bus.

- **Local Bus interface**
- Multiplexed with ISA/DMA interface.
- Low latency asynchronous bus
- 16-bit data bus with word steering capability.
- Programmable timing (Host clock granularity)
- 4 Programmable Flash Chip Select.
- 8 Programmable I/O Chip Select.
- I/O device timing (setup & recovery time) programmable
- Supports 32-bit Flash burst.
- 2-level hardware key protection for Flash boot block protection.
- Supports 2 banks of 32MB flash devices with boot block shadowed to 0x000F0000.
- Reallocatable Memory space Windows

- **Ultra DMA-33 IDE Interface**
- Compatible with EIDE (ATA-2).
- Backward compatibility with IDE (ATA-1).
- Supports up to 4 IDE devices
- Supports PIO and Bus Master IDE
- Supports up to Mode 5 Timings
- Concurrent channel operation (PIO & DMA modes) - 4 x 32-Bit Buffer FIFO per channel
- Support for 11.1/16.6 MB/s, I/O Channel Ready PIO data transfers.
- Supports 13.3/16.6/33 MB/s DMA data transfers
- Bus Master with scatter/gather capability
- Multi-word DMA support for fast IDE drives
- Individual drive timing for all four IDE devices
- Supports both legacy & native IDE modes
- Supports hard drives larger than 528MB
- Support for CD-ROM and tape peripherals

- **Integrated Peripheral Controller**
- 2X8237/AT compatible 7-channel DMA controller.
- 2X8259/AT compatible interrupt Controller. 16 interrupt inputs - ISA and PCI.
- Three 8254 compatible Timer/Counters.
- Co-processor error support logic.
- Supports external RTC (Not in Local Bus Mode).

- **PCMCIA interface**
- Support one PCMCIA 2.0 / JEIDA 4.1 68-pin standard PC Card Socket.
- Power Management support.
- Support PCMCIA/ATA specifications.
- Support I/O PC Card with pulse-mode interrupts.
- Provides an ExCA™ implementation to PCMCIA 2.0 / JEIDA 4.1 standards.

- **USB Interface**
- USB 1.1 compatible.
- Open HCI 1.0 compliant.
- User configurable RootHub.
- Support for both LowSpeed and HighSpeed USB devices.
- No bi-directionnal or Tri-state busses.
- No level sensitive latches.
- System Management Interrupt pin support
- Hooks for legacy device support.

- **Keyboard interface**
- Fully PC/AT+ compatible

- **Mouse interface**
- Fully PS/2 compatible

- **Serial interface**
- 15540 compatible
- Programmable word length, stop bits, parity.
- 16-bit programmable baud rate generator.
- Interrupt generator.
- Loop-back mode.
- 8-bit scratch register.
- Two 16-bit FIFOs.
- Two DMA handshake lines.

Parallel port
- All IEEE Standard 1284 protocols supported: Compatibility, Nibble, Byte, EPP, and ECP modes.
- 16 bytes FIFO for ECP.

- **Power Management**
- Four power saving modes: On, Doze, Standby, Suspend.
- Programmable system activity detector
- Supports Intel & Cyrix SMM and APM.
- Supports STOPCLK.
- Supports IO trap & restart.
- Independent peripheral time-out timer to monitor hard disk, serial & parallel port.
- 128K SM_RAM address space from 0xA0000 to 0xB0000

- **JTAG**
- Boundary Scan compatible IEEE1149.1.
- Scan Chain control.
- Bypass register compatible IEEE1149.1.
- ID register compatible IEEE1149.1.
- RAM BIST control.

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ExCA is a trademark of PCMCIA / JEIDA.

PanelLink is a trademark of SiliconImage, Inc

1 GENERAL DESCRIPTION

At the heart of the STPC Atlas is an advanced processor block that includes a powerful x86 processor core along with a 64-bit SDRAM controller, advanced 64-bit accelerated graphics and video controller, a high speed PCI local-bus controller and Industry standard PC chip set functions (Interrupt controller, UltraDMA IDE Controller, Interval timer and ISA bus).

The STPC Atlas has in addition, a TFT output, a Video Input, a Local Bus interface, PCMCIA and super I/O features including USB host hub.

The STPC Atlas makes use of a tightly coupled Unified Memory Architecture (UMA), where the same memory array is used for CPU main memory and graphics frame-buffer. This means a reduction in total system memory for system performances that are equal to that of a comparable frame buffer and system memory based system, and generally much better, due to the higher memory bandwidth allowed by attaching the graphics engine directly to the 64-bit processor host interface running at the speed of the processor bus rather than the traditional PCI bus.

The 64-bit wide memory array provides the system with 800MB/s peak bandwidth. This allows for higher resolution screens and greater color depth. The processor bus runs at 133Mhz further increasing “standard” bandwidth by at least a factor of two.

The ‘standard’ PC chipset functions (DMA, interrupt controller, timers, power management logic) are integrated together with the x86 processor core; additional low bandwidth functions such as communication ports are accessed by the STPC Atlas via an internal ISA bus.

The PCI bus is the main data communication link to the STPC Atlas chip. The STPC Atlas translates appropriate host bus I/O and Memory cycles onto the PCI bus. It also supports the generation of Configuration cycles on the PCI bus. The STPC Atlas, as a PCI bus agent (host bridge class), fully complies with PCI specification 2.1. The chip-set also implements the PCI mandatory header registers in Type 0 PCI configuration space for easy porting of PCI aware system BIOS. The device contains a PCI arbitration function for three external PCI devices.

Graphics functions are controlled through the on-chip SVGA controller and the monitor display is produced through the 2D graphics display engine.

This Graphics Engine is tuned to work with the host CPU to provide a balanced graphics system with a low silicon area cost. It performs limited graphics drawing operations which include hardware acceleration of text, bitblts, transparent blts and fills. The results of these operations change the contents of the on-screen or off-screen frame buffer areas of SDRAM memory. The frame buffer can occupy a space up to 4 Mbytes anywhere in the physical main memory.

The maximum graphics resolution supported is 1280x1024 in 16 Million colours at 75Hz refresh rate and is VGA and SVGA compatible. Horizontal timing fields are VGA compatible while the vertical fields are extended by one bit to accommodate above display resolution.

To generate the TFT output, the STPC Atlas extracts the digital video stream before the RAM-DAC and reformats it to the TFT format. The height and width of the flat panel are programmable through configuration registers up to a size of 1024 by 1024.

By default, lower resolution images cover only a part of the larger TFT panel. The STPC Atlas allows to expand the image vertically and horizontally in text mode by inserting programmable blank pixels. It allows expantion of the image vertically and horizontally in graphics mode by replicating pixels. The replication of J times every K pixel is independently programmable in the vertical and horizontal directions.

PanelLink™ is a proprietary interconnect protocol defined by Silicon Image, Inc. It consists of a transmitter that takes parallel video/graphics data from the host LCD graphics controller and transmits it serially at high speed to the receiver which controls the TFT panel. The TFT interface is designed to support the connection of this control signal to the **PanelLink**™ transmitter.

The STPC Atlas PCMCIA controller has been specifically designed to provide the interface with PC-Cards which contain additional memory or I/O and provides an **ExCA**™ implementation to PCMCIA 2.0 / JEIDA 4.1 standards.

GENERAL DESCRIPTION

The power management control facilities include socket power control, insertion/removal capability, power saving with Windows inactivity, NCS controlled Chip Power Down, together with further controls for 3.3v suspend with Modem Ring Resume Detection.

The need for system configuration jumpers is eliminated by providing address mapping support for PCMCIA 2.0 / JEIDA 4.1 PC-Card memory together with address windowing support for I/O space.

The STPC Atlas implements a multi-function parallel port. The standard PC/AT compatible logical address assignments for LPT1, LPT2 and LPT3 are supported.

The parallel port can be configured for any of the following 3 modes and supports the IEEE Standard 1284 parallel interface protocol standards as follow:

-Compatibility Mode (Forward channel, standard)

-Nibble Mode (Reverse channel, PC compatible)

-Byte Mode (Reverse channel, PS/2 compatible)

The STPC Atlas BGA package has 516 balls, but this is not sufficient for all the integrated functions, therefore some features are sharing the same balls and can not be used at the same time. The STPC Atlas configuration is done by 'strap options'. It is a set of pull-up or pull-down resistors on the memory data bus, checked on reset, which auto-configure the STPC Atlas.

We can distinguish three main blocks,***independently configurable***. The ISA block, the Local Bus block and the PCI/PC Card block.

From the first two blocks, we can activate either the ISA bus and some IPC additionnal features, or the Local bus, the parallel port and the second serial interface.

From the third block, we can activate either the PCI bus, or the PC Card interface (PCMCIA).

The STPC Atlas core is compliant with the Advanced Power Management (APM) specification to provide a standard method by which the BIOS can control the power used by personal computers. The Power Management Unit module (PMU) controls the power consumption providing a comprehensive set of features that control the power usage and supports compliance with the United States Environmental Protection Agency's Energy Star Computer Program. The PMU provides following hardware structures to assist the software in managing the power consumption by the system.

- System Activity Detection.

- 3 power-down timers detecting system inactivity:
  - Doze timer (short durations).
  - Stand-by timer (medium durations).
  - Suspend timer (long durations).

- House-keeping activity detection.

- House-keeping timer to cope with short bursts of house-keeping activity while dozing or in stand-by state.

- Peripheral activity detection.

- Peripheral timer detecting peripheral inactivity

- SUSP# modulation to adjust the system performance in various power down states of the system including full power on state.

- Power control outputs to disable power from different planes of the board.

Lack of system activity for progressively longer periods of time is detected by the three power down timers. These timers can generate SMI interrupts to CPU so that the SMM software can put the system in decreasing states of power consumption. Alternatively, system activity in a power down state can generate SMI interrupt to allow the software to bring the system back up to full power on state. The chip-set supports up to three power down states described above, these correspond to decreasing levels of power savings.

Power down puts the STPC Atlas into suspend mode. The processor completes execution of the current instruction, any pending decoded instructions and associated bus cycles. During the suspend mode, internal clocks are stopped. Removing power down, the processor resumes instruction fetching and begins execution in the instruction stream at the point it had stopped. Because of the static nature of the core, no internal data is lost.

An industry standard EIDE (ATA 2) controller is built in to the STPC Atlas and connected internally via the PCI bus.

The STPC Atlas has three additionnal features ; USB, GPIO, JTAG.

Figure 1-1. Functionnal description.

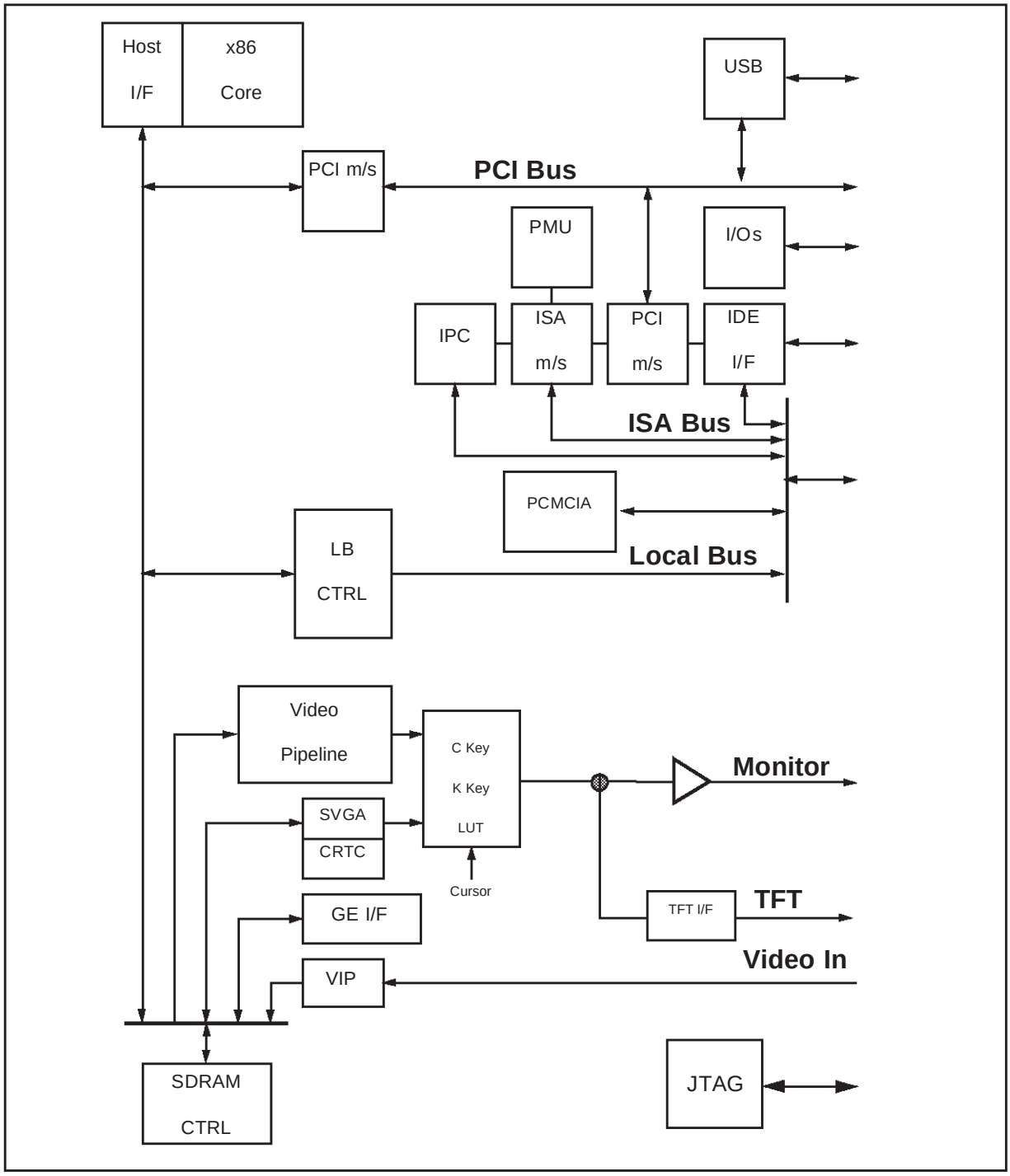


Figure 1-2. Typical PC oriented Application

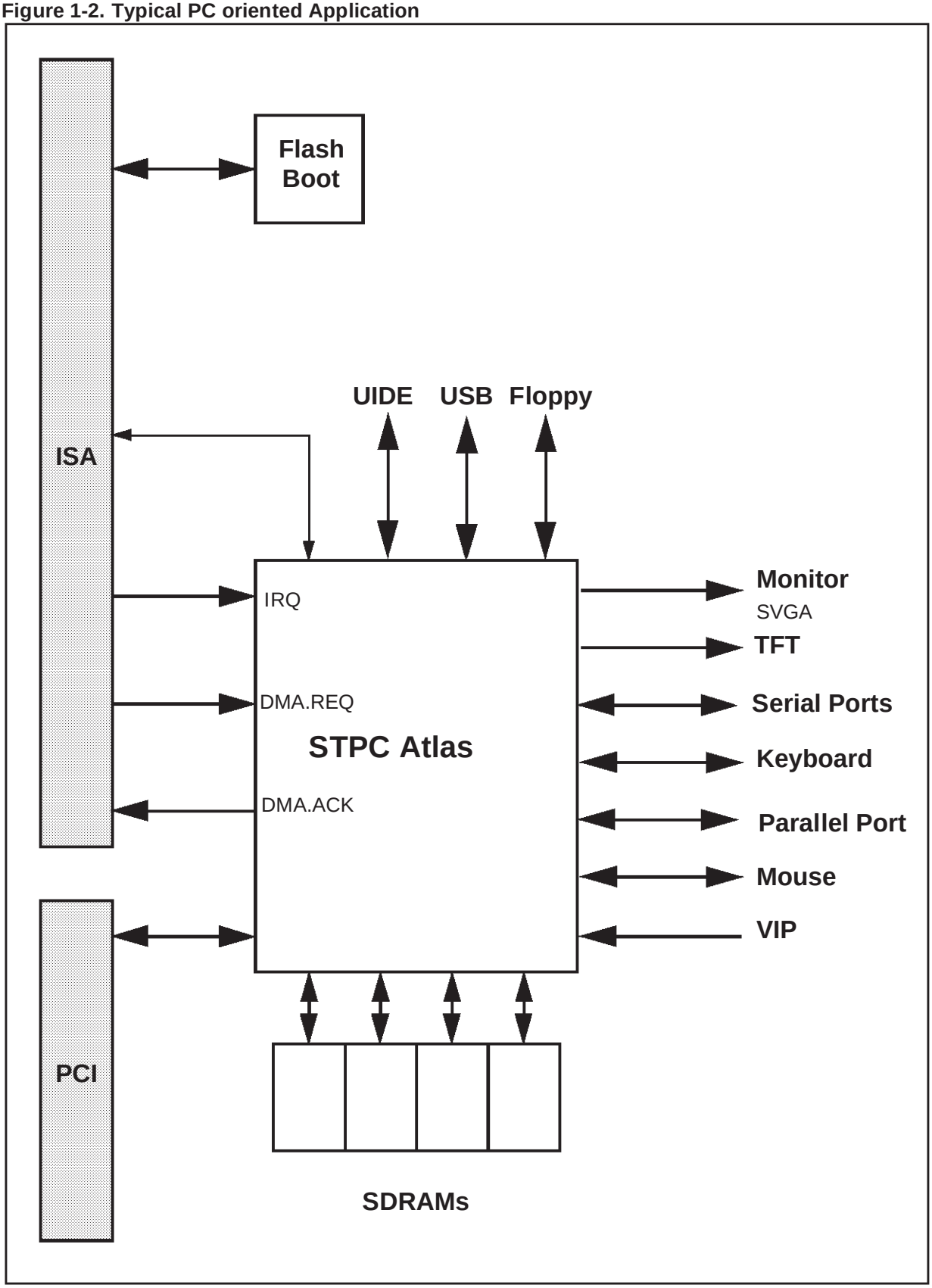
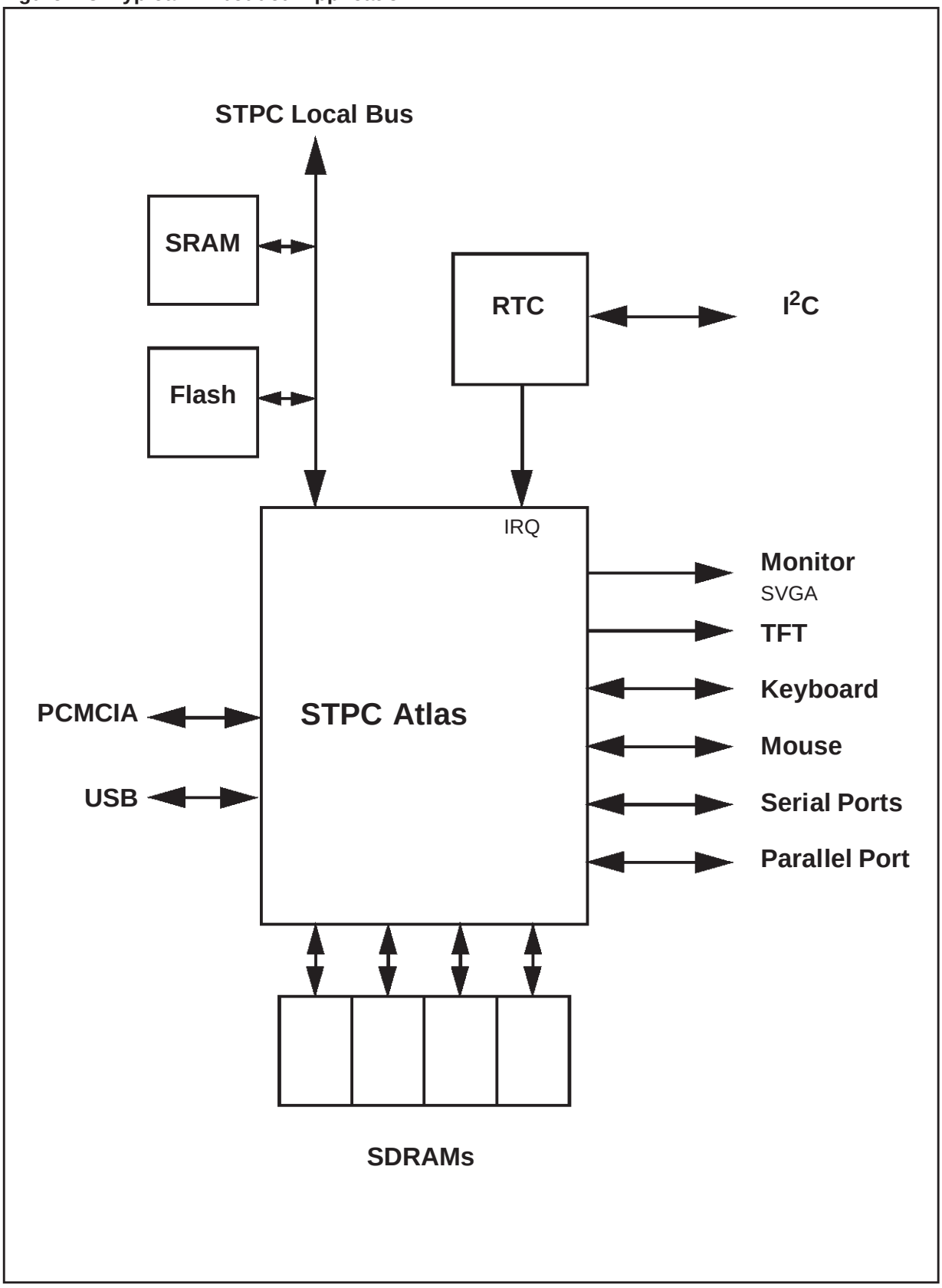


Figure 1-3. Typical Embedded Application



2 STRAP OPTION

This chapter defines the STPC Atlas Strap Options and their location. Some strap options are left programmable for future versions of silicon.

Memory Data Lines	Refer to	Designation	Location	Actual Settings	Set to '0'	Set to '1'
MD0	-	Reserved	-	-	-	-
MD1	-	Reserved	-	1	-	-
MD2	HCLK	Speed	Index 5F,bit 6	User defined	See Section 2.1.4	
MD3		Speed	Index 5F,bit 7	User defined		
MD4	PCI Clock	PCI_CLKO Divisor	Index 4A,bit 1	User defined	See Section 2.1.1	
MD5	Memory Clock	MCLK Synch	Index 4A,bit 2	User defined	Unsynch	Synch
MD6	PCICLK	PCICKLO Programming	Index 4A,bit 6	User defined	See Section 2.1.1	
MD7			Index 4A,bit 7	User defined		
MD8	Mode Select	ISA/PCMCIA/Local Bus	Index 4A,bit 3	User defined	See Section 2.1.1	
MD9			Index 4A,bit 3	User defined		
MD10	-	*Reserved*	Index 4B,bit 2	Pull down	-	-
MD11	-	*Reserved*	Index 4B,bit 3	Pull up	-	-
MD12	-	*Reserved*	Index 4B,bit 4			
MD13		*Reserved*	Index 4B,bit 5			
MD14	CPU Clock	CPUCLK Multiplication	Index 4B,bit 6	Uder defined	See Section 2.1.2	
MD15	-	*Reserved*	-	Pull up	-	-
MD16		*Reserved*	-	Pull up	-	-
MD17	PCI Clock	PCI_CLKO Divisor	Index 4A,bit 0	User defined	See Section 2.1.1	
MD18	Host Clock[1]	HCLK Pad Direction	Index 4C,bit 2	User defined	External	Internal
MD19	Memory Clock	MCLK Pad Direction	Index 4C,bit 3	User defined	External	Internal
MD20	DOT Clock	DCLK Pad Direction	Index 4C,bit 4	User defined	External	Internal
MD21		Reserved	Index 5F,bit 0	Pull up	-	-
MD22	-	*Reserved*	-	-	-	-
MD23	-	Reserved	Index 5F,bit 2	Pull up	-	-
MD24	HCLK	HCLK PLL Speed	Index 5F,bit 3	User defined	See Section 2.1.4	
MD25			Index 5F,bit 4	User defined		
MD26			Index 5F,bit 5	User defined		
MD27	-	Reserved	-	-	-	-
MD28	-	Reserved	-	-	-	-
MD29	-	Reserved	-	-	-	-
MD30	-	Reserved	-	-	-	-
MD31	-	Reserved	-	-	-	-
MD32	-	Reserved	-	-	-	-
MD33	-	Reserved	-	-	-	-
MD34	-	Reserved	-	-	-	-
MD35	-	Reserved	-	-	-	-
MD 36	Local Bus	Boot Device Selection	4B,bit 0	User defined	8 bit	16 bit
MD 37		Reserved		Pull up		
MD 38		Reserved		Pull up		
MD 39		Reserved		Pull up		
MD 40	CPU Clock	CPUCLK Multiplication	Index 4B,bit 7	User defined	See Section 2.1.2	

Note 1; When read, these strap options return an inverted value.

Memory Data Lines	Refer to	Designation	Location	Actual Settings	Set to '0'	Set to '1'
MD 41	-	*Reserved*	-	Pull down	-	-
MD 42	-	*Reserved*	-	Pull up	-	-
MD 43	-	*Reserved*	-	Pull down	-	-
MD 44	-	*Reserved*	-	-	-	-
MD 45	-	*Reserved*	-	-	-	-
MD 46	-	Reserved	-	-	-	-
MD 47		-	-	-	-	-
MD 48	-	*Reserved*	-	-	-	-
MD 49	-	*Reserved*	-	-	-	-
MD 50	Internal UART2	Enable / Disable	4C,bit0	User defined	Disable	Enable
MD 51	Internal UART1	Enable / Disable	4C,bit1	User defined	Disable	Enable
MD 52	Internal KB & Mouse	Enable / Disable	4C,bit6	User defined	Disable	Enable
MD 53	Internal Parallel Port	Enable / Disable	4C,bit7	User defined	Disable	Enable
Note 1; When read, these strap options return an inverted value.						

2.1 STRAP OPTION REGISTER DESCRIPTION

2.1.1 STRAP REGISTER 0 INDEX 4AH (STRAP0)

Bits 7-6 This bit reflcts the **value sampled on MD[7:6] pins** and controlles the PCICLK Programming.The PLL setup will vary depending on the PCICLK frequency;

MD[7]	MD[6]	Description
0	0	PCICLK frequency between 16 & 32 MHz
0	1	PCICLK frequency between 32 & 64 MHz
1	0	PCICLK frequency between 64 & 133 MHz
1	1	PCICLK frequency greater than 133 MHz

Bit 5 *Reserved*

Bits 4-3 ISA I/F, Local Bus I/F or PCMCIA I/F. These bits reflects the **values sampled on MD[9:8] pin** and sets whether the ISA I/F, Local Bus I/F or the PCMCIA I/F is available at the device I/F. The detail is shown in .

MD[9]	MD[8]	Description
0	0	ISA Mode Enabled
0	1	PCMCIA Mode Enabled
1	0	Local Bus Mode Enabled
1	1	*Reserved*

Bit 2 This bit reflects the**value sampled on MD[5] pin** and controls the MCLK/HCLK Synchronization. When MCLK and HCLK frequency are the same, this bit when 1 unifies HCLK and MCLK and it will improve system performances.

Bit 1 This bit reflects the**value sampled on MD[4] pin** and controls the PCICLKO division. It works with MD[17]. refer to Section 2.1.1 bit 0 for a detailed description.

Bits 0 This bit reflects the value sampled on MD[17] pin and controls the PCI clock output as follows:

MD[4]	MD[17]	Description
0	0	*Reserved*
0	1	PCI clock output = HCLK / 4
1	0	PCI clock output = HCLK / 3
1	1	PCI clock output = HCLK / 2

2.1.2 STRAP REGISTER 1 INDEX 4BH (STRAP1)

Bits 7-6 These bits reflect the**values sampled on MD[40],MD[14] pins** and sets the CPU Clock Multiplication:

MD[40]	MD[14]	Description
0	0	X1 Mode
0	1	*Reserved*
1	0	*Reserved*
1	1	X2 Mode

Bits 5-1 *Reserved*

Bit 0 These bits reflect the **values sampled on MD[36]** and determines the Local Bus Boot device width.

Bit 0	Description
0	8 Bit Boot Device supported
1	16 Bit Boot Device supported

2.1.3 STRAP REGISTER 2 INDEX 4CH (STRAP2)

Bit 7, This bit reflects the **value sampled on MD[53] pin** and determines whether the internal Parallel Port Controller is used.

Bit 7	Description
0	Internal Parallel Port Controller
1	External Parallel Port Controller

Bit 6, This bit reflects the **value sampled on MD[52] pin** and determines whether the internal Keyboard controller is used.

Bit 6	Description
0	Internal Keyboard Controller
1	External Keyboard Controller

Bit 5 See Section 2.1.4 , Bit 2

Bit 4, This bit reflects the **value sampled on MD[20] pin** and controls the Dot clock (DCLK) source as follows:.

Bit 4	Description
0	Input
1	Output. DCLK pin is an output and is connected to the internal frequency synthesizer output.

Bit 3, This bit reflects the **value sampled on MD[19] pin** and controls the Memory clock output (MCLKO) source as follows:.

Bit 3	Description
0	External. MCLKO pin is tristated.
1	Internal. MCLKO pin is an output and is connected to the internal frequency synthesizer output.

Bit 2, This bit reflects the **value sampled on MD[18] pin** and controls the Host/CPU clock source as follows:.

Bit 1, This bit reflects the **value sampled on MD[51] pin** and determines whether the internal UART1 is enabled.

Bit 2	Description
0	External. HCLK pin is an input.
1	Internal. HCLK pin is an output and is connected to the internal frequency synthesizer output.

Bit 1	Description
0	Internal UATR1 is disabled
1	Internal UART1 is enabled

Bit 0, This bit reflects the **value sampled on MD[50] pin** and determines whether the internal UART2 is enabled.

Bit 0	Description
0	Internal UATR2 is disabled
1	Internal UART2 is enabled

2.1.4 HCLK PLL STRAP REGISTER 0 INDEX 5FH (HCLK_STRAP0)

Bits 7-3 These pins reflect the**value sampled on MD[3:2] and MD[26:24] pins** respectively and control the Host clock frequency synthesizer as follows:

MD[3]	MD[2]	MD[26]	MD[25]	MD[24]	HCLK Speed
0	0	0	0	0	25 MHz
0	0	0	0	1	50 MHz
0	0	0	1	0	60 MHz
0	0	0	1	1	66 MHz
0	1	0	0	1	75 MHz
1	0	0	1	1	90 MHz
1	0	0	1	1	100 MHz
1	1	1	1	1	133 MHz

Bit 2-0 *Reserved*

3 PIN DESCRIPTION

3.1. INTRODUCTION

The STPC Atlas integrates most of the functionalities of the PC architecture. Therefore, many of the traditional interconnections between the host PC microprocessor and the peripheral devices are totally internal to the STPC Atlas. This offers improved performance due to the tight coupling of the processor core and it's peripherals. As a result many of the external pin connections are made directly to the on-chip peripheral functions.

Figure 3-1 shows the STPC Atlas's external interfaces. It defines the main busses and their function. Table 3-1 describes the physical implementation listing signal types and their functionalities. Table 3-2 provides a full pin listing and description.

Table 3-4 provides a full listing of the STPC Atlas package pin location physical connection. Please refer to the pin allocation drawing for reference.

Due to the number of pins available for the package, and the number of functional I/Os, some pins have several functions, selectable by strap option on Reset. Table 3-3 provides a summary of these pins and their functions.

Table 3-1. Signal Description

Group name	Qty	
Basic Clocks, Reset & Xtal (SYS)		19
SDRAM Controller(SDRAM)		95
PCI Controller		51
ISA Controller	80	100
IDE Controller	34	
Local Bus I/F	67	
PCMCIA Controller	62	
VGA Controller (VGA) / I^2C		10
Video Input Port		11
TFT output		24
USB Controller		6
Serial Interface		16
Keyboard/Mouse Controller		4
Parallel Port		18
GPIO Signals		16
JTAG Signals		5
Miscelaneous		2
Miscellaneous		3
Grounds		96
V_{DD} 3.3V/2.5V		36
Reserved		4
Total Pin Count		516

Figure 3-1. STPC Atlas External Interfaces

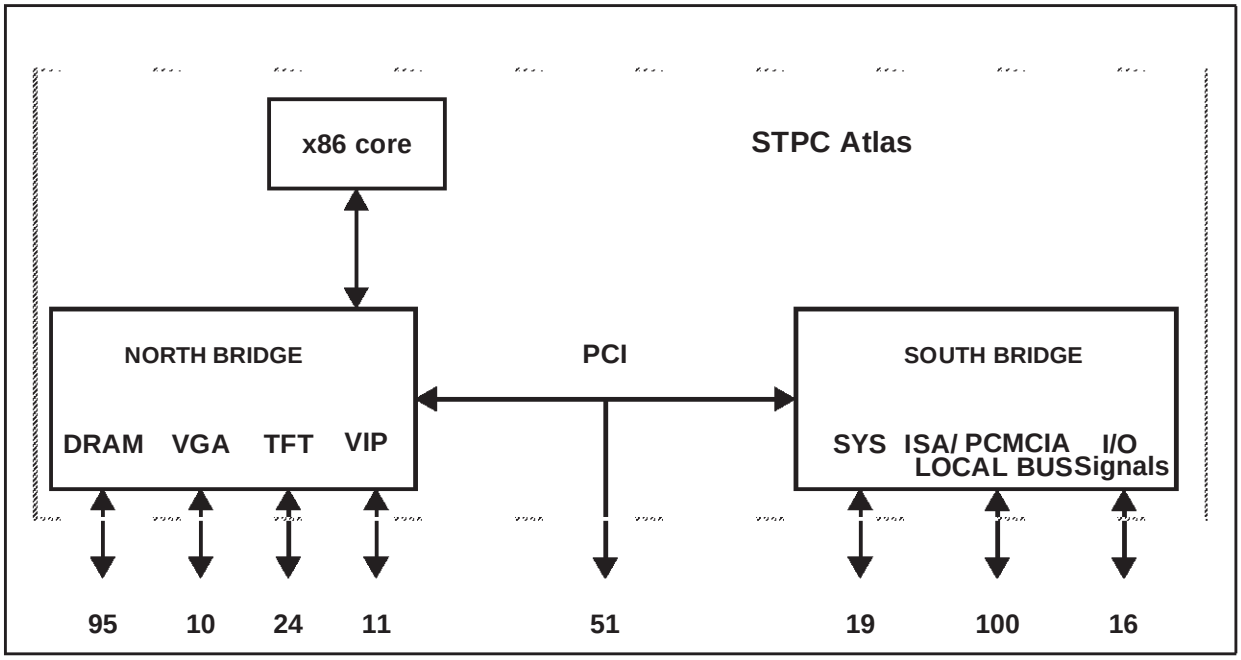


Table 3-2. Definition of Signal Pins

Signal Name	Dir	Description	Qty
BASIC CLOCKS AND RESETS			
SYSRSTI#[2]	I	System Reset / Power good	1
SYSRSTO#[2]	O	Reset Output to System	1
XTALI	I	14.3MHz Crystal Input	1
XTALO	O	14.3MHz Crystal Output	1
PCI_CLKI[2]	I	33MHz PCI Input Clock	1
PCI_CLKO	O	33MHz PCI Output Clock	1
ISA_CLK, ISA_CLK2X	O	ISA Clock x1 and x2 (also Multiplexer Select Line For IPC)	2
OSC14M[2]	O	ISA bus synchronisation clock	1
HCLK[2]	I/O	100 / 133MHz Host Clock (Test pin)	1
DEV_CLK[2]	O	24MHz Peripheral Clock	1
DCLK[2]	I/O	135MHz Dot Clock	1
V_{DD}_xxx_PLL[1]		Power Supply for PLL Clocks (2.5V)	7
MEMORY CONTROLLER			
MCLKI	I	Memory Clock Input	1
MCLKO	O	Memory Clock Output	1
CS#[1:0]	O	DIMM Chip Select	2

Note[1]; These pins are must be connected to the 2.5Vpower supply. They **must not** be connected to the 3.3V supply.

Note[2]; Denotes that the pin is V_{5T} (see Section Table 4-1.)

Note [3]; see Table 3-4 for V_{5T} signals

Table 3-2. Definition of Signal Pins

Signal Name	Dir	Description	Qty
CS#[3]/MA[12]/BA[1]	O	DIMM Chip Select/ Memory Address/ Bank Address	1
CS#[2]/MA[11]	O	DIMM Chip Select/ Bank Address	1
BA[0]	O	Bank Address	
MA[10:0]	O	Memory Row & Column Address	12
RAS#[1:0]	O	Row Address Strobe	2
CAS#[1:0]	O	Column Address Strobe	2
MWE#	O	Write Enable	1
MD[63:0][3]	I/O	Memory Data	64
CS#[3:0]	O	DIMM CHIP SELECT	4
DQM[7:0]	O	DATA INPUT/OUTPUT MASK	8
PCI INTERFACE			
AD[31:0][2]	I/O	Address / Data	32
BE[3:0][2]	I/O	Bus Commands / Byte Enables	4
FRAME#[2]	I/O	Cycle Frame	1
TRDY#[2]	I/O	Target Ready	1
IRDY#[2]	I/O	Initiator Ready	1
STOP#[2]	I/O	Stop Transaction	1
DEVSEL#[2]	I/O	Device Select	1
PAR[2]	I/O	Parity Signal Transactions	1
PERR#	I/O	Parity Error	1
SERR#[2]	O	System Error	1
LOCK#[2]	I	PCI Lock	1
PCI_REQ#[2:0][2]	I	PCI Request	3
PCI_GNT#[2:0][2]	O	PCI Grant	3
ISA BUS INTERFACE			
LA[23:17][2]	O	Unlatched Address	7
SA[19:0][2]	O	Latched Address	20
SD[15:0][2]	I/O	Data Bus	16
IOCHRDY[2]	I	I/O Channel Ready	1
ALE[2]	O	Address Latch Enable	1
BHE#[2]	O	System Bus High Enable	1
MEMR#[2], MEMW#[2]	I/O	Memory Read & Write	2
SMEMR#[2], SMEMW#[2]	O	System Memory Read and Write	2
IOR#[2], IOW#[2]	I/O	I/O Read and Write	2

Note[1]; These pins are must be connected to the 2.5Vpower supply. They **must not** be connected to the 3.3V supply.
Note[2]; Denotes that the pin is V_{5T} (see Section Table 4-1.)
Note [3]; see Table 3-4 for V_{5T} signals

Table 3-2. Definition of Signal Pins

Signal Name	Dir	Description	Qty
MASTER#[2]	I	Add On Card Owns Bus	1
MCS16#[2], IOCS16#[2]	I	Memory Chip Select 16, I/O Chip Select 16	2
REF#[2]	I	Refresh Cycle	1
AEN[2]	O	Address Enable	1
IOCHCK#[2]	I	I/O Channel Check (ISA)	1
RTCRW#[2]	O	RTC Read / Write#	1
RTCDS#[2]	O	RTC Data Strobe	1
RTCAS#[2]	O	RTC Address Strobe	1
RMRTCCS#[2]	O	ROM / RTC Chip Select	1
GPIOCS#[2]	I/O	General Purpose Chip Select	1
IRQ_MUX[3:0][2]	I	Multiplexed Interrupt Request	4
DACK_ENC[2:0][2]	O	DMA Acknowledge	3
DREQ_MUX[1:0][2]	I	Multiplexed DMA Request	2
TC[2]	O	ISA Terminal Count	1
PCI_INT[3:0][2]	I	PCI Interrupt Request	4
ISAOE#[2]	I	SELECT BETWEEN ISA OR IDE	1
KBCS#[2]	I/O	KEYBOARD CHIP SELECT	1
ZWS#[2]	I	ZERO WAIT STATE	1
IDE CONTROLLER			
DD[15:0]	I/O	Data Bus	16
DA[2:0]	O	Address Bus	3
PCS3#/PCS1#/SCS3#/ SCS1#	O	Primary / secondary Chip Select	4
DIORDY	O	Data Io Ready	1
PIRQ[2]/SIRQ[2]	I	Primary / Secondary Interupt Request	2
PDRQ[2]/SDRQ[2]	I	Primary / Secondary Drive Drq	2
PDACK#[2]/SDACK#[2]	O	Primary / Secondary Drive Dack	2
PDIOR#[2]/SDIOR#[2]	O	Primary / Secondary IO Read	2
PDIOW#[2]/SDIOW#[2]	O	Primary / Secondary IO Write	2
LOCAL BUS INTERFACE			
PA[24:0][2]	O	Address Bus [24:0]	25
PD[15:0][2]	I/O	Data Bus [15:0]	16
PRD#	O	Peripheral Read Data	1

Note[1]; These pins are must be connected to the 2.5Vpower supply. They **must not** be connected to the 3.3V supply.
Note[2]; Denotes that the pin is V_{5T} (see Section Table 4-1.)
Note [3]; see Table 3-4 for V_{5T} signals

Table 3-2. Definition of Signal Pins

Signal Name	Dir	Description	Qty
PRDY#[2]	I	Ready	1
PWR#[1:0][2]	O	Memory and I/O Write signals	2
PRD#[1:0][2]	O	Memory and I/O Read signals	2
FCS#[1:0][2]	O	Flash Memory Chip Select	2
IOCS#[7:0][2]	O	I/O Chip Select	8
PBE#[1:0]	O	PERIPHERAL BYTE ENABLES	2
FCS_0H#[2]	O	Bank 0 Upper Chip Select	1
FCS_0L#[2]	O	Bank 0 Lower Chip Select	1
FCS_1H#[2]	O	Bank 1 Upper Chip Select	1
FCS_1L#[2]	O	Bank 1 Lower Chip Select	1
IRQ_MUX[3:0][1)]	I/O	Muxed Interrupt Lines	4
PCMCIA INTERFACE			
RESET	O	Reset	1
A	O	Address Bus	26
D	I/O	Data Bus	16
IORD#, IOWR#	O	I/O Read and Write	2
WP / IOIS16#	I	DMA Request // Write Protect // I/O Size is 16 bit	1
BVD2, BVD1	I	Battery Voltage Detect	2
READY# / IREQ#	I	Busy / Ready# // Interrupt Request	1
WAIT#	I	Wait	1
OE#	O	Output Enable // DMA Terminal Count	1
WE#	O	Write Enable // DMA Terminal Count	1
REG#	O	DMA Acknowledge // Register	1
CD2#, CD1#	I	Card Detect	2
CE2#, CE1#	O	Card Enable	2
VCC5_EN	O	Power Switch control : 5v power	1
VCC3_EN	O	Power Switch control : 3.3v power	1
VPP_PGM	O	Power Switch control : Program power	1
VPP_VCC	O	Power Switch control : VCC power	1
GPI#	I	General Purpose Input	1
VGA CONTROLLER			
RED, GREEN, BLUE	O	Red, Green, Blue	3

Note[1]; These pins are must be connected to the 2.5Vpower supply. They **must not** be connected to the 3.3V supply.
Note[2]; Denotes that the pin is V_{5T} (see Section Table 4-1.)
Note [3]; see Table 3-4 for V_{5T} signals

PIN DESCRIPTION

Table 3-2. Definition of Signal Pins

Signal Name	Dir	Description	Qty
VSYNC[2]	I/O	Vertical Sync	1
HSYNC[2]	I/O	Horizontal Sync	1
VREF_DAC	I	DAC Voltage reference	1
RSET	I	Resistor Set	1
COMP	I	Compensation	1
DDC[1:0][2]	I/O	Display Data Channel Serial Link (See also SCL/SDA Signals)	2
VIDEO INPUT PORT			
VCLK[2]	I/O	27-33MHz VIDEO INPUT PORT CLOCK	1
VIN[7:0][2]	I	Video Input Data Bus	8
ODD_EVEN#[2]	I/O	Video Input/tv Output Odd/even Field	1
VCS[2]	I/O	Video Input/tv Output Horizontal Sync	1
TFT INTERFACE			
R[5:0], G[5:0], B[5:0]	O	Red, Green, Blue	18
FPLINE	O	Horizontal Sync	1
FPFRAME	O	Vertical Sync	1
DE	O	Data Enable	1
ENAVDD	O	Enable Vdd of flat panel	1
ENVCC	O	Enable Vcc of flat panel	1
PWM	O	PWM back-light control	1
USB INTERFACE			
OC	I	Over Current Detect	1
USBDPLS[0][1], USBDMNS[0][1]	I/O	Universal Serial Bus Data 0.	2
USBDPLS[1][1], USBDMNS[1][1]	I/O	Universal Serial Bus Port 1	2
POWERON[2)]	O	USB power supply lines	1
SERIAL CONTROLLER			
CTS0#[2], CTS1#[2]	I	Clear to send, MSR[4] status bit	2
DCD0#[2], DCD1#[2]	I	Data Carrier detect, MSR[7] status bit	2
DSR0#[2], DSR1#[2]	I	Data set ready, MSR[5] status bit.	2
DTR0#, DTR1#	O	Data terminal ready, MSR[0] status bit	2

Note[1]; These pins are must be connected to the 2.5Vpower supply. They **must not** be connected to the 3.3V supply.
Note[2]; Denotes that the pin is V_{5T} (see Section Table 4-1.)
Note [3]; see Table 3-4 for V_{5T} signals

Table 3-2. Definition of Signal Pins

Signal Name	Dir	Description	Qty
RI0#[2], RI1#	I	Ring indicator, MSR[6] status bit	2
RTS0#, RTS1#	O	Request to send, MSR[1] status bit	2
RXD0[2], RXD1[2]	I	Receive data, Input Serial Input	2
TXD0, TXD1	O	Transmit data, Serial Output	2
KEYBOARD & MOUSE INTERFACE			
KBDATA[2], MDATA[2]	I/O	Keyboard & Mouse Data Line	2
KBCLK[2], MCLK[2]	I/O	Keyboard & Mouse Clock Line	2
PARALLEL PORT			
PE[2]	I	Paper End	1
SLCT[2]	I	SELECT	1
BUSY#[2]	I	BUSY	1
ERR#[2]	I	ERROR	1
ACK#[2]	I	Acknowledge	1
PDDIR#[2]	O	Parallel Device Direction	1
STROBE#[2]	O	PCS / STROBE#	1
INIT#[2]	O	INIT	1
AUTPFDX#[2]	O	Automatic Line Feed	1
SLCTIN#[2]	O	SELECT IN	1
PPD[7:0][2]	I/O	Data Bus	8
I2C INTERFACE			
SCL / DDC[1][2]	I/O	I C Interface - Clock / Can be used for VGA DDC[1] signal	See VGA
SDA / DDC[0][2]	I/O	I C Interface - Data / Can be used for VGA DDC[0] signal	See VGA
GPIO SIGNALS			
GPIO[15:0][2]	I/O	General Purpose IOs	16
JTAG			
TCLK[2]	I	Test Clock	1
TRST[2]	I	Test Reset	1
TDI[2]	I	Test Data Input	
TMS[2]	I	Test Mode Set	1

Note[1]; These pins are must be connected to the 2.5Vpower supply. They **must not** be connected to the 3.3V supply.
Note[2]; Denotes that the pin is V_{5T} (see Section Table 4-1.)
Note [3]; see Table 3-4 for V_{5T} signals

Table 3-2. Definition of Signal Pins

Signal Name	Dir	Description	Qty
TDO[2]	O	Test Data output	1
MISCELLANEOUS			
SCAN_ENABLE	I	Test Pin - Reserved	1
COL_SEL[2]	O	Color Select	1
SPKRD[2]	O	Speaker Device Output	1

Note[1]; These pins are must be connected to the 2.5Vpower supply. They **must not** be connected to the 3.3V supply.
Note[2]; Denotes that the pin is V_{5T} (see Section Table 4-1.)
Note [3]; see Table 3-4 for V_{5T} signals

Note 1.

Note 2.

3.2. SIGNAL DESCRIPTIONS

3.2.2 BASIC CLOCKS AND RESETS

SYSRSTI# *System Reset/Power good.* This input is low when the reset switch is depressed. Otherwise, it reflects the power supply's power good signal. PWGD is asynchronous to all clocks, and acts as a negative active reset. The reset circuit initiates a hard reset on the rising edge of PWGD.

SYSRSTO# *Reset Output to System.* This is the system reset signal and is used to reset the rest of the components (not on Host bus) in the system. The ISA bus reset is an externally inverted buffered version of this output and the PCI bus reset is an externally buffered version of this output.

XTALI *14.3MHz Crystal Input*
XTALO *14.3MHz Crystal Output.* These pins are the 14.318 MHz crystal input; This clock is used as the reference clock for the internal frequency synthesizer to generate the HCLK and CLK24M.
A 14.318 MHz Series Cut Quartz Crystal should be connected between these two pins. Balance capacitors of 15 pF should also be added. In the event of an external oscillator providing the master clock signal to the STPC Atlas device, the TTL signal should be provided on XTALO.

PCI_CLKI *33MHz PCI Input Clock*

This signal must be connected to a clock generator and is usually connected to PCI_CLKO.

PCI_CLKO *33MHz PCI Output Clock.* This is the master PCI bus clock output

ISA_CLK *ISA Clock Output (also Multiplexer Select Line For IPC).* This pin produces the Clock signal for the ISA bus. It is also used with ISA_CLK2X as the multiplexor control lines for the Interrupt Controller Interrupt input lines. This is a divided down version of the PCICLK or OSC14M.

ISA_CLKX2 *ISA Clock Output (also Multiplexer Select Line For IPC).* This pin produces a signal at twice the frequency of the ISA bus Clock signal. It is also used with ISA_CLK as the multiplexor control lines for the Interrupt Controller Interrupt input lines.

CLK14M *ISA bus synchronisation clock.* This is the buffered 14.318 Mhz clock to the ISA bus. This clock also provides the reference clock to the frequency synthesizer that generates GCLK2X and DCLK.

HCLK *Host Clock.* This is the host 1X clock. Its frequency can vary from 50 to 75 MHz. All host transactions and PCI transactions are synchronized to this clock. Host transactions executed by the DRAM controller are also driven by this clock.

DEV_CLK *24MHz Peripheral Clock (floppy drive).* This 24MHZ signal is provided as a convenience for the system integration of a Floppy Disk driver function in an external chip.

DCLK *135MHz Dot Clock.* This is the dot clock, which drives graphics display cycles. Its frequency can be as high as 135 MHz, and it is required to have a worst case duty cycle of 60-40. For further details, refer to Section 3.1.3. bit 4.

3.2.3 MEMORY INTERFACE

MCLKI *Memory Clock Input.* This clock is driving the SDRAM controller, the graphics engine and display controller. This input should be a buffered version of the MCLKO signal with the track lengths between the buffer and the pin matched with the track lengths between the buffer and the Memory Banks.

MCLKO *Memory Clock Output.* This clock drives the Memory Banks on board and is generated from an internal PLL.

CS#[3]/MA[12]/BA[1] *Chip Select/ Memory Address/ Bank Address* This pin is CS#[3] in the case when 16Mbit devices are used. For all other densities, it becomes MA[12] when 2 internal banks devices are used and BA[1] when 4 internal bank devices are used.

MA[10:0] *Memory Address.* Multiplexed row and column address lines.

BA[0] *Memory Bank Address.*

CS#[1:0] *Chip Select* These signals are used to disable or enable device operation by masking or enabling all SDRAM inputs except MCLK, CKE, and DQM.

MD[63:0] *Memory Data.* This is the 64-bit memory data bus. If only half of a bank is populated, MD63-32 is pulled high, data is on MD31-0.
MD20-0 are also used as inputs at the rising edge of PWGD to latch in power-up configuration information into the ADPC strap registers.

RAS#[3:0] *Row Address Strobe.* There are 4 active low row address strobe outputs, one each for each bank of the memory. Each bank contains 4 or 8-Bytes of data. The memory controller allows half of a bank (4-Bytes) to be populated to enable memory upgrade at finer granularity.
The RAS# signals drive the SIMMs directly with-

out any external buffering. These pins are always outputs, but they can also simultaneously be inputs, to allow the memory controller to monitor the value of the RAS# signals at the pins.

CAS#[7:0] *Column Address Strobe.* There are 8 active low column address strobe outputs, one each for each Byte of the memory.
The CAS# signals drive the SIMMs either directly or through external buffers.
These pins are always outputs, but they can also simultaneously be inputs, to allow the memory controller to monitor the value of the CAS# signals at the pins.

MWE# *Write Enable.* Write enable specifies whether the memory access is a read (MWE# = H) or a write (MWE# = L). This single write enable controls all DRAMs. It can be externally buffered to boost the maximum number of loads (DRAM chips) supported.
The MWE# signals drive the SIMMs directly without any external buffering.

3.2.4 PCI INTERFACE

AD[31:0] *PCI Address/Data.* This is the 32-bit multiplexed address and data bus of the PCI. This bus is driven by the master during the address phase and data phase of write transactions. It is driven by the target during data phase of read transactions.

BE[3:0]# *Bus Commands/Byte Enables.* These are the multiplexed command and Byte enable signals of the PCI bus. During the address phase they define the command and during the data phase they carry the Byte enable information. These pins are inputs when a PCI master other than the STPC Atlas owns the bus and outputs when the STPC Atlas owns the bus.

FRAME# *Cycle Frame.* This is the frame signal of the PCI bus. It is an input when a PCI master owns the bus and is an output when STPC Atlas owns the PCI bus.

TRDY# *Target Ready.* This is the target ready signal of the PCI bus. It is driven as an output when the STPC Atlas is the target of the current bus transaction. It is used as an input when STPC Atlas initiates a cycle on the PCI bus.

IRDY# *Initiator Ready.* This is the initiator ready signal of the PCI bus. It is used as an output when the STPC Atlas initiates a bus cycle on the PCI bus. It is used as an input during the PCI cycles targeted to the STPC Atlas to determine when the current PCI master is ready to complete the current transaction.

STOP# *Stop Transaction.* STOP# is used to implement the disconnect, retry and abort protocol of the PCI bus. It is used as an input for the bus cycles initiated by the STPC Atlas and is used as an output when a PCI master cycle is targeted to the STPC Atlas.

DEVSEL# *Device Select.* This signal is used as an input when the STPC Atlas initiates a bus cycle on the PCI bus to determine if a PCI slave device has decoded itself to be the target of the current transaction. It is asserted as an output either when the STPC Atlas is the target of the current PCI transaction or when no other device asserts DEVSEL# prior to the subtractive decode phase of the current PCI transaction.

PAR *Parity Signal Transactions.* This is the parity signal of the PCI bus. This signal is used to guarantee even parity across AD[31:0], CBE[3:0]#, and PAR. This signal is driven by the master during the address phase and data phase of write transactions. It is driven by the target during data phase of read transactions. (Its assertion is identical to that of the AD bus delayed by one PCI clock cycle)

PERR# *Parity Error*

SERR# *System Error.* This is the system error signal of the PCI bus. It may, if enabled, be asserted for one PCI clock cycle if target aborts a STPC Atlas initiated PCI transaction. Its assertion by either the STPC Atlas or by another PCI bus agent will trigger the assertion of NMI to the host CPU. This is an open drain output.

LOCK# *PCI Lock.* This is the lock signal of the PCI bus and is used to implement the exclusive bus operations when acting as a PCI target agent.

PCI_REQ#[2:0] *PCI Request.* These pins are the three external PCI master request pins. They indicates to the PCI arbiter that the external agents desire use of the bus.

PCI_GNT#[2:0] *PCI Grant.* These pins indicate that the PCI bus has been granted to the master requesting it on its PCI_REQ#.

PCI_INT[3:0] *PCI Interrupt Request.* These are the PCI bus interrupt signals. They are to be encoded before connection to the STPC Atlas using ISACLK and ISACLKX2 as the input selection strobes.

3.2.5 LOCAL BUS

PA[24:0] *Address Bus Output.*

PD[15:0] *Data Bus.* This is the 16-bit data bus. D[7:0] is the LSB and PD[15:8] is the MSB.

PWR#[1:0] *Write Control output.* These are memory and I/O Write signals. PWR0# is used to write the LSB and PWR1# to write the MSB.

PRD#[1:0] *Read Control output.* These are memory and I/O Read signals. PWR0# is used to read the LSB and PWR1# to read the MSB.

PRDY# *Data Ready input.* This signal is used to create wait states on the bus. When low, it completes the current cycle.

FCS#[3:0] *Four Flash Memory Chip Select outputs.* These are the Programmable Chip Select signals for up to 4 banks of Flash memory (Banks 0 and 1, Upper and Lower).

IOCS#[7:0] *I/O Chip Select output.* These are the Programmable Chip Select signals for up to 4 external I/O devices.

IRQ_MUX#[3:0] *Multiplexed Interrupt Lines.*

3.2.6 ISA BUS INTERFACE

LA[23:17] *Unlatched Address.* These unlatched ISA Bus pins address bits 23-17 on 16-bit devices. When the ISA bus is accessed by any cycle initiated from the PCI bus, these pins are in output mode. When an ISA bus master owns the bus, these pins are tristated.

SA[19:0] *Unlatched Address.* These are the 20 low bits of the system address bus of ISA. These pins are used as an input when an ISA bus master owns the bus and are outputs at all other times.

SD[15:0] *I/O Data Bus (ISA).* These are the external ISA databus pins.

IOCHRDY *IO Channel Ready.* IOCHRDY is the IO channel ready signal of the ISA bus and is driven as an output in response to an ISA master cycle targeted to the host bus or an internal register of the STPC Atlas. The STPC Atlas monitors this signal as an input when performing an ISA cycle on behalf of the host CPU, DMA master or refresh.
ISA masters which do not monitor IOCHRDY are not guaranteed to work with the STPC Atlas since the access to the system memory can be considerably delayed due to CRT refresh or a write back cycle.

ALE *Address Latch Enable.* This is the address latch enable output of the ISA bus and is asserted by the STPC Atlas to indicate that LA23-17, SA19-0, AEN and SBHE# signals are valid. The ALE is driven high during refresh, DMA master or an ISA master cycles by the STPC Atlas.
ALE is driven low after reset.

BHE# *System Bus High Enable.* This signal, when asserted, indicates that a data Byte is being transferred on SD15-8 lines. It is used as an input when an ISA master owns the bus and is an output at all other times.

MEMR# *Memory Read.* This is the memory read command signal of the ISA bus. It is used as an input when an ISA master owns the bus and is an output at all other times.
The MEMR# signal is active during refresh.

MEMW# *Memory Write.* This is the memory write command signal of the ISA bus. It is used as an input when an ISA master owns the bus and is an output at all other times.

SMEMR# *System Memory Read.* The STPC Atlas generates SMEMR# signal of the ISA bus only when the address is below one MByte or the cycle is a refresh cycle.

SMEMW# *System Memory Write.* The STPC Atlas generates SMEMW# signal of the ISA bus only when the address is below one MByte.

IOR# *I/O Read.* This is the IO read command signal of the ISA bus. It is an input when an ISA master owns the bus and is an output at all other times.

IOW# *I/O Write.* This is the IO write command signal of the ISA bus. It is an input when an ISA master owns the bus and is an output at all other times.

MASTER# *Add On Card Owns Bus.* This signal is active when an ISA device has been granted bus ownership.

MCS16# *Memory Chip Select16.* This is the decode of LA23-17 address pins of the ISA address bus without any qualification of the command signal lines. MCS16# is always an input. The STPC Atlas ignores this signal during IO and refresh cycles.

IOCS16# *IO Chip Select16.* This signal is the decode of SA15-0 address pins of the ISA address bus without any qualification of the command signals. The STPC Atlas does not drive IOCS16# (similar to PC-AT design). An ISA master access to an internal register of the STPC Atlas is executed as an extended 8-bit IO cycle.

REF# *Refresh Cycle.* This is the refresh command signal of the ISA bus. It is driven as an output when the STPC Atlas performs a refresh cycle on the ISA bus. It is used as an input when an ISA master owns the bus and is used to trigger a refresh cycle.
The STPC Atlas performs a pseudo hidden re-

fresh. It requests the host bus for two host clocks to drive the refresh address and capture it in external buffers. The host bus is then relinquished while the refresh cycle continues on the ISA bus.

AEN *Address Enable.* Address Enable is enabled when the DMA controller is the bus owner to indicate that a DMA transfer will occur. The enabling of the signal indicates to IO devices to ignore the IOR#/IOW# signal during DMA transfers.

IOCHCK# *IO Channel Check.* IO Channel Check is enabled by any ISA device to signal an error condition that can not be corrected. NMI signal becomes active upon seeing IOCHCK# active if the corresponding bit in Port B is enabled.

GPIOCS# *I/O General Purpose Chip Select 1.* This output signal is used by the external latch on ISA bus to latch the data on the SD[7:0] bus. The latch can be use by PMU unit to control the external peripheral devices to power down or any other desired function.
This pin is also serves as a strap input during reset.

RTCRW# *Real Time Clock RW#.* This pin is used as RTCRW#. This signal is asserted for any I/O write to port 71h.

RTCDS# *Real Time Clock DS.* This pin is used as RTCDS. This signal is asserted for any I/O read to port 71h.

RTCAS# *Real time clock address strobe.* This signal is asserted for any I/O write to port 70h.

RMRTCCS# *ROM/Real Time clock chip select.* This pin is a multi-function pin. This signal is asserted if a ROM access is decoded during a memory cycle. It should be combined with MEMR# or MEMW# signals to properly access the ROM. During an IO cycle, this signal is asserted if access to the Real Time Clock (RTC) is decoded. It should be combined with IOR# or IOW# signals to properly access the real time clock.

IRQ_MUX[3:0] *Multiplexed Interrupt Request.* These are the ISA bus interrupt signals. They are to be encoded before connection to the STPC Atlas using ISACLK and ISACLKX2 as the input selection strobes.
Note that IRQ8B, which by convention is connected to the RTC, is inverted before being sent to the interrupt controller, so that it may be connected directly to the IRQ# pin of the RTC.

ISAOE# *Bidirectional OE Control.* This signal controls the $\overline{OE}$ signal of the external transceiver that connects the IDE DD bus and ISA SA bus.

KBCS# *Keyboard Chip Select.* This signal is asserted if a keyboard access is decoded during a I/O cycle.

ZWS# *Zero Wait State.* This signal, when asserted by addressed device, indicates that current cycle can be shortened.

DACK_ENC[2:0] *DMA Acknowledge.* These are the ISA bus DMA acknowledge signals. They are encoded by the STPC Atlas before output and should be decoded externally using ISACLK and ISACLKX2 as the control strobes.

DREQ_MUX[1:0] *ISA Bus Multiplexed DMA Request.* These are the ISA bus DMA request signals. They are to be encoded before connection to the STPC Atlas using ISACLK and ISACLKX2 as the input selection strobes.

TC *ISA Terminal Count.* This is the terminal count output of the DMA controller and is connected to the TC line of the ISA bus. It is asserted during the last DMA transfer, when the Byte count expires.

3.2.7 PCMCIA INTERFACE

RESET *Card Reset.* This output forces a hard reset to a PC Card.

A[25:0] *Address Bus.* These are the 25 low bits of the system address bus of the PCMCIA bus. These pins are used as an input when an PCMCIA bus owns the bus and are outputs at all other times.

D[15:0] *I/O Data Bus (PCMCIA).* These are the external PCMCIA databus pins.

IORD# *I/O Read.* This output is used with REG# to gate I/O read data from the PC Card, (only when REG# is asserted).

IOWR# *I/O Write.* This output is used with REG# to gate I/O write data from the PC Card, (only when REG# is asserted).

WP *Write Protect.* This input indicates the status of the Write Protect switch (if fitted) on memory PC Cards (asserted when the switch is set to write protect).

BVD1, BVD2 *Battery Voltage Detect.* These inputs will be generated by memory PC Cards that include batteries and are an indication of the condition of the batteries. BVD1 and BVD2 are kept asserted high when the battery is in good condition.

READY#/BUSY#/IREQ# *Ready/busy/Interupt request.* This input is driven low by memory PC Cards to signal that their circuits are busy processing a previous write command.

WAIT# *Bus Cycle Wait.* This input is driven by the PC Card to delay completion of the memory or I/O cycle in progress.

OE# *Output Enable.* OE# is an active low output which is driven to the PC Card to gate Memory Read data from memory PC Cards.

WE#/PRGM# *Write Enable.* This output is used by the host for gating Memory Write data. WE# is also used for memory PC Cards that have programmable memory.

REG# *Attribute Memory Select.* This output is inactive (high) for all normal accesses to the Main Memory of the PC Card. I/O PC Cards will only respond to IORD# or IOWR# when REG# is active (low). Also see Section 3.2.10

CD1#, CD2# *Card Detect.* These inputs provide for the detection of correct card insertion. CD#1 and CD#2 are positioned at opposite ends of the connector to assist in the detection process. These inputs are internally grounded on the PC Card therefore they will be forced low whenever a card is inserted in a socket.

CE1#, CE2# *Card Enable*. These are active low output signals provided from the PCIC. CE#1 enables even Bytes, CE#2 odd Bytes.

ENABLE# *Enable.* This output is used to activate/select a PC Card socket. ENABLE# controls the external address buffer logic.C card has been detected (CD#1 and CD#2 = '0').

ENIF# *ENIF*. This output is used to activate/select a PC Card socket.

EXT_DIR *EXternal Transreceiver Direction Control.* This output is high during a read and low during a write. The default power up condition is write (low). Used for both Low and High Bytes of the Data Bus.

VCC_EN#, VPP1_EN0, VPP1_EN1, VPP 2_EN0, VPP2_EN1 *Power Control.* Five output signals used to control voltages (VPP1, VPP2 and VCC) to a PC Card socket. Also see Section 13.7.5.

GPI# *General Purpose Input. This signal is hardwired to 1.*

3.2.8 IDE INTERFACE

DA[2:0] *Address.* These signals are connected to DA[2:0] of IDE devices directly or through a buffer. If the toggling of signals are to be masked during ISA bus cycles, they can be externally ORed with ISAOE# before being connected to the IDE devices.

DD[15:0] *Databus.* When the IDE bus is active, they serve as IDE signals DD[11:0]. IDE devices are connected to SA[19:8] directly and ISA bus is connected to these pins through two LS245 transceivers.

PCS1#, PCS3# *Primary Chip Select.* These signals are used as the active high primary master & slave IDE chip select signals. These signals must be externally ANDed with the ISAOE# signal before driving the IDE devices to guarantee it is active only when ISA bus is idle.

SCS1#, SCS3# *Secondary Chip Select.* These signals are used as the active high secondary master & slave IDE chip select signals. These signals must be externally ANDed with the ISAOE# signal before driving the IDE devices to guarantee it is active only when ISA bus is idle.

DIORDY *Busy/Ready.* This pin serves as IDE signal DIORDY.

PIRQ *Primary Interrupt Request.*
SIRQ *Secondary Interrupt Request.*
Interrupt request from IDE channels.

PDRQ *Primary DMA Request.*
SDRQ *Secondary DMA Request.*
DMA request from IDE channels.

PDACK# *Primary DMA Acknowledge.*
SDACK# *Secondary DMA Acknowledge.*
DMA acknoledge to IDE channels.

PDIOR#, PDIOW# *Primary I/O Read & Write.*
SDIOR#, SDIOW# *Secondary I/O Read & Write*
Primary & Secondary channel read & write.
Monitor Interface

3.2.9 USB Interface

OC *OVER CURRENT DETECT* This signal is used to monitor the status of the USB power supply lines of both devices. USB port are disabled when OC signal is asserted.

USBDPL0, USBDMNS0 *UNIVERSAL SERIAL BUS DATA 0* This signal pair comprises the differential data signal for USB port 0.

USBDPL1, USBDMNS1 *UNIVERSAL SERIAL BUS PORT 1* This signal pair comprises the differential data signal for USB port 1.

POWERON *USB power supply lines*

3.2.10 IPC

DACK_ENC[2:0] *DMA Acknowledge.* These are the ISA bus DMA acknowledge signals. They are encoded by the STPC Industrial before output and should be decoded externally using ISACLK and ISACLKX2 as the control strobes.

DREQ_MUX[1:0] *ISA Bus Multiplexed DMA Request.* These are the ISA bus DMA request signals. They are to be encoded before connection to the STPC Industrial using ISACLK and ISACLKX2 as the input selection strobes.

TC *ISA Terminal Count.* This is the terminal count output of the DMA controller and is connected to the TC line of the ISA bus. It is asserted during the last DMA transfer, when the Byte count expires.

3.2.11 KEYBOARD/MOUSE INTERFACE

KBCLK, *Keyboard Clock line.* Keyboard data is latched by the controller on each negative clock edge produced on this pin. The keyboard can be disabled by pulling this pin low by software control.

KBDATA, *Keyboard Data Line.* 11-bits of data are shifted serially through this line when data is being transferred. Data is synchronised to KBCLK.

MCLK, *Mouse Clock line.* Mouse data is latched by the controller on each negative clock edge produced on this pin. The mouse can be disabled by pulling this pin low by software control.

MDATA, *Mouse Data Line.* 11-bits of data are shifted serially through this line when data is being transferred. Data is synchronised to MCLK.

3.2.12 SERIAL INTERFACE

RXD0, RXD1 *Serial Input.* Data is clocked in using RCLK/16.

TXD0, TXD1 *Serial Output.* Data is clocked out using TCLK/16 (TCLK=BAUD#).

DCD0#, DCD1# *Input Data carrier detect.*

RI0#, RI1# *Input Ring indicator.*

DSR0#, DSR1# *Input Data set ready.*

CTS0#, CTS1# *Input Clear to send.*

RTS0#, RTS1# *Output Request to send.*

DTR0#, DTR1# *Output Data terminal read.*

3.2.13 PARALLEL PORT

PE *Paper End.* Input status signal from printer.

SLCT *Printer Select.* Printer selected input.

BUSY# *Printer Busy.*
Input status signal from printer.

ERR# *Error.* Input status signal from printer.

ACK# *Acknowledge.*
Input status signal from printer.

PDDIR# *Parallel Device Direction.*
Bidirectional control line output.

STROBE# *PCS/Strobe#.*
Data transfer strobe line to printer.

INIT# *Initialize Printer.* This output sends an initialize command to the connected printer.

AUTPFDX# *Automatic Line feed.* This output sends a command to the connected printer to automatically generate line feed on received carriage returns.

SLCTIN# *Select In.* Printer select output.

PPD[7-0] *Printer Data Lines* Data transfer lines to printer. Bidirectional depending on modes.

3.2.14 PCMCIA INTERFACE

RESET *Card Reset.* This output forces a hard reset to a PC Card.

A[25:0] *Address Bus.* These are the 25 low bits of the system address bus of the PCMCIA bus. These pins are used as an input when an PCMCIA bus owns the bus and are outputs at all other times.

D[15:0] *I/O Data Bus (PCMCIA).* These are the external PCMCIA databus pins.

IORD# *I/O Read.* This output is used with REG# to gate I/O read data from the PC Card, (only when REG# is asserted).

IOWR# *I/O Write.* This output is used with REG# to gate I/O write data from the PC Card, (only when REG# is asserted).

WP *Write Protect.* This input indicates the status of the Write Protect switch (if fitted) on memory PC Cards (asserted when the switch is set to write protect).

BVD1, BVD2 *Battery Voltage Detect.* These inputs will be generated by memory PC Cards that

include batteries and are an indication of the condition of the batteries. BVD1 and BVD2 are kept asserted high when the battery is in good condition.

READY#/BUSY#/IREQ# *Ready/busy/Interupt request.* This input is driven low by memory PC Cards to signal that their circuits are busy processing a previous write command.

WAIT# *Bus Cycle Wait.* This input is driven by the PC Card to delay completion of the memory or I/O cycle in progress.

OE# *Output Enable.* OE# is an active low output which is driven to the PC Card to gate Memory Read data from memory PC Cards.

WE#/PRGM# *Write Enable.* This output is used by the host for gating Memory Write data. WE# is also used for memory PC Cards that have programmable memory.

REG# *Attribute Memory Select.* This output is inactive (high) for all normal accesses to the Main Memory of the PC Card. I/O PC Cards will only respond to IORD# or IOWR# when REG# is active (low). Also see Section 3.2.10

CD1#, CD2# *Card Detect.* These inputs provide for the detection of correct card insertion. CD#1 and CD#2 are positioned at opposite ends of the connector to assist in the detection process. These inputs are internally grounded on the PC Card therefore they will be forced low whenever a card is inserted in a socket.

CE1#, CE2# *Card Enable*. These are active low output signals provided from the PCIC. CE#1 enables even Bytes, CE#2 odd Bytes.

ENABLE# *Enable.* This output is used to activate/select a PC Card socket. ENABLE# controls the external address buffer logic.C card has been detected (CD#1 and CD#2 = '0').

ENIF# *ENIF*. This output is used to activate/select a PC Card socket.

EXT_DIR *EXternal Transreceiver Direction Control.* This output is high during a read and low during a write. The default power up condition is write (low). Used for both Low and High Bytes of the Data Bus.

VCC_EN#, VPP1_EN0, VPP1_EN1, VPP 2_EN0, VPP2_EN1 *Power Control.* Five output signals used to control voltages (VPP1, VPP2 and VCC) to a PC Card socket. Also see Section 13.7.5.

GPI# *General Purpose Input. This signal is hardwired to 1.*

3.2.15 MONITOR INTERFACE

RED, GREEN, BLUE *RGB Video Outputs.* These are the 3 analog color outputs from the RAMDACs. These signals are sensitive to interference, therefore they need to be properly shielded.

VSYNC *Vertical Synchronisation Pulse.* This is the vertical synchronization signal from the VGA controller.

HSYNC *Horizontal Synchronisation Pulse.* This is the horizontal synchronization signal from the VGA controller.

VREF_DAC *DAC Voltage reference.* This pin is an input driving the digital to analog converters. This allows an external voltage reference source to be used.

RSET *Resistor Current Set.* This is the reference current input to the RAMDAC. Used to set the full-scale output of the RAMDAC.

COMP *Compensation.* This is the RAMDAC compensation pin. Normally, an external capacitor (typically 10nF) is connected between this pin and V_{DD} to damp oscillations.

DDC[1:0] *Direct Data Channel Serial Link.* These bidirectional pins are connected to CRTC register 3Fh to implement DDC capabilities. They conform to I^2C electrical specifications, they have open-collector output drivers which are internally connected to V_{DD} through pull-up resistors.

They can instead be used for accessing I C devices on board. DDC1 and DDC0 correspond to SCL and SDA respectively.

3.2.16 VIDEO INTERFACE

VCLK *Pixel Clock Input.* This signal is used to synchronise data being transfered from an external video device to either the frame buffer, or alternatively out the TV output in bypass mode. This pin can be sourced from STPC if no external VCLK is detected, or can be input from an external video clock source.

VIN[7:0] *YUV Video Data Input CCIR 601 or 656.* Time multiplexed 4:2:2 luminance and chrominance data as defined in ITU-R Rec601-2 and Rec656 (except for TTL input levels). This bus typically carries a stream of Cb,Y,Cr,Y digital video at VCLK frequency, clocked on the rising edge (by default) of VCLK.

3.2.17 FLAT PANEL INTERFACE SIGNALS

FPFRAME, *Vertical Sync. pulse Output.*

FPLINE, *Horizontal Sync. Pulse Output.*

DE, *Data Enable.*

R5-0, *Red Output.*

G5-0, *Green Output.*

B5-0, *Blue Output.*

ENAVDD *Enable VDD of Flat Panel.*

ENVCC *Enable VCC of Flat Panel.*

PWM *PWM Back-Light Control.*

3.2.18 MISCELLANEOUS

SPKRD *Speaker Drive.* This is the output to the speaker and is the AND of the counter 2 output with bit 1 of Port 61h and drives an external speaker driver. This output should be connected to a 7407 type high voltage driver.

SCAN_ENABLE *Reserved.* This pin is reserved for Test and Miscellaneous functions. It has to be set to '0' or connected to ground in normal operation.

3.1. SIGNAL DETAIL

The muxing between ISA, LOCAL BUS and PCMCIA is performed by external strap options. The resulting interface is then dynamically muxed with the UIDE Interface.

Table 3-3. Signals multiplexing on the same pin

ISA Pin Name	IDE Pin Name	Local Bus Pin Name	PCMCIA Pin Names
SA[19:8]	DD[11:0]		A[19:8]
SA[7:0]		PA[7:4],PRDY, IOCS#[2:0]	A[7:0]
SD[15:0]		PD[15:0]	D[15:0]
LA[23:20]	SCS3#,SCS1#, PCS3#,PCS1#		A[23:20]
LA[19:17]	DA[2:0]		Not used,A[25:24]
IOCHRDY	DIORDY		
RMRTCCS#,RTCAS, RTCRW#, RTCDS	DD[15:12]		
BHE#		PA[17]	OE#
ALE		PA[15]	
AEN		PA[16]	WAIT#
MEMR#		PA[14]	
MEMW#		PA[18]	
SMEMR#		PA[19]	VCC3_EN
SMEMW#		PBE#[1]	VPP_PGM
IOR#		PA[13]	IORD#
IOW#		PA[12]	IOWR#
MASTER#		PRD#	BVD1
MCS16#		PWR#	
IOCS16#		PBE#[0]	WP/IOIS16#
REF#		PA[11]	RESET
IOCHCK#		PA[10]	BVD2
GPIOCS#		PA[9]	VCC5_EN
ZWS#		PA[8]	GPI#
ISAOE#	ISAOE#	IOCS#[3]	
DREQ_MU#[1:0]		PA[21:20]	CE2#, CE1#
DACK_ENC [2:0]		PA[2:0]	
TC		PA[3]	
		PA[23]	VPP_VCC
		PA[24]	WE#
		IOCS#[7]	REG#
		IOCS#[6]	READY#
		IOCS#[5]	CD1#
		IOCS#[4]	CD2#

Table 3-4. Pinout.

Table 3-5.

Pin#	Pin Name
D15	SYSRSETI#
C15	SYSRSETO#
AF21	XTALI
AF22	XTALO
AF23	PCI_CLKI
AF24	PCI_CLKO
E15	ISA_CLK
A16	ISA_CLK2X
AB18	OSC14M
AB24	HCLK
AB25	DEV_CLK
AC18	DCLK
AF20	MCLKI
AF19	MCLKO
U5	MA[0]
V1	MA[1]
V2	MA[2]
V3	MA[3]
V4	MA[4]
V5	MA[5]
W1	MA[6]
W2	MA[7]
W3	MA[8]
W5	MA[9]
Y1	MA[10]
Y2	BA[0]
U3	RAS#[0]
U4	RAS#[1]
R5	CAS#[0]
T1	CAS#[1]
R4	MWE#
J4	MD[0][2]

Note[1]; This signal is multiplexed see Table 3-3

Note[2]; See Table 3-1

Table 3-5.

Pin#	Pin Name
J2	MD[1]
K5	MD[2]
K3	MD[3]
K1	MD[4]
L4	MD[5]
L2	MD[6]
M5	MD[7]
M3	MD[8]
M1	MD[9]
N4	MD[10]
N2	MD[11]
P1	MD[12]
P3	MD[13]
P5	MD[14]
R2	MD[15]
AA4	MD[16]
AB1	MD[17]
AB3	MD[18]
AC1	MD[19]
AC3	MD[20]
AD2	MD[21]
AF3	MD[22]
AE4	MD[23]
AF4	MD[24]
AD5	MD[25]
AF5	MD[26]
AC6	MD[27]
AF6	MD[28]
AC7	MD[29]
AE7	MD[30]
AB8	MD[31]
J3	MD[32]
J1	MD[33]
K4	MD[34]

Note[1]; This signal is multiplexed see Table 3-3

Note[2]; See Table 3-1

Table 3-5.

Pin#	Pin Name
K2	MD[35]
L5	MD[36]
L3	MD[37]
L1	MD[38]
M4	MD[39]
M2	MD[40]
N5	MD[41]
N3	MD[42]
N1	MD[43]
P2	MD[44]
P4	MD[45]
R1	MD[46]
R3	MD[47]
AA5	MD[48]
AB2	MD[49]
AB4	MD[50]
AC2	MD[51]
AD1	MD[52]
AE3	MD[53]
AD4	MD[54][2]
AC5	MD[55][2]
AB6	MD[56][2]
AE5	MD[57][2]
AB7	MD[58][2]
AD6	MD[59][2]
AE6	MD[60][2]
AD7	MD[61][2]
AF7	MD[62][2]
AC8	MD[63][2]
U1	CS#[0]
U2	CS#[1]
Y3	CS#[2]
Y4	CS#[3]/MA[12]/BA[1]
T2	DQM[0]

Note[1]; This signal is multiplexed see Table 3-3

Note[2]; See Table 3-1

Table 3-5.

Pin#	Pin Name
T4	DQM[1]
Y5	DQM[2]
AA2	DQM[3]
T3	DQM[4]
T5	DQM[5]
AA1	DQM[6]
AA3	DQM[7]
B3	AD[0]
A3	AD[1]
C4	AD[2]
B4	AD[3]
A4	AD[4]
D5	AD[5]
C5	AD[6]
B5	AD[7]
A5	AD[8]
D6	AD[9]
C6	AD[10]
B6	AD[11]
A6	AD[12]
E7	AD[13]
D7	AD[14]
C7	AD[15]
A9	AD[16]
E10	AD[17]
C10	AD[18]
B10	AD[19]
A10	AD[20]
E11	AD[21]
D11	AD[22]
C11	AD[23]
A11	AD[24]
E12	AD[25]

Note[1]; This signal is multiplexed see Table 3-3

Note[2]; See Table 3-1

Table 3-5.

Pin#	Pin Name
D12	AD[26]
C12	AD[27]
B12	AD[28]
A12	AD[29]
E13	AD[30]
D13	AD[31]
E6	BE[0]
B7	BE[1]
B9	BE[2]
B11	BE[3]
C9	FRAME#
E9	TRDY#
D9	IRDY#
B8	STOP#
A8	DEVSEL#
A7	PAR
D08	PERR#
E8	SERR#
C8	LOCK#
C14	PCI_REQ#[0]
B14	PCI_REQ#[1]
A14	PCI_REQ#[2]
A13	PCI_GNT#[0]
B13	PCI_GNT#[1]
C13	PCI_GNT#[2]
C20	LA[17][1]
B21	LA[18][1]
B20	LA[19][1]
E19	LA[20][1]
E18	LA[21][1]
C21	LA[22][1]
D19	LA[23][1]
P22	SA[0][1]

Note[1]; This signal is multiplexed see Table 3-3

Note[2]; See Table 3-1

Table 3-5.

Pin#	Pin Name
P23	SA[1][1]
P24	SA[2][1]
P25	SA[3][1]
P26	SA[4][1]
N26	SA[5][1]
N25	SA[6][1]
N24	SA[7][1]
N23	SA[8][1]
N22	SA[9][1]
M26	SA[10][1]
M25	SA[11][1]
M24	SA[12][1]
M23	SA[13][1]
M22	SA[14][1]
L26	SA[15][1]
L25	SA[16][1]
L24	SA[17][1]
L23	SA[18][1]
L22	SA[19][1]
K24	SD[0][1]
J26	SD[1][1]
J25	SD[2][1]
J24	SD[3][1]
K23	SD[4][1]
K22	SD[5][1]
H26	SD[6][1]
H25	SD[7][1]
H24	SD[8][1]
G26	SD[9][1]
G25	SD[10][1]
G24	SD[11][1]
J22	SD[12][1]
J23	SD[13][1]
F26	SD[14][1]

Note[1]; This signal is multiplexed see Table 3-3

Note[2]; See Table 3-1

Table 3-5.

Pin#	Pin Name
F25	SD[15][1]
F23	IOCHRDY[1]
D20	ALE[1]
K25	BHE#[1]
F24	MEMR#[1]
A22	MEMW#[1]
G23	SMEMR#[1]
E21	SMEMW#[1]
H22	IOR#[1]
E26	IOW#[1]
E25	MASTER#[1]
E24	MCS16#[1]
C22	IOCS16#[1]
G22	REF#[1]
E17	AEN[1]
A23	IOCHCK#[1]
U25	RTCRW#[1]
U26	RTCDS[1]
U24	RTCAS[1]
U23	RMRTCCS#[1]
D22	GPIOCS#[1]
D24	IRQ_MUX[0]
E23	IRQ_MUX[1]
C26	IRQ_MUX[2]
F22	IRQ_MUX[3]
A24	DACK_ENC[0]
C23	DACK_ENC[1][1]
B23	DACK_ENC[2][1]
D26	DREQ_MUX[0][1]
D25	DREQ_MUX[1][1]
B24	TC[1]
B15	PCI_INT[0]
A15	PCI_INT[1]
E14	PCI_INT[2]

Note[1]; This signal is multiplexed see Table 3-3

Note[2]; See Table 3-1

Table 3-5.

Pin#	Pin Name
D14	PCI_INT[3]
B16	ISAOE#[1]
B22	KBCS#
K26	ZWS#[1]
R23	PIRQ
R24	SIRQ
T22	PDRQ
T23	SDRQ
R25	PDACK#
R26	SDACK#
T25	PIOR#
T24	PIOW#
R22	SIOR#
T26	SIOW#
D18	PA[22]
C19	PA[23]
B19	PA[24]
A17	FCS_0H
B17	FCS_0L
C16	FCS_1H
E16	FCS_1L
D17	IOCS#[4]
C18	IOCS#[5]
B18	IOCS#[6]
C17	IOCS#[7]
AD8	RED
AF8	GREEN
AC9	BLUE
AB10	VSYNC
AF9	HSYNC
AB09	VREF_DAC

Note[1]; This signal is multiplexed see Table 3-3

Note[2]; See Table 3-1

Table 3-5.

Pin#	Pin Name
AD9	RSET
AE8	COMP
AB15	VCLK
AF16	VIN[0]
AE16	VIN[1]
AC16	VIN[2]
AB16	VIN[3]
AF17	VIN[4]
AE17	VIN[5]
AD17	VIN[6]
AB17	VIN[7]
AD18	ODD_EVEN#
AF18	VCS
AE10	R0[2]
AF10	R1[2]
AB11	R2
AD11	R3
AE11	R4
AF11	R5
AB12	G0[2]
AC12	G1[2]
AD12	G2
AE12	G3
AF12	G4
AB13	G5
AC13	B0[2]
AD13	B1[2]
AE13	B2
AF13	B3
AF14	B4
AE14	B5
AB14	FPLINE

Note[1]; This signal is multiplexed see Table 3-3

Note[2]; See Table 3-1

Table 3-5.

Pin#	Pin Name
AC14	FPFRAME
AF15	DE
AE15	ENAVDD
AD15	ENVCC
AC15	PWM
D21	OC
A20	USBDMNS[0]
A18	USBDMNS[1]
A21	USBDPLS[0]
A19	USBDPLS[1]
E20	POWERON
AC22	CTS0#
AC24	CTS1#
AD21	DCD0#
AE24	DCD1#
AC21	DSR0#
AD25	DSR1#
AD22	DTR0#
AC26	DTR1#
AD23	RI0#
AA22	RI1#
AE22	RTS0#
AC25	RTS1#
AB21	RXD0
AD26	RXD1
AE23	TXD0
AB23	TXD1
AD20	KBCLK
AB19	KBDATA
AC20	MDATA
AB20	MOUSE_CLK

Note[1]; This signal is multiplexed see Table 3-3

Note[2]; See Table 3-1

Table 3-5.

Pin#	Pin Name
AA23	PE
W24	SLCT
W23	BUSY
W25	ERR#
W26	ACK#
V22	PDDIR
V24	STROBE#
V25	INIT#
V26	AUTOPFD#
U22	SLCTIN#
Y22	PD[0]
AA24	PD[1]
AA25	PD[2]
AA26	PD[3]
Y24	PD[4]
Y25	PD[5]
Y26	PD[6]
W22	PD[7]
AC19	SCL / DDC[1]
AD19	SDA / DDC[0]
C2	GPIO[0]
C1	GPIO[1]
D3	GPIO[2]
D2	GPIO[3]
D1	GPIO[4]
E4	GPIO[5]
E3	GPIO[6]
E2	GPIO[7]
E1	GPIO[8]
F5	GPIO[9]
F4	GPIO[10]

Note[1]; This signal is multiplexed see Table 3-3

Note[2]; See Table 3-1

Table 3-5.

Pin#	Pin Name
F3	GPIO[11]
F2	GPIO[12]
G5	GPIO[13]
G4	GPIO[14]
G2	GPIO[15]
H2	TCLK
J5	TRST
H5	TDI
H3	TMS
H1	TDO
G1	SCAN_ENABLE
AD10	COL_SEL
C25	SPKRD
AD16	VDD_DCLKPLL
Y23	VDD_DEVCLKPLL
AE20	VDD_HCLKIPLL
AB26	VDD_HCLKOPLL
AE19	VDD_MCLKIPLL
AE18	VDD_MCLKOPLL
AE21	VDD_PCICLKPLL
F13	VDD_CORE
F15	VDD_CORE
F17	VDD_CORE
K6	VDD_CORE
M21	VDD_CORE
N6	VDD_CORE
P21	VDD_CORE
R6	VDD_CORE
U21	VDD_CORE
AA10	VDD_CORE

Note[1]; This signal is multiplexed see Table 3-3

Note[2]; See Table 3-1

Table 3-5.

Pin#	Pin Name
AA12	VDD_CORE
AA14	VDD_CORE
A02	VDD
A25	VDD
B1	VDD
B26	VDD
F7	VDD
F11	VDD
F20	VDD
G6	VDD
G21	VDD
H6	VDD
J21	VDD
K21	VDD
U6	VDD
V6	VDD
Y6	VDD
Y21	VDD
AA7	VDD
AA16	VDD
AA18	VDD
AA20	VDD
AE01	VDD
AE26	VDD
AF02	VDD
AF25	VDD
A1	gnd
A26	gnd
B2	gnd
B25	gnd
C3	gnd
C24	gnd

Note[1]; This signal is multiplexed see Table 3-3

Note[2]; See Table 3-1

Table 3-5.

Pin#	Pin Name
D4	gnd
D10	gnd
D16	gnd
D23	gnd
E5	gnd
E22	gnd
F6	gnd
F8	gnd
F9	gnd
F10	gnd
F12	gnd
F14	gnd
F16	gnd
F18	gnd
F19	gnd
F21	gnd
H4	gnd
H21	gnd
H23	gnd
J6	gnd
L6	gnd
L11	gnd
L12	gnd
L13	gnd
L14	gnd
L15	gnd
L16	gnd
L21	gnd
M6	gnd
M11	gnd
M12	gnd
M13	gnd
M14	gnd
M15	gnd

Note[1]; This signal is multiplexed see Table 3-3

Note[2]; See Table 3-1

Table 3-5.

Pin#	Pin Name
M16	gnd
N11	gnd
N12	gnd
N13	gnd
N14	gnd
N15	gnd
N16	gnd
N21	gnd
P6	gnd
P11	gnd
P12	gnd
P13	gnd
P14	gnd
P15	gnd
P16	gnd
R11	gnd
R12	gnd
R13	gnd
R14	gnd
R15	gnd
R16	gnd
R21	gnd
T6	gnd
T11	gnd
T12	gnd
T13	gnd
T14	gnd
T15	gnd
T16	gnd
T21	gnd
V21	gnd
V23	gnd
W4	gnd
W6	gnd

Note[1]; This signal is multiplexed see Table 3-3

Note[2]; See Table 3-1

Table 3-5.

Pin#	Pin Name
W21	gnd
AA6	gnd
AA8	gnd
AA9	gnd
AA11	gnd
AA13	gnd
AA15	gnd
AA17	gnd
AA19	gnd
AA21	gnd
AB5	gnd
AB22	gnd
AC4	gnd
AC11	gnd
AC17	gnd
AC23	gnd
AD3	gnd
AD24	gnd
AE2	gnd
AE25	gnd
AF1	gnd
AF26	gnd
AC10	*Reserved*
AE09	*Reserved*
G3	*Reserved*
F1	*Reserved*

Note[1]; This signal is multiplexed see Table 3-3

Note[2]; See Table 3-1

4 ELECTRICAL SPECIFICATIONS

4.1 INTRODUCTION

The electrical specifications in this chapter are valid for the STPC Atlas.

4.2 ELECTRICAL CONNECTIONS

4.2.1 Power/Ground Connections/Decoupling

Due to the high frequency of operation of the STPC Atlas, it is necessary to install and test this device using standard high frequency techniques. The high clock frequencies used in the STPC Atlas and its output buffer circuits can cause transient power surges when several output buffers switch output levels simultaneously. These effects can be minimized by filtering the DC power leads with low-inductance decoupling capacitors, using low impedance wiring, and by utilizing all of the VSS and VDD pins.

4.2.2 Unused Input Pins

All inputs not used by the designer and not listed in the table of pin connections in Section 2 should be connected either to VDD or to VSS. Connect active-high inputs to VDD through a 20 kΩ (±10%) pull-down resistor and active-low inputs to VSS and connect active-low inputs to VCC through a 20 kΩ (±10%) pull-up resistor to prevent spurious operation.

4.2.3 Reserved Designated Pins

Pins designated reserved should be left disconnected. Connecting a reserved pin to a pull-up resistor, pull-down resistor, or an active signal could cause unexpected results and possible circuit malfunctions.

4.3 ABSOLUTE MAXIMUM RATINGS

The following table lists the absolute maximum ratings for the STPC Atlas device. Stresses beyond those listed under Table 4-1 limits may cause permanent damage to the device. These are stress ratings only and do not imply that operation under any conditions other than those specified in section "Operating Conditions".

Exposure to conditions beyond those outlined in Table 4-1 may (1) reduce device reliability and (2) result in premature failure even when there is no immediately apparent sign of failure. Prolonged exposure to conditions at or near the absolute maximum ratings (Table 4-1) may also result in reduced useful life and reliability.

4.3.1 5V Tolerance

The STPC is capable of running with I/O systems that operate at 5V such as PCI and ISA devices. Certain pins of the STPC tolerate inputs up to 5.5V. Above this limit thecomponent is likely to sustain permanent damage.

All the pin that are V_{5T} have been denoted with a * besides the Signal Name in Table 2-1 .

Table 4-1. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Units
V_{DDx}	DC Supply Voltage	-0.3	4.0	V
V_{CORE}	DC Supply Voltage for Core	-0.3	2.75	V
V_I, V_O	Digital Input and Output Voltage	-0.3	VDD + 0.3	V
V_{5T}	5Volt Tolerance	-0.3	5.5	V
T_{STG}	Storage Temperature	-40	+150	°C
T_{OPER}	Operating Temperature	0	+70	°C
P_{TOT}	Maximum Power Dissipation (package)	-	4.8	W

4.4 DC CHARACTERISTICS

Table 4-2. DC Characteristics

VDD = 3.3V ±0.3V, Vcore = 2.5V ±0.25V, Tcase = -40 to 115°C unless otherwise specified

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{DD}	Operating Voltage		3.0	3.3	3.6	V
V_{CORE}	Operating Voltage		2.25	2.50	2.75	V
P_{DD}	Supply Power	V_{DD}=3.3V,V_{DD_CORE}=2.5V,H_{CLK}=133 MHz		2.0	2.6	W
H_{CLK}	Internal Clock	(Note 1)			133	MHz
V_{DAC}	DAC Voltage Reference		1.215	1.235	1.255	V
V_{OL}	Output Low Voltage	I_{Load} =1.5 to 8mA depending of the pin			0.5	V
V_{OH}	Output High Voltage	I_{Load} =-0.5 to -8mA depending of the pin	2.4			V
V_{ILD}	Input Low Voltage	Except XTALI	-0.3		0.8	V
		XTALI	-0.3		0.5	V
V_{IHD}	Input High Voltage	Except XTALI	2.1		V_{DD}+0.3	V
		XTALI	2.35		V_{DD}+0.3	V
I_{LK}	Input Leakage Current	Input, I/O	-5		5	µA
C_{IN}	Input Capacitance	(Note 2)				pF
C_{OUT}	Output Capacitance	(Note 2)				pF
C_{CLK}	Clock Capacitance	(Note 2)				pF

Notes:

1. MHz ratings refer to CPU clock frequency.

2. Not yet released.

Table 4-3. RAMDAC DC Specification

Symbol	Parameter	Min	Nom	Max
Vref	Voltage Reference	1.00V	1.12V	1.24V
INL	Integrated Non Linear Error	-	-	2 lsb
DNL	Differentiated Non Linear Error	-	-	1lsb
FS	Full Scale	-	-	20mA
FSR	Full Scale Range	14.00 mA	16.50mA	19.00 mA
LSB	Least Significant Byte Size	54uA	63uA	72uA
Zero	Zero Scale @ 7.5IRE Mode	0.95mA	1.44mA	1.90mA
Compare	DAC to DAC matching	-	-	+/- 5%

4.5 AC CHARACTERISTICS

Table 4-4 through Table 4-18 list the AC characteristics including output delays, input setup requirements, input hold requirements and output float delays. These measurements are based on the measurement points identified in Figure 4-1. The rising clock edge reference level VREF , and other reference levels are shown in Table 4-4 below for the STPC Atlas. Input or output signals must cross these levels during testing.

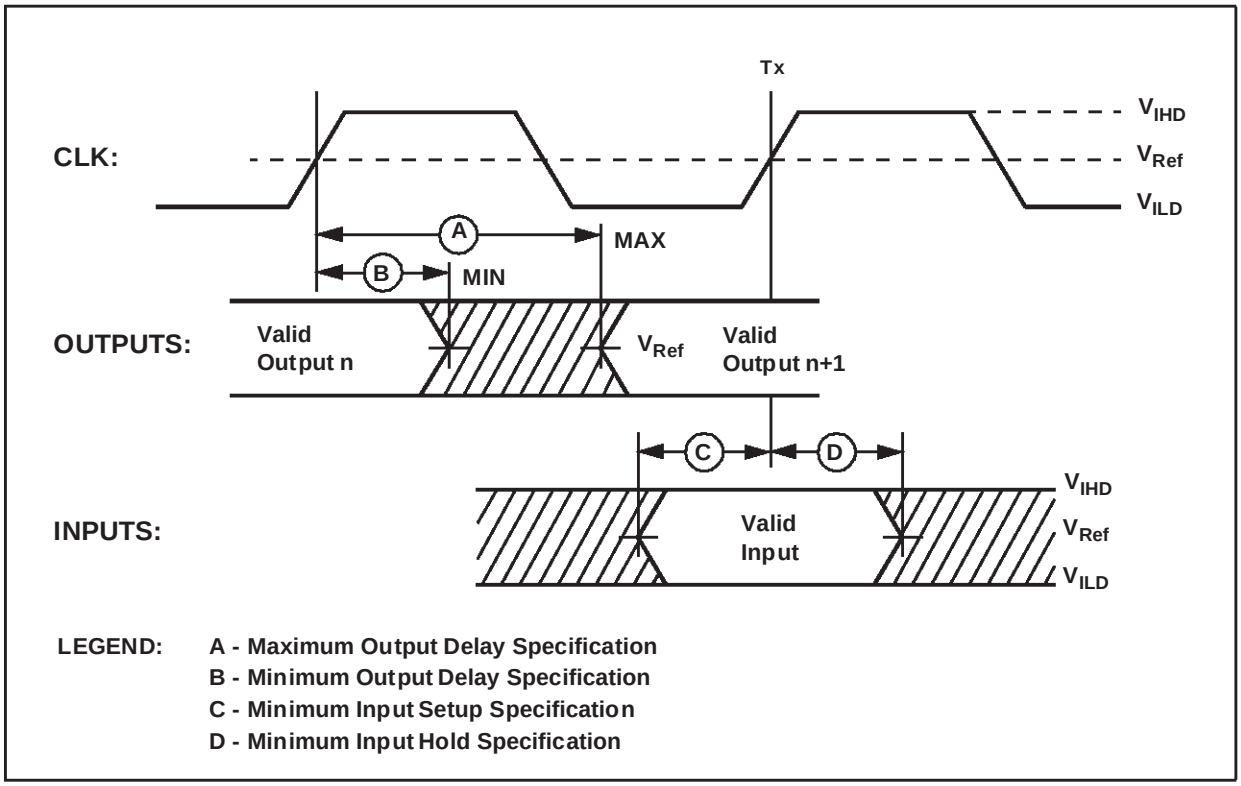
Figure 4-1 shows output delay (A and B) and input setup and hold times (C and D). Input setup and hold times (C and D) are specified minimums, defining the smallest acceptable sampling window a synchronous input signal must be stable for correct operation.

Table 4-4. Drive Level and Measurement Points for Switching Characteristics

Symbol	Value	Units
V_{REF}	1.5	V
V_{IHD}	2.5	V
V_{ILD}	0.0	V

Note: Refer to Figure 4-1.

Figure 4-1. Drive Level and Measurement Points for Switching Characteristics



4.5.1 POWER ON SEQUENCE

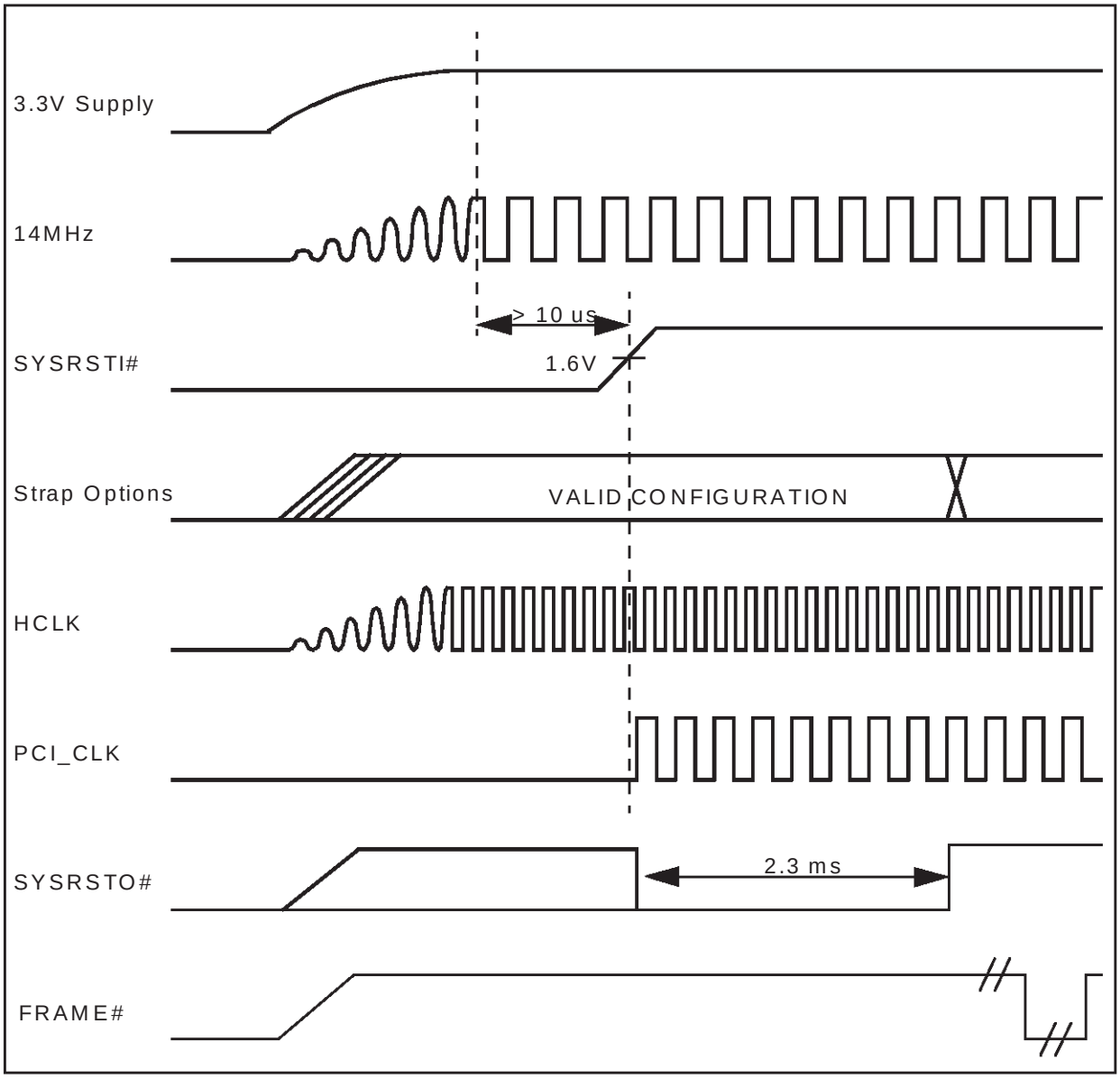


Table 4-5. SDRAM Bus AC Timing

Name	Parameter	Min	Max	Unit
t1	MCLKI to RAS#[1:0] Output Valid	-	6.2	ns
t2	MCLKI to CAS#[1:0] Output Valid	-	6.2	ns
t3	MCLKI to CS#[3:0] Output Valid	-	7.6	ns
t4	MCLKI to DQM#[7:0] Output Valid	-	8.1	ns
t5	MCLKI to MA[11:0] Output Valid	-	6.2	ns
t6	MCLKI to MWE# Output Valid	-	6.2	ns
t7	MCLKI to MD[63:0] Output Valid	-	8.2	ns
t8	MD[63:0] setup to MCKLI (no RDCLK)	8.2	-	ns
t9	MD[63:0] setup to MCKLI (RDCLK at min delay)	4.9	-	ns
t10	MD[63:0] setup to MCKLI (RDCLK at mid delay)	4.0	-	ns
t11	MD[63:0] setup to MCKLI (RDCLK at max delay)	3.0	-	ns
t12	MD[63:0] hold from MCKLI (no RDCLK)	3.1	-	ns
t13	MD[63:0] 0hold from MCKLI (RDCLK at min delay)	6.5	-	ns
t14	MD[63:0] hold from MCKLI (RDCLK at mid delay)	7.1	-	ns
t15	MD[63:0] hold from MCKLI (RDCLK at max delay)	8.5	-	ns
Note; The figures are extrapolated from silicon characterisation results and design timing analysis				

Table 4-6. PCI Bus AC Timing

Name	Parameter	Min	Max	Unit
t16	PCICLKI to any output	-	12.8	ns
t17	Setup to PCICKLI	7.0	-	ns
t18	Hold from PCICLKI	1.0	-	ns
t19	PCICLKI to PCIGNT# output valid	-	12.0	ns
t20	PCIREQ# setup to PCICLKI	12.0	-	ns
t21	PCIREQ# hold to PCICLKI	0.0	-	ns

Table 4-7. Graphics Adapter (VGA) AC Timing

Name	Parameter	Min	Max	Unit
t21	DCLK to VSYNC valid		27	ns
t22	DCLK to HSYNC valid		27	ns

Table 4-8. Video Input/TV Output AC Timing

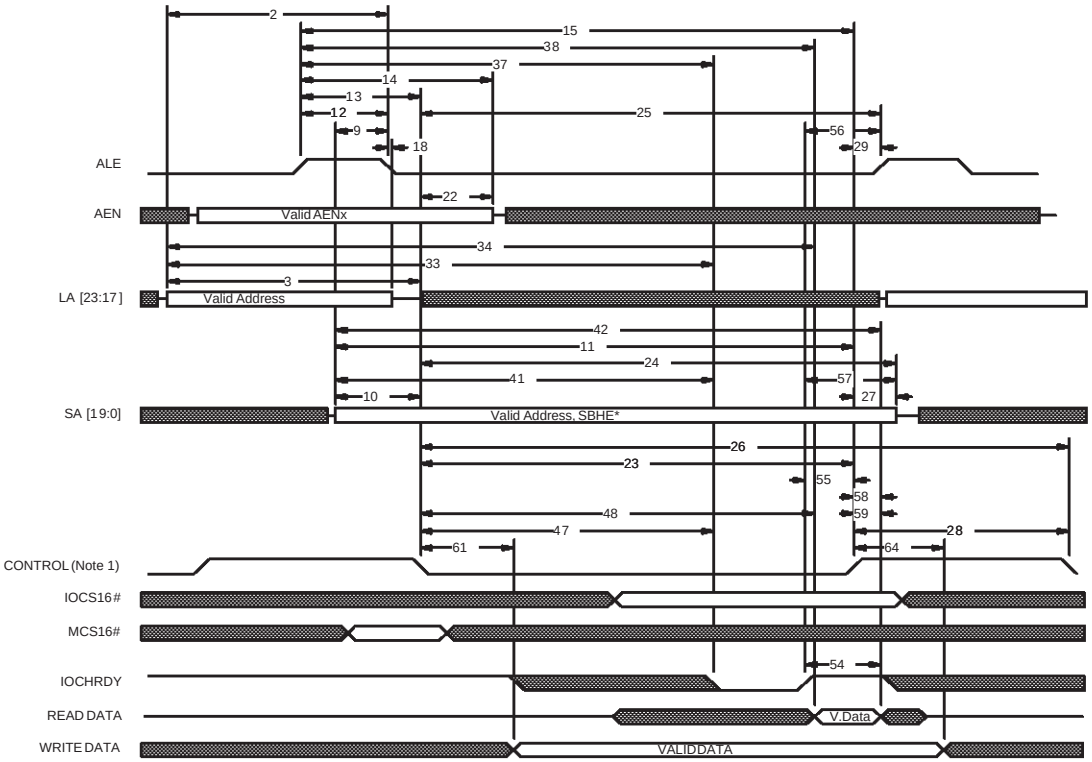
Name	Parameter	Min	Max	Unit
t56	VIN[7:0] setup to VCLK	5		ns
t57	VIN[7:0] hold from VCLK	4		ns
t58	VCLK to ODD_EVEN valid		15	ns
t59	VCLK to VCS valid		15	ns
t60	ODD_EVEN setup to VCLK	10		ns
t61	ODD_EVEN hold from VCLK	5		ns
t62	VCS setup to VCLK	10		ns
t63	VCS hold from VCLK	5		ns

Table 4-9. IPC Interface AC Timings

Name	Parameter	Min	Max	Unit
t23	XTALO to DACK_EN[2:0] valid		71	nS
t24	XTALO to TC valid		68	nS
t25	IRQ_MUX Input setup to ISACLK2X	0	-	nS
t26	DREQ_MUX[1:0] Input setup to ISACLK2X	0	-	nS

4.5.2 ISA INTERFACE AC TIMING CHARCTERISTICS

Figure 4-2 ISA Cycle (ref table Table 4-10**)**



Note 1; Stands for SMEMR#, SMEMW#, MEMR#, MEMW#, IOR# & IOW#.

Note; The clock has not been represented as it cannot be accuratly represented depending on the ISA Slave mode.

Table 4-10. ISA Bus AC Timing

Name	Parameter	Min	Max	Units
2	LA[23:17] valid before ALE# negated	5T		Cycles
3	**LA[23:17] valid before MEMR#, MEMW# asserted**			
3a	Memory access to 16 bit ISA Slave	5T		Cycles
3b	Memory access to 8 bit ISA Slave	5T		Cycles
9	SA[19:0] & SBHE valid before ALE# negated	1T		Cycles
10	**SA[19:0] & SBHE valid before MEMR#, MEMW# asserted**			
10a	Memory access to 16 bit ISA Slave	2T		Cycles
10b	Memory access to 8 bit ISA Slave	2T		Cycles
10	**SA[19:0] & SHBE valid before SMEMR#, SMEMW# asserted**			
10c	Memory access to 16 bit ISA Slave	2T		Cycle
10d	Memory access to 8 bit ISA Slave	2T		Cycle
10e	SA[19:0] & SBHE valid before IOR#, IOW# asserted	2T		Cycles
11	**XTALO to IOW# valid**			
Note; The signal numbering refers to Table 4-2				

Table 4-10. ISA Bus AC Timing

Name	Parameter		Min	Max	Units
	11a	Memory access to 16 bit ISA Slave - 2BCLK	2T		Cycles
	11b	Memory access to 16 bit ISA Slave - Standard 3BCLK	2T		Cycles
	11c	Memory access to 16 bit ISA Slave - 4BCLK	2T		Cycles
	11d	Memory access to 8 bit ISA Slave - 2BCLK	2T		Cycles
11e		Memory access to 8 bit ISA Slave - Standard 3BCLK	2T		Cycles
12	ALE# asserted before ALE# negated		1T		Cycles
13	**ALE# asserted before MEMR#, MEMW# asserted**				
	13a	Memory Access to 16 bit ISA Slave	2T		Cycles
	13b	Memory Access to 8 bit ISA Slave	2T		Cycles
13	**ALE# asserted before SMEMR#, SMEMW# asserted**				
	13c	Memory Access to 16 bit ISA Slave	2T		Cycles
	13d	Memory Access to 8 bit ISA Slave	2T		Cycles
13e	ALE# asserted before IOR#, IOW# asserted		2T		Cycles
14	**ALE# asserted before AL[23:17]**				
	14a	Non compressed	15T		Cycles
	14b	Compressed	15T		Cycles
15	**ALE# asserted before MEMR#, MEMW#, SMEMR#, SMEMW# negated**				
	15a	Memory Access to 16 bit ISA Slave- 4 BCLK	11T		Cycles
	15e	Memory Access to 8 bit ISA Slave- Standard Cycle	11T		Cycles
18a	ALE# negated before LA[23:17] invalid (non compressed)		14T		Cycles
18a	ALE# negated before LA[23:17] invalid (compressed)		14T		Cycles
22	**MEMR#, MEMW# asserted before LA[23:17]**				
	22a	Memory access to 16 bit ISA Slave.	13T		Cycles
	22b	Memory access to 8 bit ISA Slave.	13T		Cycles
23	**MEMR#, MEMW# asserted before MEMR#, MEMW# negated**				
	23b	Memory access to 16 bit ISA Slave Standard cycle	9T		Cycles
	23e	Memory access to 8 bit ISA Slave Standard cycle	9T		Cycles
23	**SMEMR#, SMEMW# asserted before SMEMR#, SMEMW# negated**				
	23h	Memory access to 16 bit ISA Slave Standard cycle	9T		Cycles
	23l	Memory access to 16 bit ISA Slave Standard cycle	9T		Cycles
23	**IOR#, IOW# asserted before IOR#, IOW# negated**				
	23o	Memory access to 16 bit ISA Slave Standard cycle	9T		Cycles
	23r	Memory access to 8 bit ISA Slave Standard cycle	9T		Cycles
24	**MEMR#, MEMW# asserted before SA[19:0]**				
	24b	Memory access to 16 bit ISA Slave Standard cycle	10T		Cycles
	24d	Memory access to 8 bit ISA Slave - 3BLCK	10T		Cycles
	24e	Memory access to 8 bit ISA Slave Standard cycle	10T		Cycles
	24f	Memory access to 8 bit ISA Slave - 7BCLK	10T		Cycles
24	**SMEMR#, SMEMW# asserted before SA[19:0]**				
	24h	Memory access to 16 bit ISA Slave Standard cycle	10T		Cycles
	24i	Memory access to 16 bit ISA Slave - 4BCLK	10T		Cycles
	24k	Memory access to 8 bit ISA Slave - 3BCLK	10T		Cycles
	24l	Memory access to 8 bit ISA Slave Standard cycle	10T		Cycles
24	**IOR#, IOW# asserted before SA[19:0]**				
	24o	I/O access to 16 bit ISA Slave Standard cycle	19T		Cycles
	24r	I/O access to 16 bit ISA Slave Standard cycle	19T		Cycles
Note; The signal numbering refers to Table 4-2					

Table 4-10. ISA Bus AC Timing

Name	Parameter		Min	Max	Units
25	**MEMR#, MEMW# asserted before next ALE# asserted**				
	25b	Memory access to 16 bit ISA Slave Standard cycle	10T		Cycles
	25d	Memory access to 8 bit ISA Slave Standard cycle	10T		Cycles
25	**SMEMR#, SMEMW# asserted before next ALE# aserted**				
	25e	Memory access to 16 bit ISA Slave - 2BCLK	10T		Cycles
	25f	Memory access to 16 bit ISA Slave Standard cycle	10T		Cycles
	25h	Memory access to 8 bit ISA Slave Standard cycle	10T		Cycles
25	**IOR#, IOW# asserted before next ALE# asserted**				
	25i	I/O access to 16 bit ISA Slave Standard cycle	10T		Cycles
	25k	I/O access to 16 bit ISA Slave Standard cycle	10T		Cycles
26	**MEMR#, MEMW# asserted before next MEMR#, MEMW# asserted**				
	26b	Memory access to 16 bit ISA Slave Standard cycle	12T		Cycles
	26d	Memory access to 8 bit ISA Slave Standard cycle	12T		Cycles
26	**SMEMR#, SMEMW# asserted before next SMEMR#, SMEMW# asserted**				
	26f	Memory access to 16 bit ISA Slave Standard cycle	12T		Cycles
	26h	Memory access to 8 bit ISA Slave Standard cycle	12T		Cycles
26	**IOR#, IOW# asserted before next IOR#, IOW# asserted**				
	26i	I/O access to 16 bit ISA Slave Standard cycle	12T		Cycles
	26k	I/O access to 8 bit ISA Slave Standard cycle	12T		Cycles
28	**Any command negated to MEMR#, SMEMR#, MEMR#, SMEMW# asserted**				
	28a	Memory access to 16 bit ISA Slave	3T		Cycles
	28b	Memory access to 8 bit ISA Slave	3T		Cycles
28	**Any command negated to IOR#, IOW# asserted**				
	28c	I/O access to ISA Slave	3T		Cycles
29a	MEMR#, MEMW# negated before next ALE# asserted		1T		Cycles
29b	SMEMR#, SMEMW# negated before next ALE# asserted		1T		Cycles
29c	IOR#, IOW# negated before next ALE# asserted		1T		Cycles
33	**LA[23:17] valid to IOCHRDY negated**				
	33a	Memory access to 16 bit ISA Slave - 4 BCLK	8T		Cycles
	33b	Memory access to 8 bit ISA Slave - 7 BCLK	14T		Cycles
34	**LA[23:17] valid to read data valid**				
	34b	Memory access to 16 bit ISA Slave Standard cycle	8T		Cycles
	34e	Memory access to 8 bit ISA Slave Standard cycle	14T		Cycles
37	**ALE# asserted to IOCHRDY# negated**				
	37a	Memory access to 16 bit ISA Slave - 4 BCLK	6T		Cycles
	37b	Memory access to 8 bit ISA Slave - 7 BCLK	12T		Cycles
	37c	I/O access to 16 bit ISA Slave - 4 BCLK	6T		Cycles
	37d	I/O access to 8 bit ISA Slave - 7 BCLK	12T		Cycles
38	**ALE# asserted to read data valid**				
	38b	Memory access to 16 bit ISA Slave Standard Cycle	4T		Cycles
	38e	Memory access to 8 bit ISA Slave Standard Cycle	10T		Cycles
	38h	I/O access to 16 bit ISA Slave Standard Cycle	4T		Cycles
	38l	I/O access to 8 bit ISA Slave Standard Cycle	10T		Cycles
41	**SA[19:0] SBHE valid to IOCHRDY negated**				
	41a	Memory access to 16 bit ISA Slave	6T		Cycles
	41b	Memory access to 8 bit ISA Slave	12T		Cycles
Note; The signal numbering refers to Table 4-2					

Table 4-10. ISA Bus AC Timing

Name	Parameter		Min	Max	Units
	41c	I/O access to 16 bit ISA Slave	6T		Cycles
	41d	I/O access to 8 bit ISA Slave	12T		Cycles
42	**SA[19:0] SBHE valid to read data valid**				
	42b	Memory access to 16 bit ISA Slave Standard cycle	4T		Cycles
	42e	Memory access to 8 bit ISA Slave Standard cycle	10T		Cycles
	42h	I/O access to 16 bit ISA Slave Standard cycle	4T		Cycles
	42l	I/O access to 8 bit ISA Slave Standard cycle	10T		Cycles
47	**MEMR#, MEMW#, SMEMR#, SMEMW#, IOR#, IOW# asserted to IOCHRDY negated**				
	47a	Memory access to 16 bit ISA Slave	2T		Cycles
	47b	Memory access to 8 bit ISA Slave	5T		Cycles
	47c	I/O access to 16 bit ISA Slave	2T		Cycles
	47d	I/O access to 8 bit ISA Slave	5T		Cycles
48	**MEMR#, SMEMR#, IOR# asserted to read data valid**				
	48b	Memory access to 16 bit ISA Slave Standard Cycle	2T		Cycles
	48e	Memory access to 8 bit ISA Slave Standard Cycle	5T		Cycles
	48h	I/O access to 16 bit ISA Slave Standard Cycle	2T		Cycles
	48l	I/O access to 8 bit ISA Slave Standard Cycle	5T		Cycles
54	**IOCHRDY asserted to read data valid**				
	54a	Memory access to 16 bit ISA Slave	1T(R)/2T(W)		Cycles
	54b	Memory access to 8 bit ISA Slave	1T(R)/2T(W)		Cycles
	54c	I/O access to 16 bit ISA Slave	1T(R)/2T(W)		Cycles
	54d	I/O access to 8 bit ISA Slave	1T(R)/2T(W)		Cycles
55a	IOCHRDY asserted to MEMR#, MEMW#, SMEMR#, SMEMW#, IOR#, IOW# negated		1T		Cycles
55b	IOCHRY asserted to MEMR#, SMEMR# negated (refresh)		1T		Cycles
56	IOCHRDY asserted to next ALE# asserted		2T		Cycles
57	IOCHRDY asserted to SA[19:0], SBHE invalid		2T		Cycles
58	MEMR#, IOR#, SMEMR# negated to read data invalid		0T		Cycles
59	MEMR#, IOR#, SMEMR# negated to daabus float		0T		Cycles
61	**Write data before MEMW# asserted**				
	61a	Memory access to 16 bit ISA Slave	2T		Cycles
	61b	Memory access to 8 bit ISA Slave (Byte copy at end of start)	2T		Cycles
61	**Write data before SMEMW# asserted**				
	61c	Memory access to 16 bit ISA Slave	2T		Cycles
	61d	Memory access to 8 bit ISA Slave	2T		Cycles
61	**Write Data valid before IOW# asserted**				
	61e	I/O access to 16 bit ISA Slave	2T		Cycles
	61f	I/O access to 8 bit ISA Slave	2T		Cycles
64a	MEMW# negated to write data invalid - 16 bit		1T		Cycles
64b	MEMW# negated to write data invalid - 8 bit		1T		Cycles
64c	SMEMW# negated to write data invalid - 16 bit		1T		Cycles
64d	SMEMW# negated to write data invalid - 8 bit		1T		Cycles
64e	IOW# negated to write data invalid		1T		Cycles
Note; The signal numbering refers to Table 4-2					

Table 4-10. ISA Bus AC Timing

Name	Parameter	Min	Max	Units
64f	MEMW# negated to copy data float, 8 bit ISA Slave, odd Byte by ISA Master	1T		Cycles
64g	IOW# negated to copy data float, 8 bit ISA Slave, odd Byte by ISA Master	1T		Cycles
Note; The signal numbering refers to Table 4-2				

Table 4-11. PCMCIA Interface AC Timing

Name	Parameters	Min	Max	Units
t27	Input setup to ISACLK2X	24		nS
t28	Input hold from ISACLK2X	5		nS
t29	ISACLK2X to IORD	-	55	nS
t30	ISACLK2X to IORW	-	55	nS
t31	ISACLK2X to AD[25:0]	-	25	nS
t32	ISACLK2X to OE#	2	55	nS
t33	ISACLK2X to WE#	2	55	nS
t34	ISACLK2X to DATA[15:0]	0	35	nS
t35	ISACLK2X to INPACK	2	55	nS
t36	ISACLK2X to CE1#	7	65	nS
t37	ISACLK2X to CE2#	7	65	nS
t38	ISACLK2X to RESET	2	55	nS

Table 4-12. IDE Interface Timing

Name	Parameters	Min	Max	Units

Table 4-13. Serial Port Interface AC Timing

Name	Parameters	Min	Max	Units
				nS nS nS

Table 4-14. Parallel Interface AC Timing

Name	Parameters	Min	Max	Units
t39	STROBE# to BUSY setup	0	-	nS
t40	PD bus to AUTPFD# hold	0	-	nS
t41	PB bus to BUSY setup	0	-	nS

Table 4-15. Keyboard Interface AC Timing

Name	Parameters	Min	Max	Units
t42	Input setup to KBCLK	5	-	nS
t43	Input hold to KBCLK	1	-	nS
t44	KBCLK to KBDATA	-	12	nS

Table 4-16. Mouse Interface AC Timing

Name	Parameters	Min	Max	Units
t45	Input setup to MCLK	5	-	nS
t46	Input hold to MCLK	1	-	nS
t47	MCLK to MDATA	-	12	nS

Table 4-17. Local Bus Interface AC Timing

Name	Parameters	Min	Max	Units
t48	PRDY# Input hold to HCLK	2		nS
t49	PD[15:0] Input hold to HCLK	2		nS
t50	PRDY# Input setup to HCLK	1	-	nS
t51	PD[15:0] Input setup to HCLK	2	4	nS
t52	HCLK to PA bus	-	15	nS
t53	HCLK to PD bus	-	15	nS
t54	HCLK to PWR0#	-	15	nS
t55	HCLK to PWR1#	-	15	nS
t56	HCLK to PRD0#	-	15	nS
t57	HCLK to PRD1#	-	15	nS
t58	HCLK to FCS0#	-	15	nS
t59	HCLK to FCS1#	-	15	nS
t60	HCLK to IOCS#[3:0]	-	15	nS

Table 4-18. TFT Interface Timing

Name	Parameters	Min	Max	Units
t61	DCLK to FPLINE		15	nS
t62	DCLK to R[2]		15	nS
t63	DCLK to R[3]		15	nS
t64	DCLK to R[4]		15	nS
t65	DCLK to R[5]		15	nS
t66	DCLK to G[2]		15	nS
t67	DCLK to G[3]		15	nS
t68	DCLK to G[4]		15	nS
t69	DCLK to G[5]		15	nS
t70	DCLK to B[2]		15	nS
t71	DCLK to B[3]		15	nS
t72	DCLK to B[4]		15	nS
t73	DCLK to B[5]		15	nS
t74	DCLK to FPFRAME		15	nS

Table 4-19. USB Interface Timing

Name	Parameters	Min	Max	Units

5. BOARD LAYOUT

5.1 Thermal dissipation

Thermal dissipation of the STPC depends mainly on supply voltage. As a result, when the system does not need to work at 3.45V, it is interesting to reduce the voltage to 3.15V, for example, if it is possible. This may save few 100's of mW.

The second area to look at is unused interfaces and functions. Depending on the application, some input signals can be grounded, and some blocks not powered or shutdown. Clock speed dynamic adjustment is also a solution that can be used along with the integrated power management unit.

The standard way to route thermal balls to internal ground layer implements only one via pad for each ball pad, connected using a 8-mil wire.

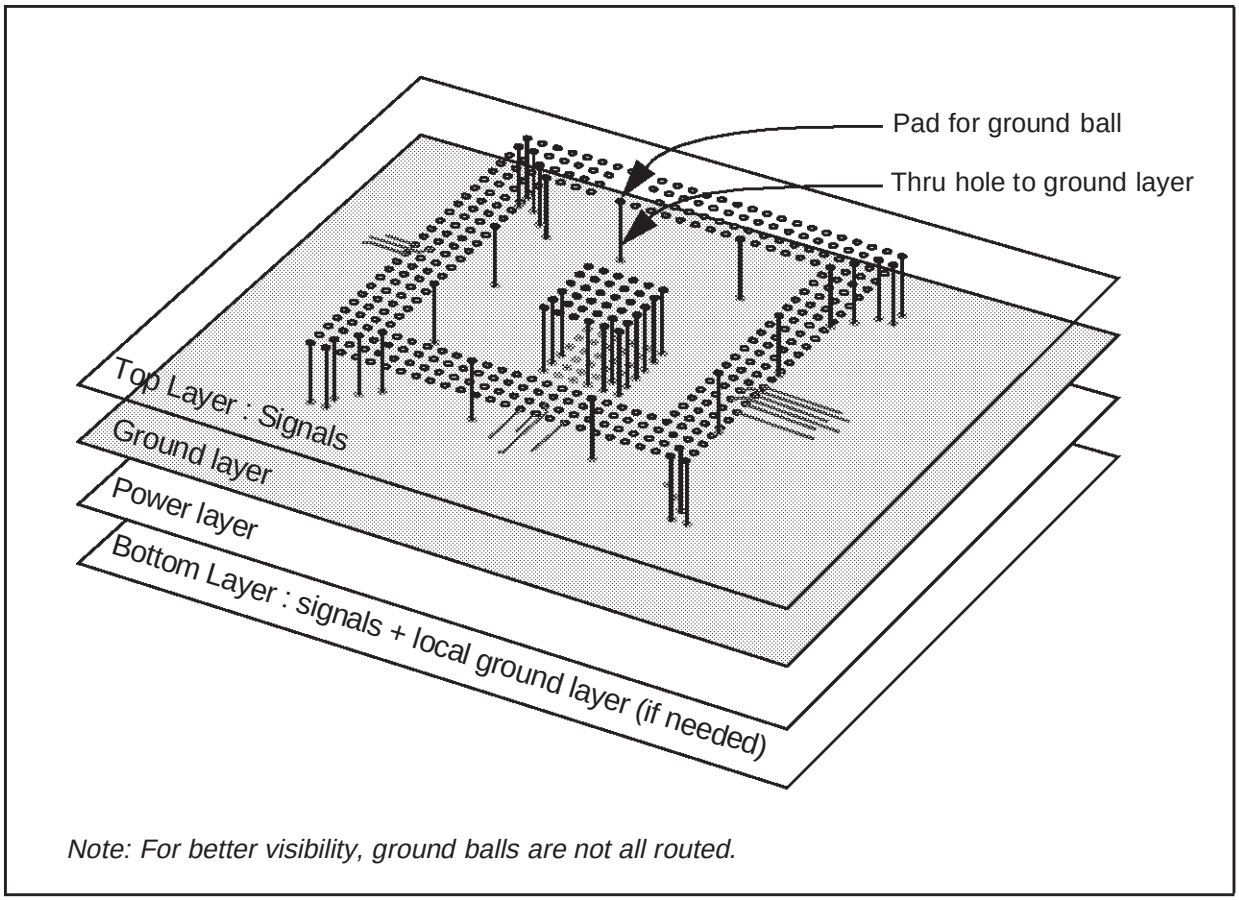
With such configuration the Plastic BGA 388 package does 90% of the thermal dissipation through the ground balls, and especially the central thermal balls which are directly connected to the die, the remaining 10% is dissipated through the case. Adding a heat sink reduces this value to 85%.

As a result, some basic rules has to be applied when routing the STPC in order to avoid thermal problems.

First of all, the whole ground layer acts as a heat sink and ground balls must be directly connected to it as illustrated in Figure 5-1.

If one ground layer is not enough, a second ground plane may be added on solder side.

Figure 5-1. Ground routing



Note: For better visibility, ground balls are not all routed.

BOARD LAYOUT

When considering thermal dissipation, the most important - and not the more obvious - part of the layout is the connection between the ground balls and the ground layer.

A 1-wire connection is shown in Figure 5-2. The use of a 8-mil wire results in a thermal resistance of 105°C/W assuming copper is used (418 W/ m.°K). This high value is due to the thickness (34 µm) of the copper on the external side of the PCB.

Considering only the central matrix of 36 thermal balls and one via for each ball, the global thermal resistance is 2.9°C/W. This can be easily improved using four 10 mil wires to connect to the four vias around the ground pad link as inFigure 5-3. This gives a total of 49 vias and a global resistance for the 36 thermal balls of 0.6°C/W.

The use of a ground plane like in Figure 5-4 is even better.

To avoid solder wicking over to the via pads during soldering, it is important to have a solder mask of 4 mil around the pad (NSMD pad), this gives a diameter of 33 mil for a 25 mil ground pad.

To obtain the optimum ground layout, place the vias directly under the ball pads. In this case no local boar d distortion is tolerated.

The thickness of the copper on PCB layers is typically 34 µm for external layers and 17 µm for internal layers. That means thermal dissipation is not good and temperature of the board is concentrated around the devices and falls quickly with increased distance.

When it is possible to place a metal layer inside the PCB, this improves dramatically the heat spreading and hence thermal dissipation of the board.

Figure 5-2. Recommended 1-wire ground pad layout

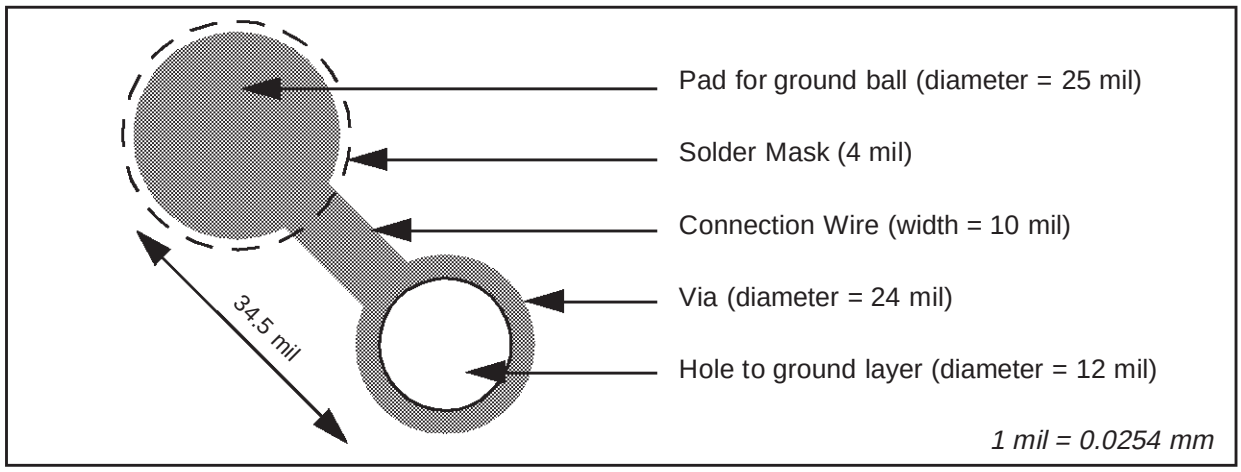


Figure 5-3. Recommended 4-wire ground pad layout

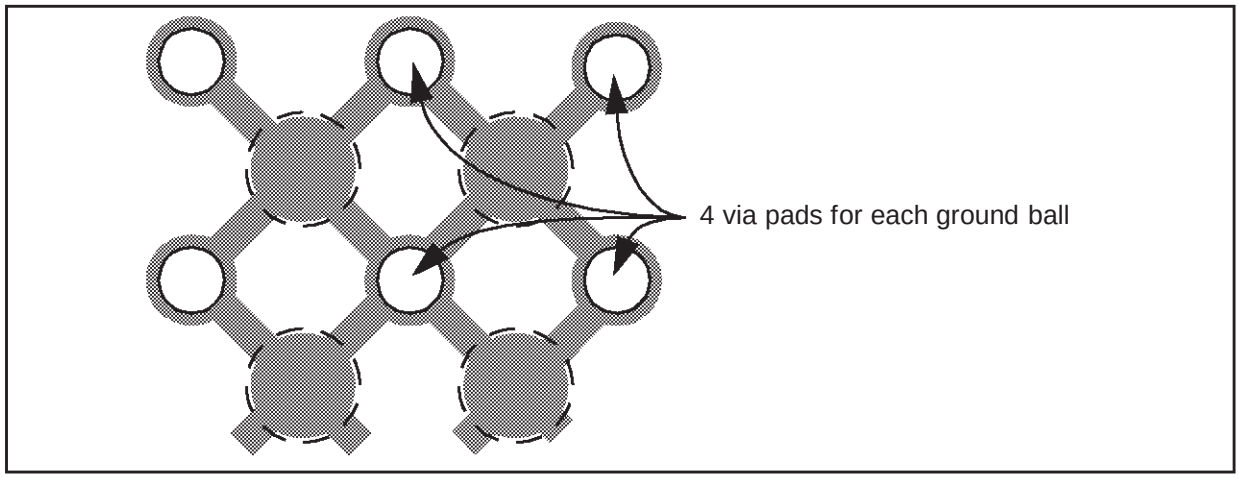
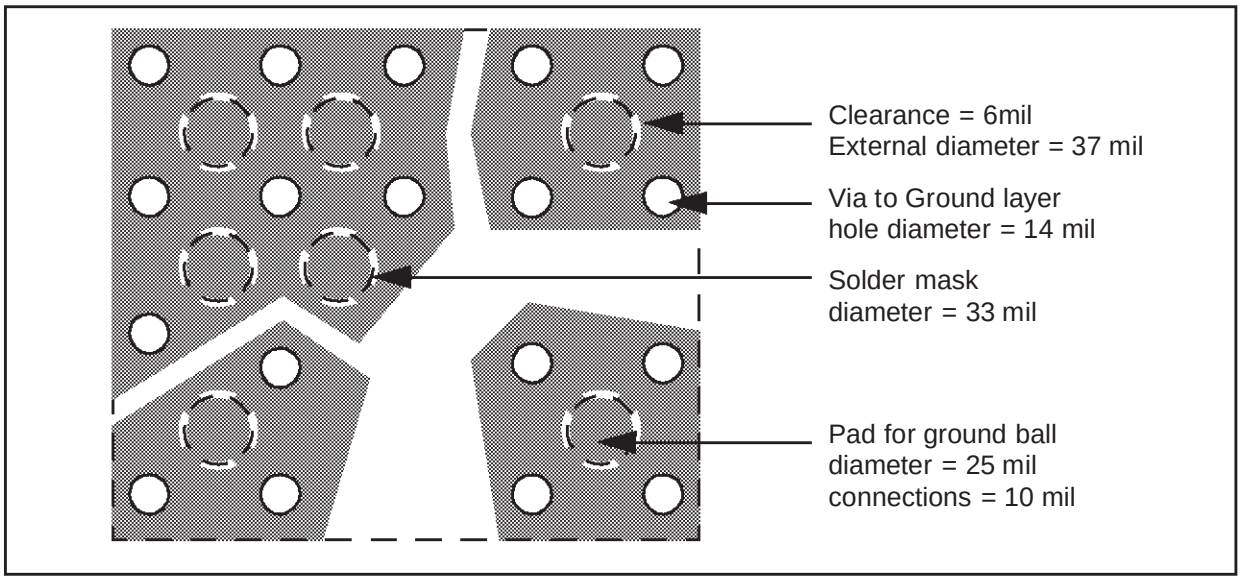


Figure 5-4. Optimum layout for central ground ball



The PBGA Package dissipates also through peripheral ground balls. When a heat sink is placed on the device, heat is more uniformely spread throughout the moulding increasing heat dissipation through the peripheral ground balls.

The more via pads are connected to each ground ball, the more heat is dissipated . The only limitation is the risk of lossing routing channels.

Figure 5-5 shows a routing with a good trade off between thermal dissipation and number of routing channels.

A local ground plane on opposite side of the board as shown in Figure 5-6 improves thermal dissipation. It is used to connect decoupling capacitances but can also be used for connection to a heat sink or to the system's metal box for better dissipation.

This possibility of using the whole system's box for thermal dissipation is very usefull in case of high temperature inside the system and low temperature outside. In that case, both sides of the PBGA should be thermally connected to the metal chassis in order to propagate the heat flow through the metal. Figure 5-7 illustrates such implementation.

5.2 High speed signals

Some Interfaces of the STPC run at high speed and have to be carefully routed or even shielded.

Here is the list of these interfaces, in decreasing speed order:

1) Memory Interface.

2) Graphics and video interfaces

3) PCI bus

4) 14MHz oscillator stage

All the clocks haves to be routed first and shielded for speeds of 27MHz or more. The high speed signals follow the same contrainsts, like the memory control signals and the PCI control signals.

The next interfaces to be routed are Memory, Video/graphics, and PCI.

All the analog noise sensitive signals have to be routed in a separate area and hence can be routed indepedently.

Figure 5-5. Global ground layout for good thermal dissipation

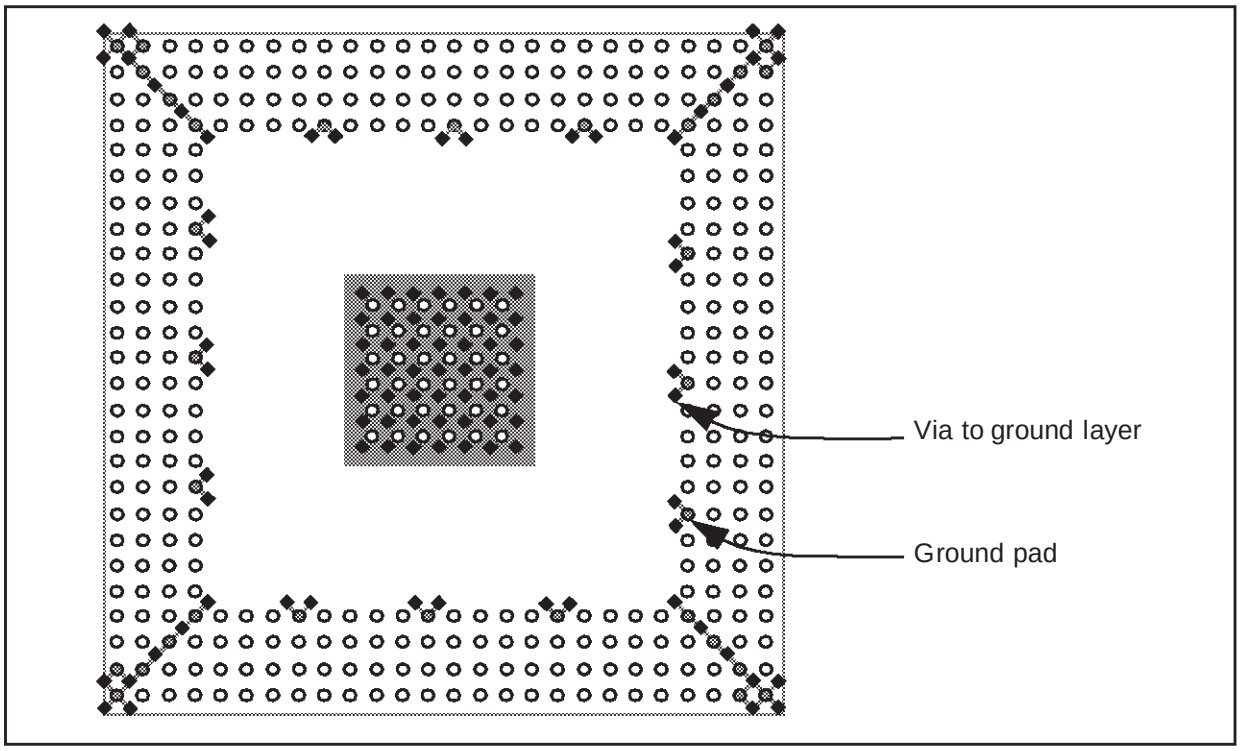


Figure 5-6. Bottom side layout and decoupling

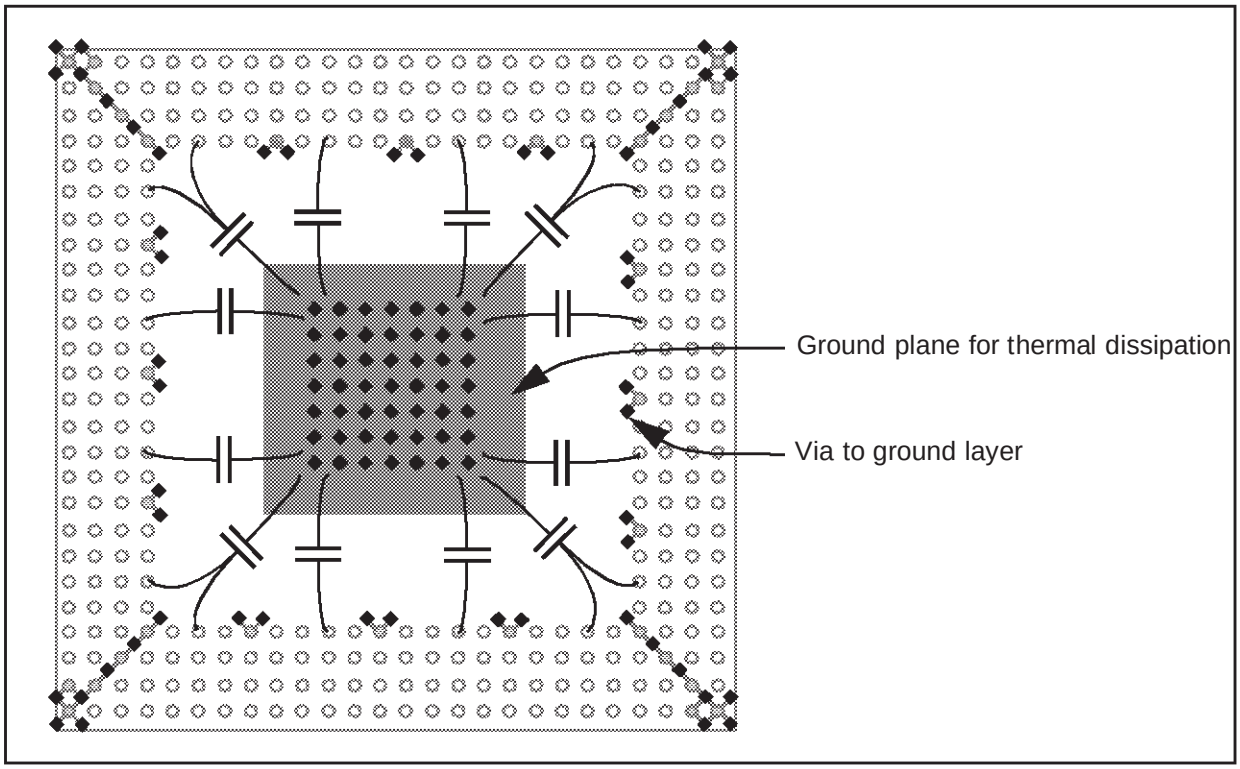


Figure 5-7. Use of metal plate for thermal dissipation

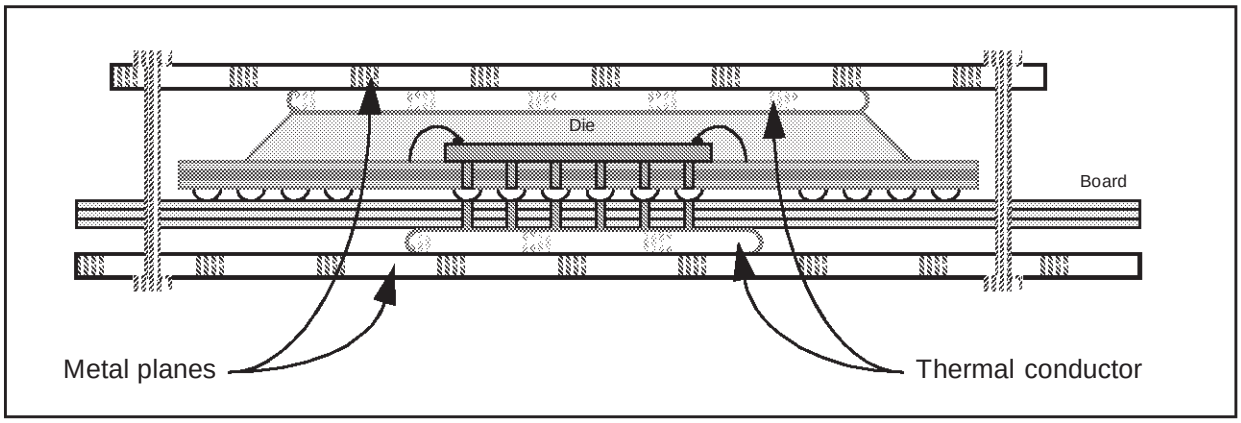
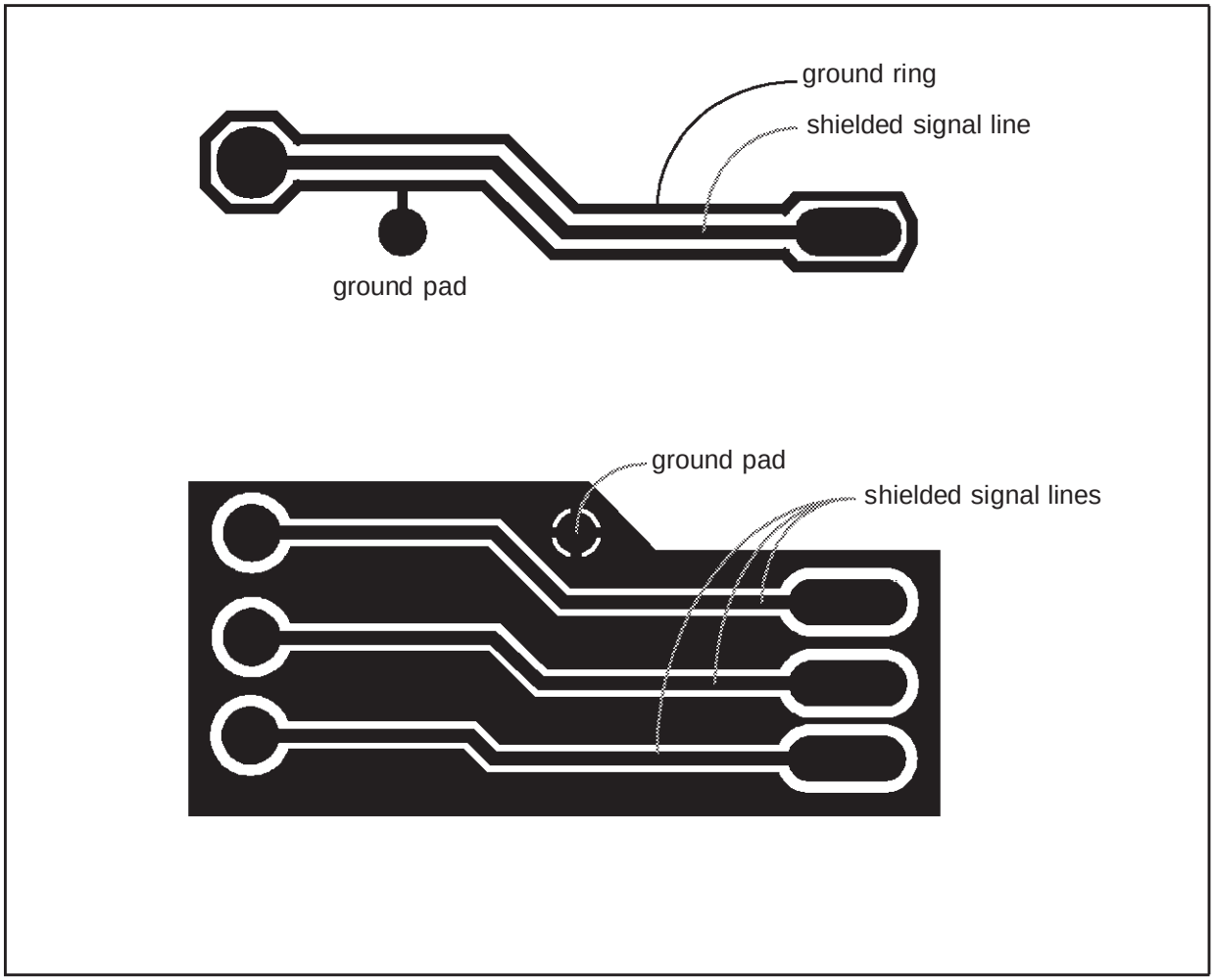


Figure 5-8. Shielding signals



5.3 Memory interface

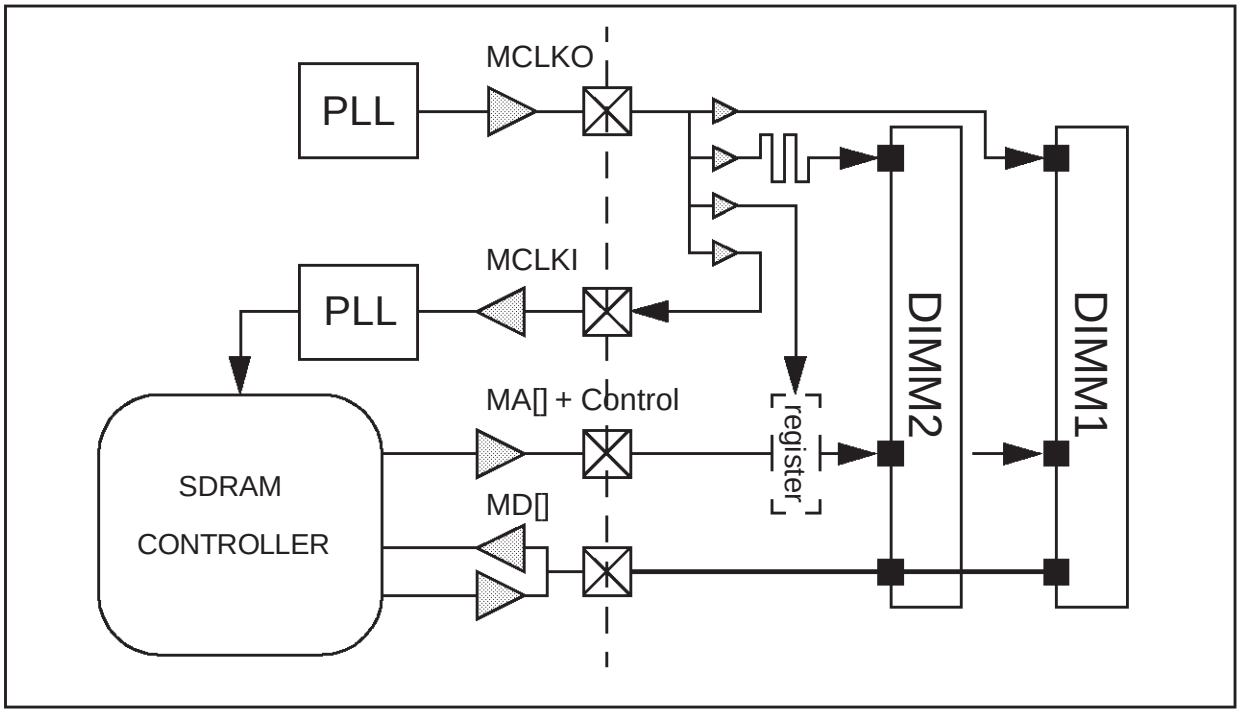
5.3.1 Introduction

In order to achieve SDRAM memory interfaces which work at clock frequencies of 100MHz and above, careful consideration has to be given to the timing of the interface with all the various electrical and physical constraints taken into consideration. The guidelines described below are related to SDRAM components on DIMM modules. For applications where the memories are directly soldered to the motherboard, the PCB should be laid out such that the trace lengths fit within the constraints shown here. The traces could be slightly longer since the extra routing on the DIMM PCB is no longer present but it is then up to the user to verify the timings.

5.3.2 SDRAM Clocking Scheme

The SDRAM Clocking Scheme deserves a special mention here. Basically the memory clock is generated on-chip through a PLL and goes directly to the MCLKO output pin of the STPC. The nominal frequency is 100MHz. Because of the high load presented to the MCLK on the board by the DIMMs it is recommeded to rebuffer the MCLKO signal on the board and balance the skew to the clock ports of the different DIMMs and the MCLKI input pin of STPC.

Figure 5-9. Clock scheme



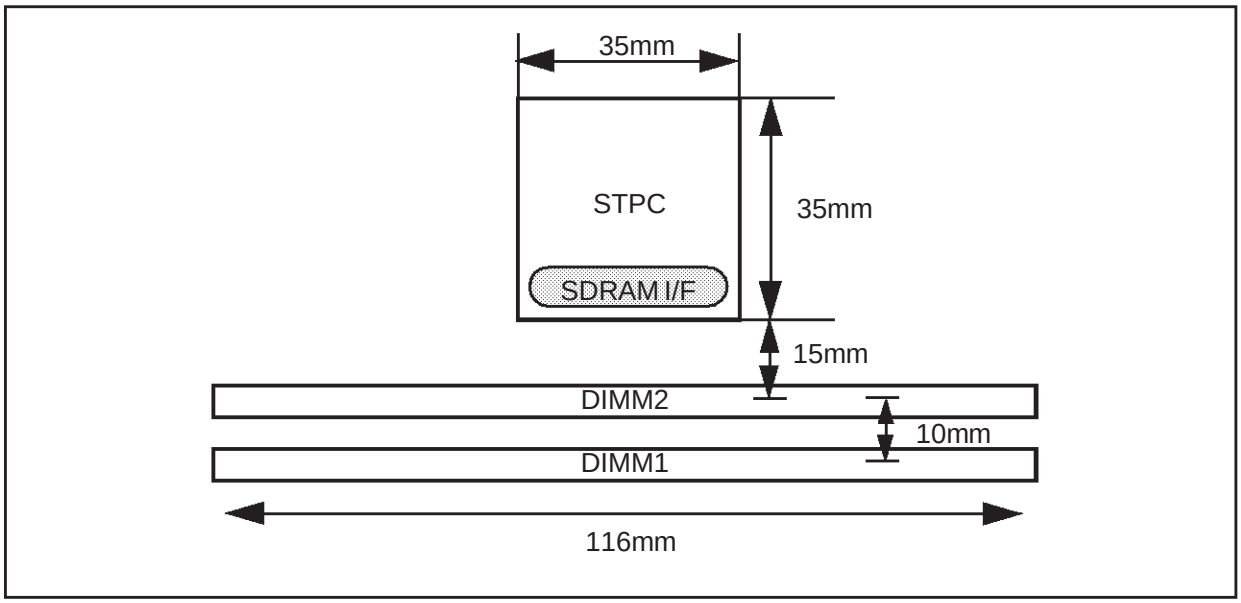
5.3.3 Board Layout Issues

The physical layout of the motherboard PCB assumed in this presentation is as shown inFigure 5-10. Because all the memory interface signal balls are located in the same region of the STPC device it is possible to orientate the device to reduce the trace lengths. The worst case routing length to the DIMM1 is estimated to be 100mm.

Solid power and ground planes are a must in order to provide good return paths for the signals and to reduce EMI and noise. Also there should be ample high frequency decoupling between the power and ground planes to provide a low impedance path between the planes for the return paths for signal routings which change layers. If possible the traces should be routed adjacent to the same power or ground plane for the length of the trace.

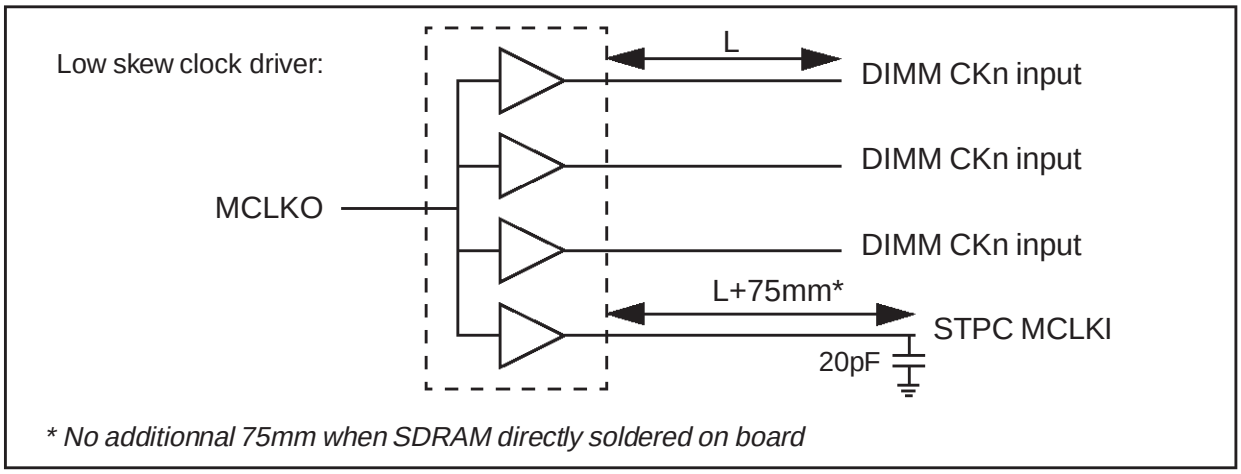
For the SDRAM interface the most critical signal is the clock. Any skew between the clocks at the SDRAM components and the memory controller will impact the timing budget. In order to get well matched clocks at all the components it is recommended that all the DIMM clock pins, STPC memory clock input (MCLKI) and any other component using the memory clock are individually driven

Figure 5-10. DIMM placement



from a low skew clock driver with matched routing lengths. This is shown in Figure 5-11.

Figure 5-11. Clock routing



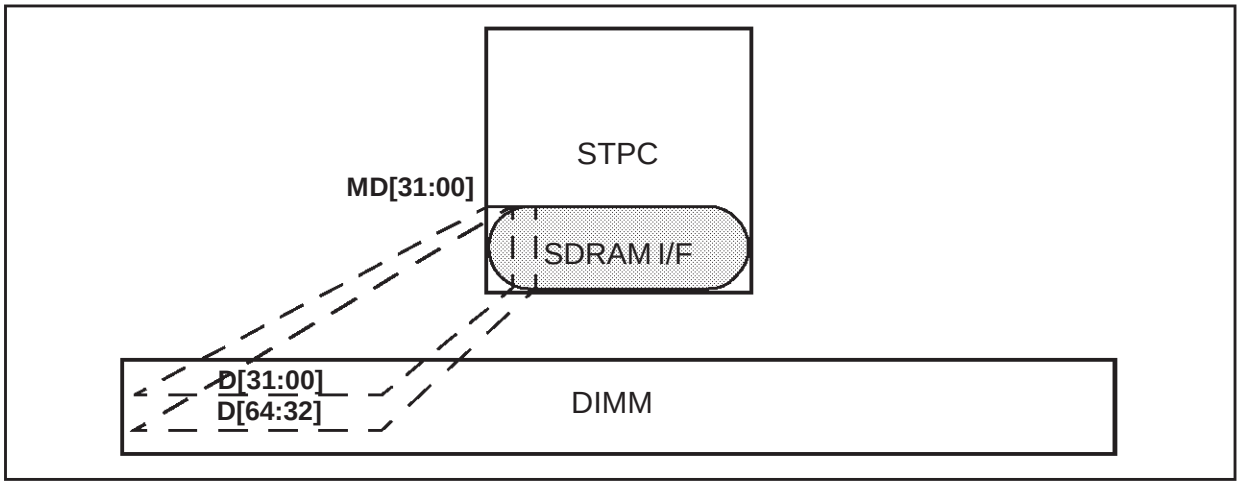
The maximum skew between pins for this part is 250ps. The important factors for the clock buffer are a consistent drive strength and low skew between the outputs. The delay through the buffer is not important so it does not have to be a zero delay PLL type buffer. The trace lengths from the clock driver to the DIMM CKn pins should be matched exactly. Since the propagation speed can vary between PCB layers the clocks should be routed in a consistent way. The routing to the STPC memory input should be longer by 75mm to compensate for the extra clock routing on the DIMM. Also a 20pF capacitor should be placed as near as possible to the clock input of the STPC to compensate for the DIMM's higher clock load. The impedance of the trace used for the clock routing should be matched to the DIMM clock trace impedance (60-75 ohms). To minimise crosstalk the clocks should be routed with spacing to adjacent tracks of at least twice the clock trace width. For designs which use SDRAMs directly mounted on the motherboard PCB all the clock trace lengths should be matched exactly.

The DIMM sockets should be populated starting with the furthest DIMM from the STPC device first

(DIMM1). There are 2 types of DIMM devices; single row and dual row. The dual row devices require 2 chip select signals to select between the two rows. A STPC device with 4 chip select control lines could control either 4 single row DIMMs or 2 dual row DIMMs.

When using DIMM modules, schematics have to be done carefully in order to avoid data busses completely crossed on the board. This has to be checked at the library level. The DQM signals must be exchanged using the same order.

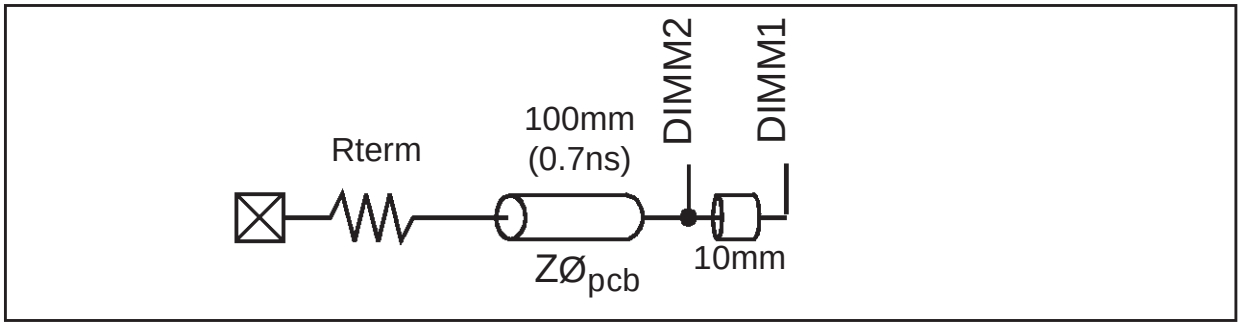
Figure 5-12. Optimum data bus layout for DIMM



5.3.4 Address & Control Signals

This group encompasses the memory address MA[10:0], bank address BA[0], RAS, CAS and write enable WE signals. The load of the DIMM module on these signals is the most important one and depends upon the type of SDRAM components used (x4, x8 or x16) and whether the DIMM module is single or dual row. The capacitive loading of the SDRAM inputs alone for an x8 single row DIMM will be about 30-40pF. An equivalent circuit for the timing simulation is shown inFigure 5-13 Most of the delays are due to the PCB traces and loading rather than the pad itself.

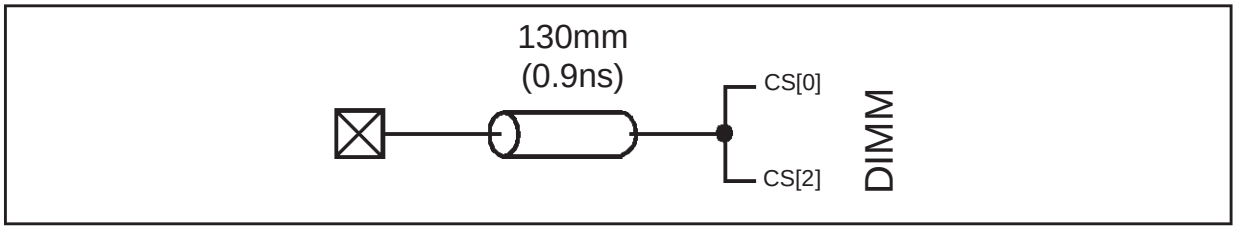
Figure 5-13. Address/control equivalent circuit



5.3.5 Chip Select Signals (CS#[3:0])

There are 4 chip select pins per DIMM. Chip selects 0 and 2 are always used to select the first row of SDRAMs and chip selects 1 and 3 select the second row on dual bank SDRAMs. The chip select outputs only have to drive one DIMM each

Figure 5-14. CS# equivalent circuit



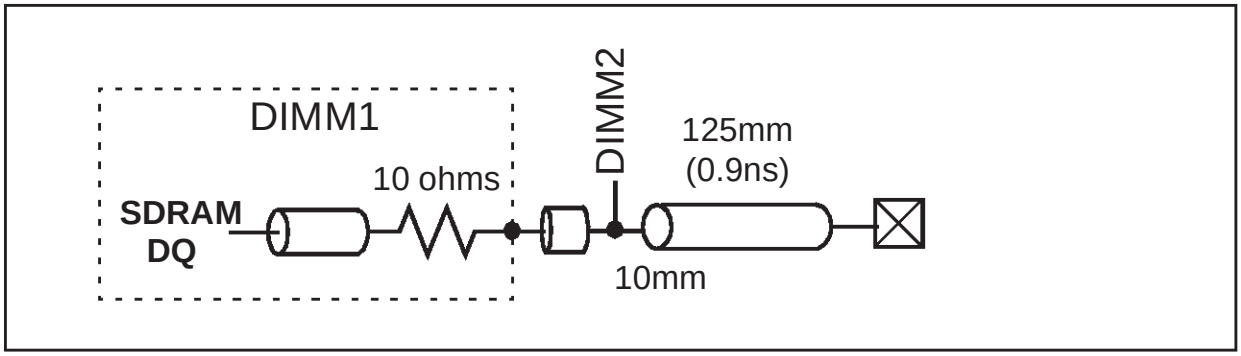
5.3.6 Data Write (MD[63:0])

The load on the data signals is much lower than the address/control signals for an unbuffered DIMM. For a registered DIMM the data signals are the only memory pins of the DIMM which are not registered. For the design to get maximum benefit from using registered DIMMs the timings should be compared to the timings for registered DIMMs for the other pins.

5.3.7 Data Read (MD[63:0])

The data read simulation circuit is shown below..

Figure 5-15. Data read equivalent circuit



5.3.8 Data Mask (DQM[7:0])

The data mask load is quite similar to that of the data signals.

5.3.9 Summary

For unbuffered DIMMs the address/control signals will be the most critical for timing. The simulations show that for these signals the best way to drive them is to use a parallel termination. For applications where speed is not so critical series termination can be used as this will save power. Using a low impedance such as 50Ω for these critical traces is recommended as it both reduces the delay and the overshoot.

The other memory interface signals will typically be not as critical as the address/control signals for unbuffered DIMMs. When using registered DIMMs the other signals will probably be just as critical as the address/control signals so to gain maximum benefit from using registered DIMMs the timings should also be considered in that situation. Using lower impedance traces is also beneficial for the other signals but if their timing is not as critical as the address/control signals they could use the default value. Using a lower impedance implies using wider traces which may have an impact on the routing of the board.

5.4 SDRAM LAYOUT EXAMPLES

The STPC provides MA, RAS#, CAS#, WE#, CS#, DQM#, BA0 (MA[11])and MD for SDRAM control. From 2 to 128 MBytes of main memory are supported in 1 to 4 banks. All Banks must be 64 bits wide.

The following memory devices are supported:

4Mbit x 4, 8Mbit x 2 & 16Mbit x 1 or if in the case of two internal bank chips, 2Mbit x 4 x 2, 4Mbit x 2 x 2 & 8Mbit x 1 x 2 .

The following Figure 5-16 and Figure 5-17, shows two possible SDRAM organizations based on one or two bank configurations.

Notes for Figure 5-16 and Figure 5-17;

All buffers must be low skew clock buffers

One clock driver can operate upto four memory chips.

All the clock lines must follow the rules below;

MCLKI = MCLK0 + MCLK0A

= .....

= MCLK0 + MCLK0D

= MCLK1 + MCLK1A

= .....

= MCLK1 + MCLK1D

This means that all line lengths must go from the buffer to the memory chips (MCLK1 or MCLK0 or ...) and from the buffer to the STPC (MCLKI) must be identical.

5.4.1 Host Address to MA bus Mapping

Graphics memory resides at the beginning of Bank 0. Host memory begins at the top of graphics memory and extends to the top of populated SDRAM.

The bank attributes can be retrieved from a lookup table to select the final SDRAM row and column address mappings. (Table 5-2). Also Table 5-1 shows the Standard DIMM Pinout for the users that wish to design with DIMMs.

.

Figure 5-16. One memory Bank with eight chips (8-Bit)

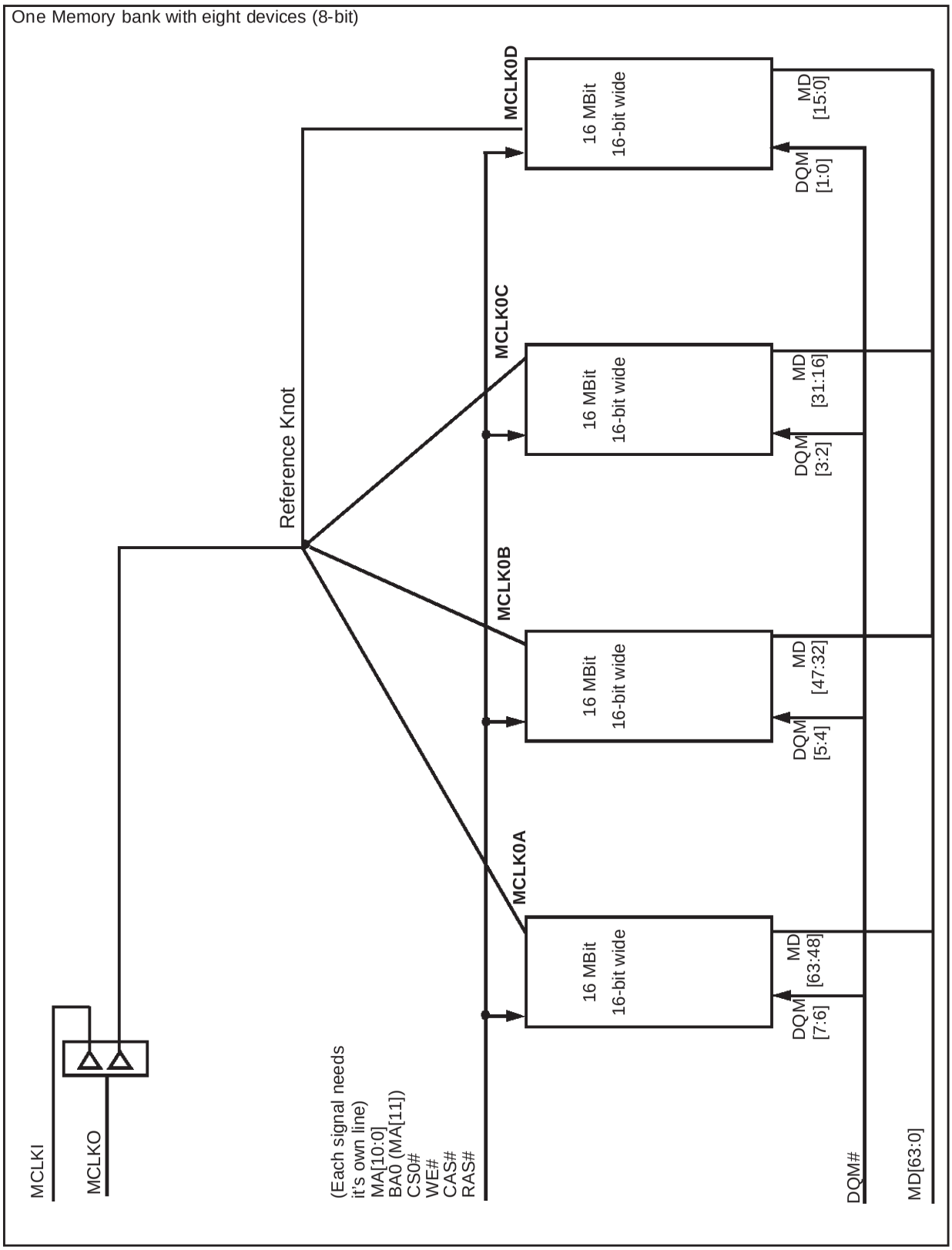


Figure 5-17. Two memory banks with eight chips on each (8-Bit)

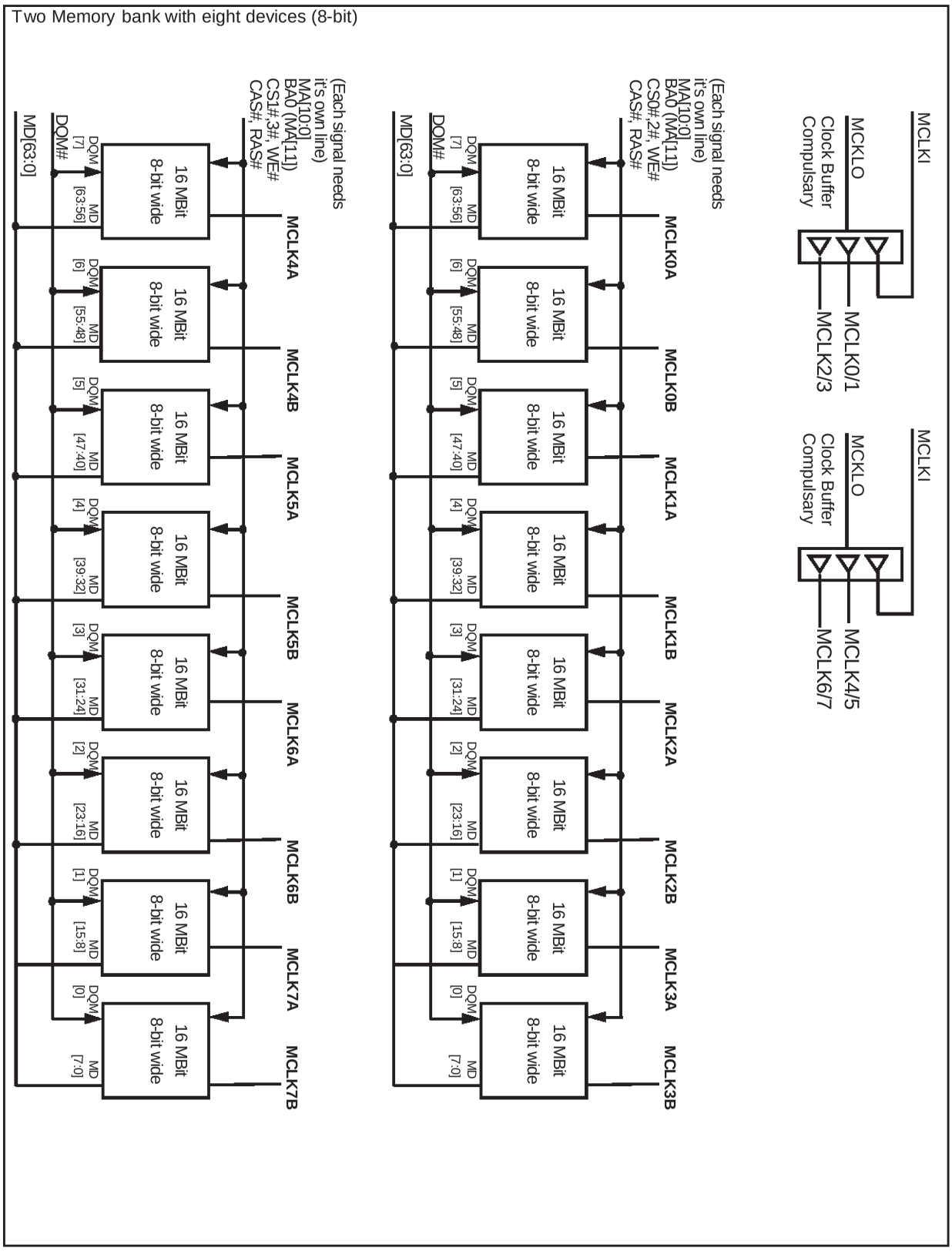


Table 5-1. Standard Memory DIMM Pinout

Memory Banks pin number	16Mbit(2 banks)
...	MA[10:0]
123	-
126	-
39	-
122	BA0(MA11)

Table 5-2. Address Mapping

Address Mapping: 16 Mbit - 2 banks												
STPC I/F	BA0(MA11)	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
RAS ADDRESS	A11	A22	A21	A2	A19	A18	A17	A16	A15	A14	A13	A12
CAS ADDRESS	A11	0	A24	A23	A10	A9	A8	A7	A6	A5	A4	A3

6. MECHANICAL DATA

6.1 516-Pin Package Dimension

The pin numbering for the STPC 516-pin Plastic BGA package is shown in Figure 6-1.

Dimensions are shown in Figure 6-2, Table 6-1 and Figure 6-3, Table 6-2.

Figure 6-1. 516-Pin PBGA Package - Top View

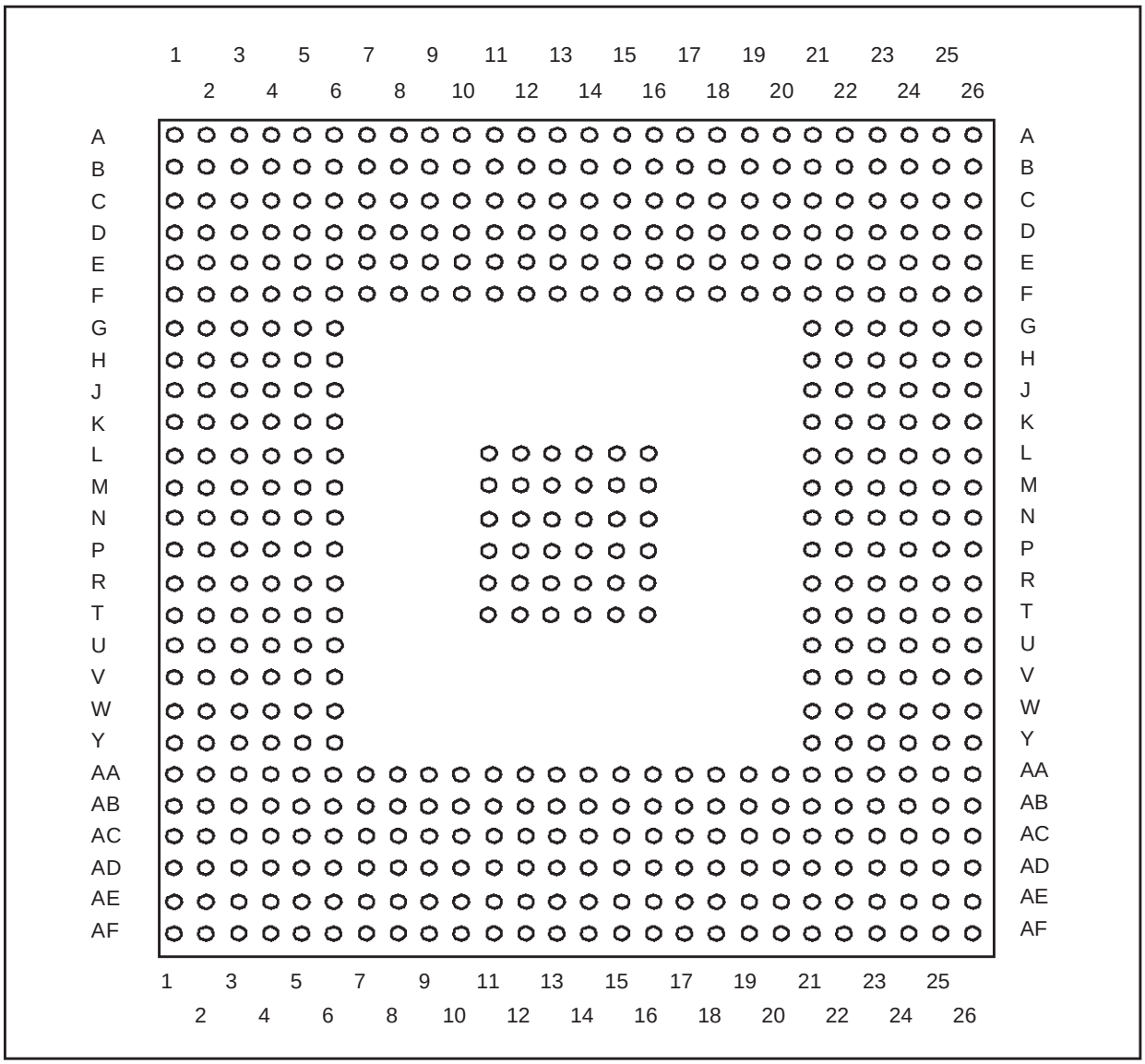


Figure 6-2. 516-pin PBGA Package - PCB Dimensions

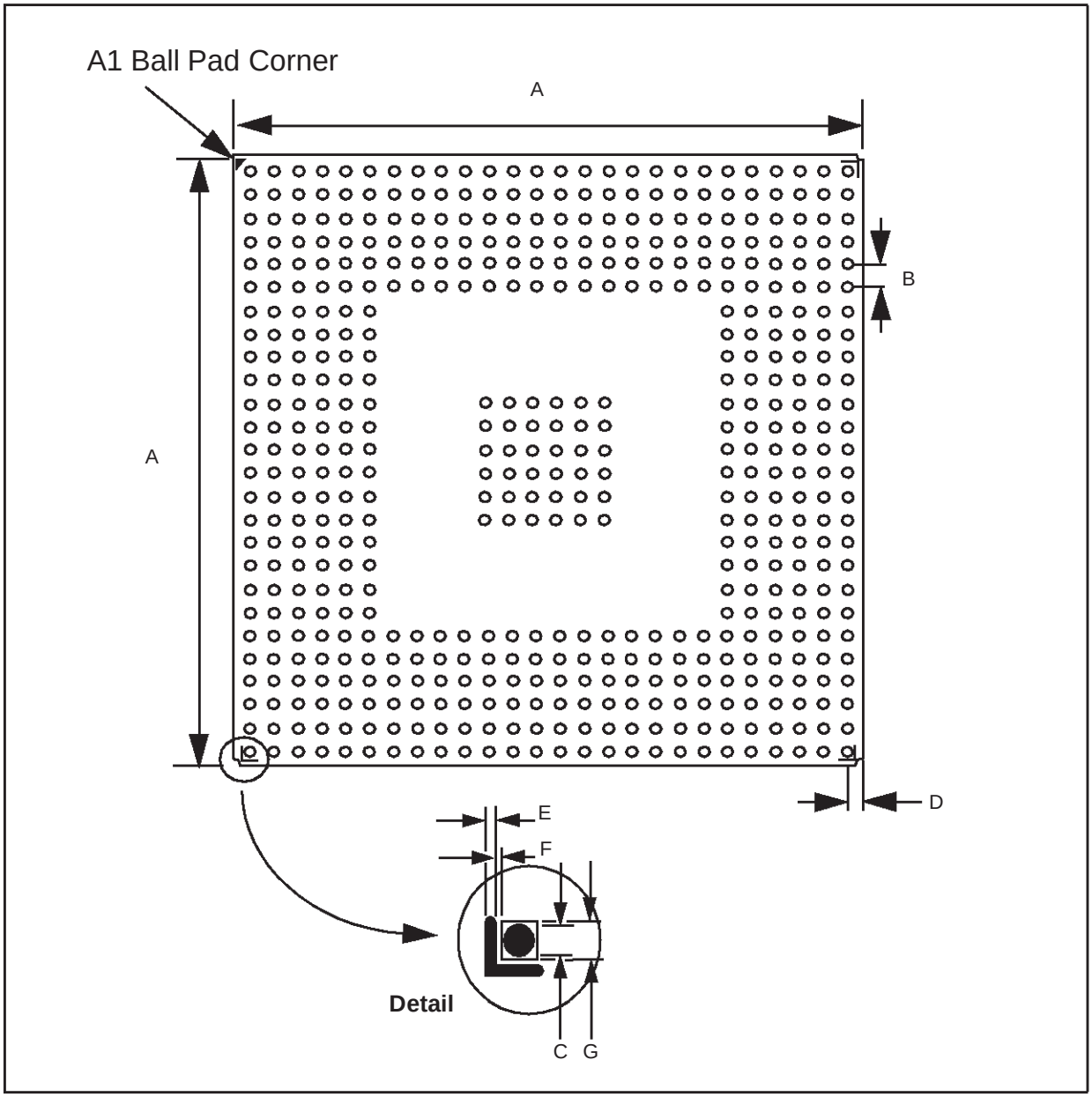


Table 6-1. 516-pin PBGA Package - PCB Dimensions

Symbols	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	34.80	35.00	35.20	1.370	1.378	1.386
B	1.22	1.27	1.32	0.048	0.050	0.052
C	0.60	0.76	0.90	0.024	0.030	0.035
D	1.57	1.62	1.67	0.062	0.064	0.066
E	0.15	0.20	0.25	0.006	0.008	0.001
F	0.05	0.10	0.15	0.002	0.004	0.006
G	0.75	0.80	0.85	0.030	0.032	0.034

Figure 6-3. 516-pin PBGA Package - Dimensions

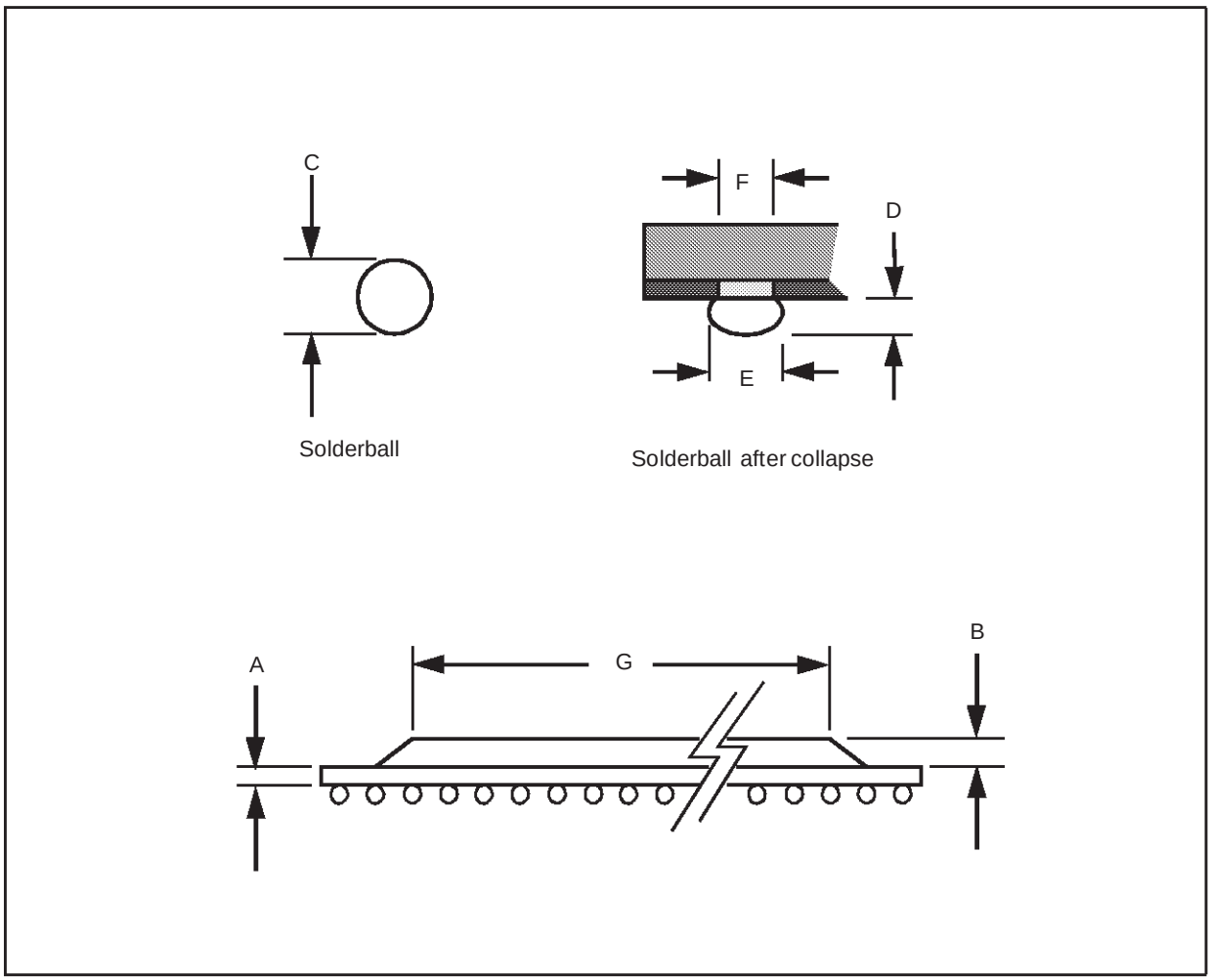


Table 6-2. 516-pin PBGA Package - Dimensions

Symbols	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	0.50	0.56	0.62	0.020	0.022	0.024
B	1.12	1.17	1.22	0.044	0.046	0.048
C	0.60	0.76	0.92	0.024	0.030	0.036
D	0.52	0.53	0.54	0.020	0.021	0.022
E	0.63	0.78	0.93	0.025	0.031	0.037
F	0.60	0.63	0.66	0.024	0.025	0.026
G		30.0			11.8	

6.2 516-Pin Package thermal data

516-pin PBGA package has a Power Dissipation Capability of 4.5W which increases to 6W when used with a Heatsink.

Structure in shown in Figure 6-4.

Thermal dissipation options are illustrated in Figure 6-5 and Figure 6-6.

Figure 6-4. 516-Pin PBGA structure

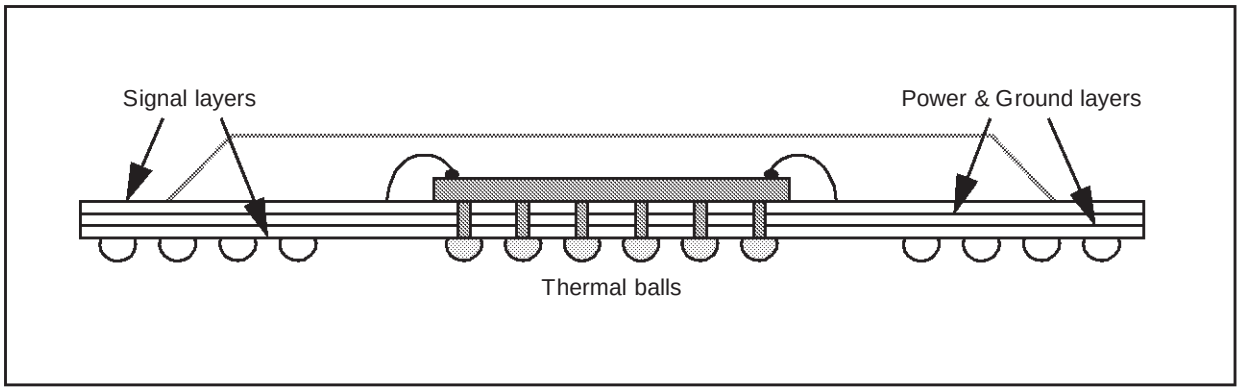


Figure 6-5. Thermal dissipation without heatsink

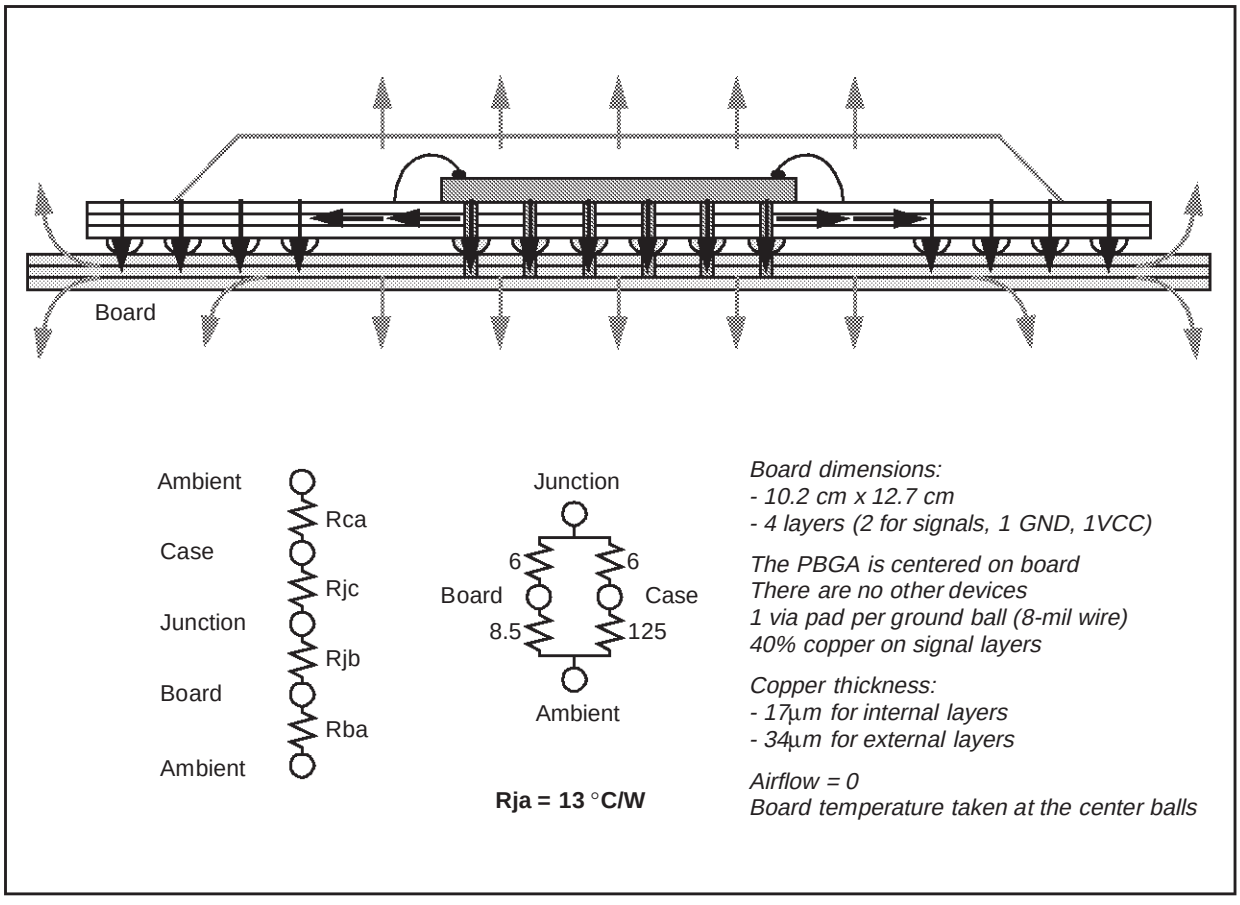
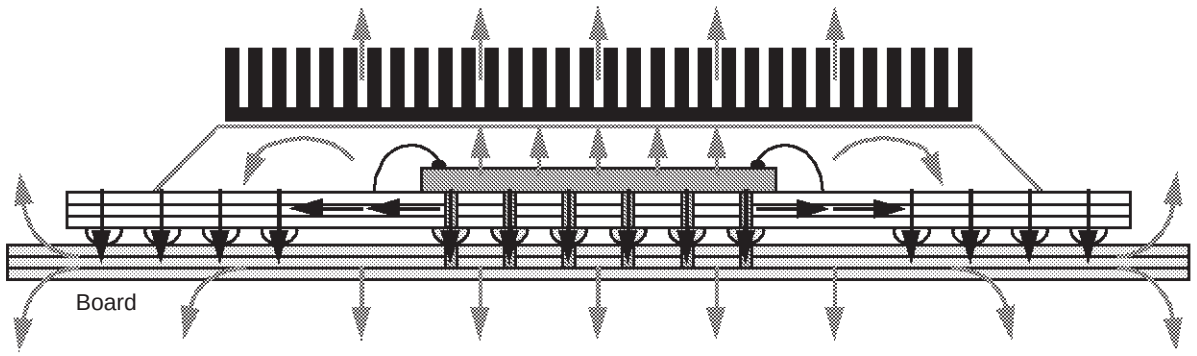
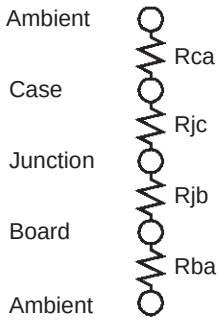
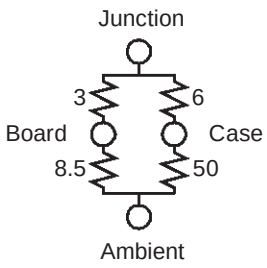


Figure 6-6. Thermal dissipation with heatsink







Rja = 9.5 °C/W

Board dimensions:
- 10.2 cm x 12.7 cm
- 4 layers (2 for signals, 1 GND, 1VCC)

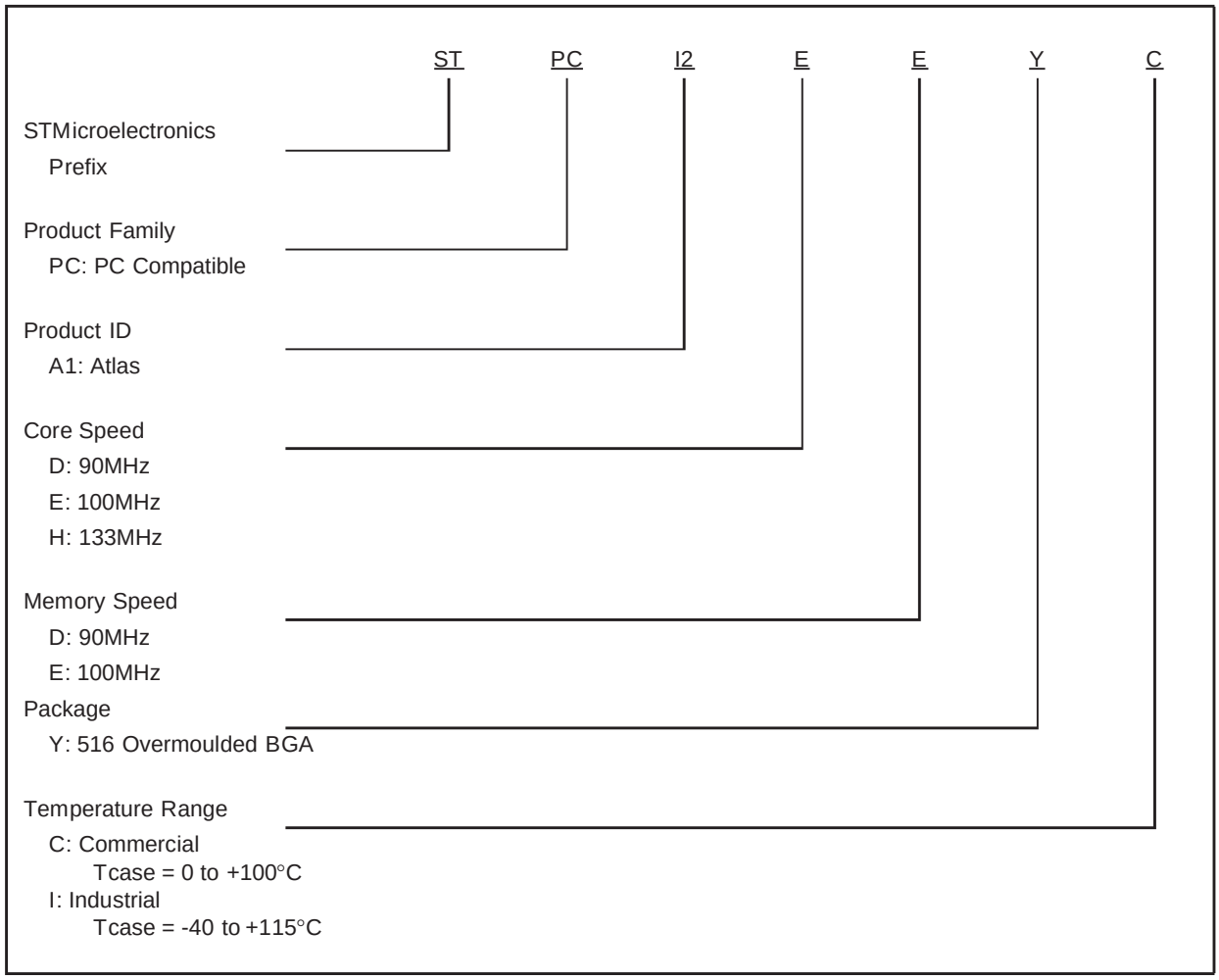
The PBGA is centered on board
There are no other devices
1 via pad per ground ball (8-mil wire)
40% copper on signal layers

Copper thickness:
- 17µm for internal layers
- 34µm for external layers

Airflow = 0
Board temperature taken at the center balls
Heat sink is 11.1°C/W

7 ORDERING DATA

7.1 ORDERING CODES



7.2 AVAILABLE PART NUMBERS

Part Number	Core Frequency (MHz)	CPU Mode	Memory Interface Speed (MHz)	Tcase Range (C)	Operating Voltage (V)
STPCI2DDYC	90	X1	90	0°C to +100°C	2.5± 0.25, 3.3V ± 0.3V
STPCI2EEYC	100	X1	100		
STPCI2HEYC	133	X1	100		
STPCI2DDYI	90	X1	90	-40°C to +100°C	
STPCI2EEYI	100	X1	100		
STPCI2HEYC	133	X1	100		