QRR0002
QUALITY & RELIABILITY REPORT

July 1999 June 2000

EPROM, Flash Memory, EEPROM, NVRAM and SMARTCARD Products

INTRODUCTION

STMicroelectronics manufactures a wide range of memory types which include:

Non-volatile memories: Flash memory, UV EPROM, OTP EPROM and EEPROMs. EPROM products are manufactured in both 1.5µm NMOS and 0.8µm to 0.35µm CMOS technology; Flash memories in 0.8µm to 0.35µm CMOS technology; OTP EPROMs in 0.8µm to 0.35µm and EEPROMs in 1.2µm to 0.6µm CMOS technology.

Packages for non-volatile memories include both ceramic FDIP and plastic PDIP, PLCC, SO and TSOP.

Non-volatile RAM: ZEROPOWER and TIMEKEEPER ranges are manufactured in 1.2-0.7µm HCMOS technology.

SMARTCARD (ST16 based) products are manufactured in 0.7µm CMOS technology.

Packages for ZEROPOWER and TIMEKEEPER products use a modified PDIP or SO with an additional "top hat" assembly mounted above and containing a Lithium battery and optionally a quartz crystal. The battery and crystal are sealed in the plastic cap with a plastic resin.

The results presented in this quarterly report cover the tests made from July 1999 June 2000. Regular reports are issued each quarter with the last years cumulative results.

Director of
Memory Products Group
Quality Control & Reliability

Attilio PANCHIERI

Find the report to the ST web site at **www.st.com**

CONTENT

Table 1. Final Average Outgoing Quality (AOQ)
July 1999 June 2000

Process	Electrical ppm				Visual ppm			
	3Q99	4Q99	1Q00	2Q00	3Q99	4Q99	1Q00	2Q00
UV EPROM								
CMOS	10	2	9	8	14	6	6	7
NMOS	0	0	0	0	0	0	0	0
OTP EPROM								
CMOS	10	9	13	9	7	2	4	4
FLASH								
CMOS	1	0	0	3	6	8	2	5
NVRAM								
CMOS	0	0	0	1	6	3	0	2
EEPROM								
CMOS	2	2	5	3	5	5	5	4
SMARTCARD (1)	-	0	0	0	-	0	0	5

Note: 1. Devices in TQFP package.

Table 2. Failure Rate Predictions (Fit)
July 1999 June 2000

Process	Actual Device hrs		Temperature Activation Energy (eV)	Voltage Acceleration Factor	Equivalent hrs 55 °C (x 10^6)	Life Test Failure	Failure Rate (Fit) Confidence Level	
	Dev. hrs (x 10^6)	Temp. (°C)					60%	90%
UV EPROM								
CMOS E6 -10%	2.178	140	0.6	4.0	595	0	1.53	3.86
CMOS E6 -30%	5.879	140	0.6	4.0	1.608	0	0.57	1.43
OTP EPROM								
CMOS E6-30%	3.520	140	0.6	4.0	912	0	1.00	2.52
FLASH								
CMOS T5 -20% (1)	2.264	140	0.6	4.0	586	0	1.56	3.93
CMOS T6	2.040	140	0.6	4.6	608	0	1.50	3.78
CMOS T6X -35%	12.921	140	0.6	4.6	3,851	0	0.24	0.60
EEPROM								
CMOS F4S	3.504	140	0.6	3.0	824	0	1.11	2.79
CMOS F6SP	3.971	140	0.6	4.6	1,432	0	0.64	1.60
NVRAM								
HCMOS S3	2.026	100	0.7	64	2,594	3	1.6	2.58
HCMOS 4DZ	3.175	125	0.7	6.0	1,467	1	1.37	2.65

Note: 1. Data related to QRR0001 due to phase out of T5 –20% upgrade process.

Table 3. NMOS E3/1.5µm Process UV EPROM Reliability Data, Die Related Tests
July 1999 June 2000

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M2764A		M27128		M27512	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,						
		– 48 hrs	390	0	80	0	160	0
		– 168 hrs	390	0	80	0	160	0
		– 500 hrs	390	0	80	0	160	0
		– 1000 hrs	390	0	80	0	80	0
Retention Bake	1008	250°C,						
		– 48 hrs	390	0	80	0	160	0
		– 168 hrs	390	0	80	0	160	0
		– 500 hrs	390	0	80	0	160	0

Table 4. CMOS E5/0.6µm Process (–35% upgrade) UV EPROM Reliability Data, Die Related Tests
July 1999 June 2000

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C256 (D) M87C257 (D)		M27C512 (D)		M27C801 (D)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,						
		– 48 hrs	930	0	2,406	0	80	0
		– 168 hrs	160	0	320	0	80	0
		– 500 hrs	160	0	320	0	80	0
		– 1000 hrs	160	0	320	0	80	0
Retention Bake	1008	250°C,						
		– 48 hrs	160	0	320	0	80	0
		– 168 hrs	160	0	320	0	80	0
		– 500 hrs	160	0	320	0	80	0

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 5. CMOS E6/0.6µm Process (–10% upgrade) UV EPROM Reliability Data, Die Related Tests
July 1999 June 2000

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C1001 (F)		M27C1024 (F)		M27C2001 (F)		M27C4001 (F)		M27C4002 (F)		M27C801 (F)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,												
		– 48 hrs	310	0	80	0	240	0	1,953	0	470	0	1,086	0
		– 168 hrs	310	0	80	0	240	0	560	0	470	0	470	0
		– 500 hrs	310	0	80	0	240	0	560	0	470	0	470	0
		– 1000 hrs	310	0	80	0	240	0	560	0	470	0	470	0
Retention Bake	1008	250°C,												
		– 48 hrs	310	0	80	0	240	0	560	0	470	0	470	0
		– 168 hrs	310	0	80	0	240	0	560	0	470	0	470	0
		– 500 hrs	310	0	80	0	240	0	560	0	470	0	470	0

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 6. CMOS E6DM/0.6µm Process UV EPROM Reliability Data, Die Related Tests
July 1999 June 2000

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C4001 (F)		M27C800 (F)		M27C160 (F)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,						
		– 48 hrs	-	-	-	-	70	0
		– 168 hrs	-	-	-	-	70	0
		– 500 hrs	-	-	-	-	70	0
		– 1000 hrs	-	-	-	-	70	0
Retention Bake	1008	250°C,						
		– 48 hrs	-	-	-	-	70	0
		– 168 hrs	-	-	-	-	70	0
		– 500 hrs	-	-	-	-	70	0

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 7. CMOS E6DM/0.5µm Process (–15% upgrade) UV EPROM Reliability Data, Die Related Tests
July 1999 June 2000

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C160 (F)	
			Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz, – 48 hrs – 168 hrs – 500 hrs – 1000 hrs	 14,800 720 720 720	 0 0 0 0
Retention Bake	1008	250°C, – 48 hrs – 168 hrs – 500 hrs	 690 690 690	 0 0 0

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 8. CMOS E6/0.35µm Process (–30% upgrade) UV EPROM Reliability Data, Die Related Tests
July 1999 June 2000

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C256 (F)		M27C512 (F)		M27C1001 (F)		M27C1024 (F)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,								
		– 48 hrs	1,262	0	1,730	0	711	0	320	0
		– 168 hrs	800	0	720	0	480	0	320	0
		– 500 hrs	800	0	720	0	480	0	320	0
		– 1000 hrs	800	0	720	0	480	0	320	0
Retention Bake	1008	250°C,								
		– 48 hrs	880	0	800	0	560	0	320	0
		– 168 hrs	880	0	800	0	560	0	320	0
		– 500 hrs	880	0	800	0	560	0	320	0

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 9. CMOS E6/0.35µm Process (–30% upgrade) UV EPROM Reliability Data, Die Related Tests
July 1999 June 2000

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C2001 (F)		M27C4002 (F)		M27C801 (F)		M27C160		M27C320 (F)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,										
		– 48 hrs	550	0	640	0	17,564	0	5,683	0	10,986	0
		– 168 hrs	80	0	640	0	960	0	160	0	80	0
		– 500 hrs	80	0	640	0	960	0	160	0	80	0
		– 1000 hrs	80	0	560	0	880	0	160	0	80	0
Retention Bake	1008	250°C,										
		– 48 hrs	80	0	640	0	960	0	160	0	80	0
		– 168 hrs	80	0	640	0	960	0	160	0	80	0
		– 500 hrs	80	0	560	0	880	0	160	0	80	0

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 10. UV EPROM Reliability Data, Package Related Tests (Ceramic Frit-Seal)
July 1999 June 2000

Test Procedure	MIL-STD-883 Procedure	Test Conditions	Samp.	Fail
Temperature Cycling	1010	–65 to 150°C, – 100 cycles – 500 cycles – 1000 cycles	 4,400 4,400 4,400	 0 0 0
– Fine Leak – Gross Leak	1014 1014	Test Condition A1 Test Condition C1	- -	- -
Solderability	2003	245°C, 5sec, Precondition Steam, 1hr	1,210	0

Table 11. CMOS E5/0.6µm Process (–35% upgrade) OTP EPROM Reliability Data, Die Related Tests
July 1999 June 2000

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C256 (D) M87C257 (D)		M27C512 (D)		M27C516 (D)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,						
		– 168 hrs	60	0	120	0	-	-
		– 500 hrs	60	0	120	0	-	-
		– 1000 hrs	60	0	120	0	-	-
Retention Bake	1008	150°C,						
		– 168 hrs	60	0	120	0	-	-
		– 500 hrs	60	0	120	0	-	-
		– 1000 hrs	60	0	120	0	-	-

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 12. CMOS E5/0.6µm Process (–35% upgrade) OTP EPROM Reliability Data, Package Related Tests
July 1999 June 2000

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C256 (D) M87C257 (D)		M27C512 (D)		M27C516 (D)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,						
		– 168 hrs	60	0	120	0	-	-
		– 500 hrs	60	0	120	0	-	-
		– 1000 hrs	60	0	120	0	-	-
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,						
		– 48 hrs	25	0	50	0	-	-
		– 96 hrs	25	0	50	0	-	-
		– 168 hrs	25	0	50	0	-	-
		– 240 hrs	-	-	-	-	-	-
Pressure Pot		121°C, 2Atm,						
		– 48 hrs	60	0	120	0	-	-
		– 96 hrs	60	0	120	0	-	-
		– 168 hrs	60	0	120	0	-	-
		– 240 hrs	60	0	120	0	-	-
Temperature Cycling	1010	–65 to 150°C,						
		– 100 cycles	60	0	60	0	-	-
		– 500 cycles	60	0	60	0	-	-
		– 1000 cycles	60	0	60	0	-	-
Solderability								
– PLCC/TSOP Packages	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	(See cumulative data on Table 19B)					
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	(See cumulative data on Table 19B)					

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 13. CMOS E6/0.6µm Process (–10% upgrade) OTP EPROM Reliability Data, Die Related Tests
July 1999 June 2000

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C1001 (F)		M27C1024 (F)		M27C2001 (F)		M27C4001 (F)		M27C4002 (F)		M27C801 (F)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,												
		– 168 hrs	780	0	60	0	-	-	420	0	-	-	60	0
		– 500 hrs	780	0	60	0	-	-	420	0	-	-	60	0
		– 1000 hrs	780	0	60	0	-	-	420	0	-	-	60	0
Retention Bake	1008	150°C,												
		– 168 hrs	780	0	60	0	-	-	420	0	-	-	60	0
		– 500 hrs	780	0	60	0	-	-	420	0	-	-	60	0
		– 1000 hrs	780	0	60	0	-	-	420	0	-	-	60	0

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 14A. CMOS E6/0.6µm Process (–10% upgrade) OTP EPROM Reliability Data, Package Related Tests
July 1999 June 2000

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C1001 (F)		M27C1024 (F)		M27C2001 (F)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,						
		– 168 hrs	780	0	60	0	-	-
		– 500 hrs	780	0	60	0	-	-
		– 1000 hrs	780	0	60	0	-	-
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,						
		– 48 hrs	325	0	25	0	-	-
		– 96 hrs	325	0	25	0	-	-
		– 168 hrs	300	0	25	0	-	-
		– 240 hrs	-	-	-	-	-	-
Pressure Pot		121°C, 2Atm,						
		– 48 hrs	780	0	60	0	-	-
		– 96 hrs	780	0	60	0	-	-
		– 168 hrs	780	0	60	0	-	-
		– 240 hrs	780	0	60	0	-	-
Temperature Cycling	1010	–65 to 150°C,						
		– 100 cycles	660	0	60	0	-	-
		– 500 cycles	660	0	60	0	-	-
		– 1000 cycles	600	0	60	0	-	-
Solderability								
– PLCC Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	(See cumulative data on Table 19B)					
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	(See cumulative data on Table 19B)					

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 14B. CMOS E6/0.6µm Process (–10% upgrade) OTP EPROM Reliability Data, Package Related Tests
July 1999 June 2000

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C4001 (F)		M27C4002 (F)		M27C801 (F)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,						
		– 168 hrs	420	0	-	-	60	0
		– 500 hrs	420	0	-	-	60	0
		– 1000 hrs	420	0	-	-	60	0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,						
		– 48 hrs	175	0	-	-	25	0
		– 96 hrs	175	0	-	-	25	0
		– 168 hrs	175	0	-	-	25	0
		– 240 hrs	25	0	-	-	-	-
Pressure Pot		121°C, 2Atm,						
		– 48 hrs	420	0	-	-	60	0
		– 96 hrs	420	0	-	-	60	0
		– 168 hrs	420	0	-	-	60	0
		– 240 hrs	420	0	-	-	60	0
Temperature Cycling	1010	–65 to 150°C,						
		– 100 cycles	360	0	-	-	60	0
		– 500 cycles	360	0	-	-	60	0
		– 1000 cycles	360	0	-	-	60	0
Solderability								
– PLCC Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	(See cumulative data on Table 19B)					
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	(See cumulative data on Table 19B)					

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 15. CMOS E6DM/0.5µm Process (–15% upgrade) OTP EPROM Reliability Data, Die Related Tests
July 1999 June 2000

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C160 (F)	
			Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz, – 168 hrs – 500 hrs – 1000 hrs	 180 180 180	 0 0 0
Retention Bake	1008	150°C, – 168 hrs – 500 hrs – 1000 hrs	 180 180 180	 0 0 0

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 16. CMOS E6DM/0.5µm Process (–15% upgrade) OTP EPROM Reliability Data, Package Related Tests
July 1999 June 2000

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C160 (F)	
			Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs	 - - -	 - - -
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V, – 48 hrs – 96 hrs – 168 hrs – 240 hrs	 - - - -	 - - - -
Pressure Pot		121°C, 2Atm, – 48 hrs – 96 hrs – 168 hrs – 240 hrs	 180 180 180 180	 0 0 0 0
Temperature Cycling	1010	–65 to 150°C, – 100 cycles – 500 cycles – 1000 cycles	 120 120 120	 0 0 0
Solderability				
– PLCC/TSOP Packages	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	(See cumulative data on Table 19B)	
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	(See cumulative data on Table 19B)	

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 17. CMOS E6/0.35µm Process (–30% upgrade) OTP EPROM Reliability Data, Die Related Tests
July 1999 June 2000

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C256B		M27C512		M27C1001		M27C1024	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,								
		– 168 hrs	900	0	660	0	720	0	720	0
		– 500 hrs	840	0	660	0	720	0	660	0
		– 1000 hrs	840	0	600	0	660	0	660	0
Retention Bake	1008	150°C,								
		– 168 hrs	900	0	660	0	720	0	720	0
		– 500 hrs	840	0	660	0	720	0	660	0
		– 1000 hrs	840	0	600	0	660	0	660	0

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 18. CMOS E6/0.35µm Process (–30% upgrade) OTP EPROM Reliability Data, Die Related Tests
July 1999 June 2000

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C2001		M27C4001		M27C800		M27C801	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,								
		– 168 hrs	420	0	120	0	120	0	60	0
		– 500 hrs	420	0	120	0	120	0	60	0
		– 1000 hrs	420	0	60	0	60	0	60	0
Retention Bake	1008	150°C,								
		– 168 hrs	420	0	120	0	120	0	60	0
		– 500 hrs	420	0	120	0	120	0	60	0
		– 1000 hrs	420	0	60	0	60	0	60	0

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 19A. CMOS E6/0.35µm Process (–30% upgrade) OTP EPROM Reliability Data, Package Related Tests
July 1999 June 2000

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C256B		M27C512		M27C1001		M27C1024	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,								
		– 168 hrs	900	0	660	0	720	0	720	0
		– 500 hrs	840	0	660	0	720	0	660	0
		– 1000 hrs	840	0	600	0	660	0	660	0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,								
		– 48 hrs	325	0	275	0	300	0	325	0
		– 96 hrs	325	0	275	0	300	0	325	0
		– 168 hrs	300	0	275	0	300	0	325	0
		– 240 hrs	-	-	-	-	-	-	-	-
Pressure Pot		121°C, 2Atm,								
		– 48 hrs	900	0	660	0	720	0	720	0
		– 96 hrs	900	0	660	0	720	0	720	0
		– 168 hrs	900	0	660	0	720	0	720	0
		– 240 hrs	840	0	660	0	720	0	660	0
Temperature Cycling	1010	–65 to 150°C,								
		– 100 cycles	780	0	660	0	720	0	720	0
		– 500 cycles	720	0	660	0	660	0	660	0
		– 1000 cycles	720	0	600	0	660	0	660	0
Solderability										
– PLCC Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	(See cumulative data on Table 19B)							
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	(See cumulative data on Table 19B)							

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 19B. CMOS E6/0.35µm Process (–30% upgrade) OTP EPROM Reliability Data, Package Related Tests
July 1999 June 2000

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C2001		M27C4001		M27C800		M27C801	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,								
		– 168 hrs	420	0	120	0	120	0	60	0
		– 500 hrs	420	0	120	0	120	0	60	0
		– 1000 hrs	420	0	60	0	60	0	60	0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,								
		– 48 hrs	175	0	50	0	50	0	25	0
		– 96 hrs	175	0	50	0	50	0	25	0
		– 168 hrs	175	0	50	0	50	0	25	0
		– 240 hrs	-	-	-	-	-	-	-	-
Pressure Pot		121°C, 2Atm,								
		– 48 hrs	420	0	120	0	120	0	60	0
		– 96 hrs	420	0	120	0	120	0	60	0
		– 168 hrs	420	0	120	0	120	0	60	0
		– 240 hrs	420	0	120	0	60	0	60	0
Temperature Cycling	1010	–65 to 150°C,								
		– 100 cycles	360	0	120	0	120	0	60	0
		– 500 cycles	360	0	120	0	120	0	60	0
		– 1000 cycles	360	0	60	0	120	0	60	0
Solderability										
– PLCC Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	Cumulative Sample/Fail = 1,024/0							
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	Cumulative Sample/Fail = 164/0							

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 20. CMOS T5/0.8µm Process (–20% upgrade) Flash Memory Reliability Data, Die Related Tests
July 1999 June 2000

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F256 (B)		M28F512 (B)		M28F101 (B)		M28F102 (B)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test (1)	1005	140°C, V_{CC} = 6V,f = 500kHz,								
		– 24 hrs	-	-	930	0	1,235	0	3,175	0
		– 168 hrs	-	-	930	0	985	0	1,790	0
		– 500 hrs	-	-	180	0	360	0	540	0
		– 1000 hrs	-	-	180	0	300	0	540	0
Retention Bake (1)	1008	150°C,								
		– 168 hrs	-	-	180	0	300	0	540	0
		– 500 hrs	-	-	180	0	300	0	540	0
		– 1000 hrs	-	-	180	0	300	0	540	0
Retention Bake	1008	250°C,								
		– 168 hrs	-	-	-	-	240	0	60	0
		– 500 hrs	-	-	-	-	240	0	60	0
		– 1000 hrs	-	-	-	-	240	0	60	0
Write/Erase Cycling		1,000 cycles	-	-	347	0	672	0	736	0
		10,000 cycles	-	-	-	-	448	0	-	-
Retention Bake	1008	150°C, 36 hrs	-	-	347	0	224	0	736	0

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.
2. A quarter of sample size was subjected to 10,000 Write/Erase cycles before operating life test and retention bake.

Table 21. CMOS T5/0.8µm Process (–20% upgrade) Flash Memory Reliability Data, Package Related Tests
July 1999 June 2000

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F256 (B)		M28F512 (B)		M28F101 (B)		M28F102 (B)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,								
		– 168 hrs	-	-	180	0	360	0	540	0
		– 500 hrs	-	-	180	0	360	0	540	0
		– 1000 hrs	-	-	180	0	360	0	540	0
		– 2000 hrs	-	-	-	-	-	-	-	-
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,								
		– 48 hrs	-	-	75	0	155	0	225	0
		– 96 hrs	-	-	75	0	155	0	225	0
		– 168 hrs	-	-	75	0	155	0	225	0
		– 240 hrs	-	-	75	0	125	0	225	0
Pressure Pot		121°C, 2Atm,								
		– 48 hrs	-	-	180	0	360	0	540	0
		– 96 hrs	-	-	180	0	360	0	540	0
		– 168 hrs	-	-	180	0	360	0	540	0
		– 240 hrs	-	-	180	0	360	0	540	0
Temperature Cycling	1010	–65 to 150°C,								
		– 100 cycles	-	-	180	0	330	0	540	0
		– 500 cycles	-	-	180	0	330	0	540	0
		– 1000 cycles	-	-	180	0	330	0	540	0
Solderability										
– TSOP/PLCC Packages	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	(See cumulative data on Table 25B)							

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 22A. CMOS T6/0.55µm Process Flash Memory Reliability Data, Die Related Tests
July 1999 June 2000

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F201 (B)		M28F210 (B) M28F211 (B) M28F220 (B)	
			Samp.	Fail	Samp.	Fail
Operating Life Test (1)	1005	140°C, V_{CC} = 6V,f = 500kHz,				
		– 24 hrs	685	0	15,210	0
		– 168 hrs	60	0	660	0
		– 500 hrs	60	0	660	0
		– 1000 hrs	60	0	660	0
Retention Bake (1)	1008	150°C,				
		– 168 hrs	60	0	660	0
		– 500 hrs	60	0	660	0
		– 1000 hrs	-	-	660	0
Retention Bake	1008	250°C,				
		– 168 hrs	-	-	-	-
		– 500 hrs	-	-	-	-
		– 1000 hrs	-	-	-	-
Write/Erase Cycling		1,000 cycles	160	0	2,784	0
		10,000 cycles	-	-	-	-
		100,000 cycles	-	-	-	-
Retention Bake	1008	150°C, 36 hrs	160	0	2,784	0

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.
1. A quarter of sample size was subjected to 10,000 Write/Erase cycles before operating life test and retention bake.

Table 22B. CMOS T6/0.55µm Process Flash Memory Reliability Data, Die Related Tests
July 1999 June 2000

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M29F102 M29F105		M29F002		M29F200 M29F100		M29F040 (C) M29W040		M29F400 M29W400	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test (1)	1005	140°C, V_{CC} = 6V,f = 500kHz,										
		– 24 hrs	2,736	0	1,890	0	4,650	0	555	0	750	0
		– 168 hrs	120	0	-	-	240	0	240	0	120	0
		– 500 hrs	120	0	-	-	240	0	240	0	120	0
		– 1000 hrs	120	0	-	-	240	0	240	0	120	0
Retention Bake (1)	1008	150°C,										
		– 168 hrs	120	0	-	-	240	0	210	0	120	0
		– 500 hrs	120	0	-	-	240	0	210	0	120	0
		– 1000 hrs	120	0	-	-	240	0	210	0	120	0
Retention Bake	1008	250°C,										
		– 168 hrs	-	-	-	-	-	-	-	-	-	-
		– 500 hrs	-	-	-	-	-	-	-	-	-	-
		– 1000 hrs	-	-	-	-	-	-	-	-	-	-
Write/Erase Cycling		1,000 cycles	827	0	192	0	763	0	730	0	184	0
		10,000 cycles	224	0	-	-	-	-	319	0	124	0
		100,000 cycles	-	-	-	-	-	-	191	0	92	0
		200,000 cycles	-	-	-	-	-	-	63	0	60	0
Retention Bake	1008	150°C, 36 hrs	603	0	192	0	763	0	411	0	184	0

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.
1. A quarter of sample size was subjected to 10,000 Write/Erase cycles before operating life test and retention bake.

Table 23A. CMOS T6/0.55µm Process Flash Memory Reliability Data, Package Related Tests
July 1999 June 2000

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F201 (B)		M28F211 (B) M28F210 (B) M28F220 (B)	
			Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,				
		– 168 hrs	60	0	660	0
		– 500 hrs	60	0	660	0
		– 1000 hrs	-	-	660	0
		– 2000 hrs	-	-	-	-
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,				
		– 48 hrs	25	0	275	0
		– 96 hrs	25	0	275	0
		– 168 hrs	25	0	275	0
		– 240 hrs	25	0	275	0
Pressure Pot		121°C, 2Atm,				
		– 48 hrs	60	0	660	0
		– 96 hrs	60	0	660	0
		– 168 hrs	60	0	660	0
		– 240 hrs	60	0	660	0
Temperature Cycling	1010	–65 to 150°C,				
		– 100 cycles	60	0	660	0
		– 500 cycles	60	0	659	0
		– 1000 cycles	-	-	659	0
Solderability						
– TSOP/SO Packages	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	(See cumulative data on Table 25B)			

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 23B. CMOS T6/0.55µm Process Flash Memory Reliability Data, Package Related Tests
July 1999 June 2000

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M29F102 M29F105		M29F002		M29F200 M29F100		M29F040 (C) M29W040		M29F400 M29W400	
			Fail	Fail	Samp.	Fail	Samp.	Samp.	Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,										
		– 168 hrs	120	0	-	-	240	0	240	0	120	0
		– 500 hrs	120	0	-	-	240	0	240	0	120	0
		– 1000 hrs	120	0	-	-	240	0	240	0	120	0
		– 2000 hrs	-	-	-	-	-	-	-	-	-	-
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,										
		– 48 hrs	50	0	-	-	100	0	105	0	50	0
		– 96 hrs	50	0	-	-	100	0	105	0	50	0
		– 168 hrs	50	0	-	-	100	0	105	0	50	0
		– 240 hrs	25	0	-	-	100	0	75	0	50	0
Pressure Pot		121°C, 2Atm,										
		– 48 hrs	120	0	-	-	240	0	240	0	120	0
		– 96 hrs	120	0	-	-	240	0	240	0	120	0
		– 168 hrs	120	0	-	-	240	0	240	0	120	0
		– 240 hrs	120	0	-	-	240	0	240	0	120	0
Temperature Cycling	1010	–65 to 150°C,										
		– 100 cycles	120	0	-	-	240	0	240	0	120	0
		– 500 cycles	120	0	-	-	240	0	240	0	120	0
		– 1000 cycles	120	0	-	-	236	0	175	0	120	0
Solderability												
– TSOP/SO Packages	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	(See cumulative data on Table 25B)									

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 24A. CMOS T6X/0.35µm Process Flash Memory Reliability Data
July 1999 June 2000

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M29F010 M29F102 M29F512		M29F002 M29F200		M29F040 M29F400	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V,f = 500kHz,						
		– 24 hrs	135,651	0	740	0	36,011	0
		– 168 hrs	780	0	240	0	720	0
		– 500 hrs	780	0	240	0	720	0
		– 1000 hrs	720	0	240	0	720	0
Retention Bake	1008	150°C,						
		– 168 hrs	900	0	240	0	660	0
		– 500 hrs	900	0	240	0	660	0
		– 1000 hrs	840	0	240	0	660	0
Retention Bake	1008	250°C,						
		– 168 hrs	60	0	-	-	-	-
		– 500 hrs	60	0	-	-	-	-
		– 1000 hrs	60	0	-	-	-	-
Write/Erase Cycling		1,000 cycles	22,885	0	316	0	10,022	0
		10,000 cycles	1,370	0	63	0	863	0
		100,000 cycles	288	0	-	-	352	0
		200,000 cycles	50	0	-	-	-	-
		1,000,000 cycles	50	0	-	-	-	-
Retention Bake	1008	150°C, 36 hrs	21,515	0	253	0	9,159	0

Table 24B. CMOS T6X/0.35µm Process Flash Memory Reliability Data
July 1999 June 2000

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M29W040 M29W400 M29W004		M29F800 M29F080		M29W800 M29W008		M29W160	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V,f = 500kHz,								
		– 24 hrs	12,269	0	41,346	0	150,306	0	8,924	0
		– 168 hrs	60	0	780	0	1,200	0	140	0
		– 500 hrs	60	0	780	0	1,200	0	140	0
		– 1000 hrs	60	0	780	0	960	0	140	0
Retention Bake	1008	150°C,								
		– 168 hrs	60	0	780	0	1,766	0	99	0
		– 500 hrs	60	0	780	0	1,476	0	99	0
		– 1000 hrs	60	0	780	0	1,407	0	99	0
Retention Bake	1008	250°C,								
		– 168 hrs	-	-	273	0	264	0	70	0
		– 500 hrs	-	-	273	0	230	0	70	0
		– 1000 hrs	-	-	150	0	82	0	70	0
Write/Erase Cycling		1,000 cycles	3,002	0	8,919	0	30,895	0	913	0
		10,000 cycles	-	-	256	0	1,289	0	49	0
		100,000 cycles	-	-	64	0	634	0	49	0
		200,000 cycles	-	-	-	-	128	0	-	-
		1,000,000 cycles	-	-	-	-	64	0	-	-
Retention Bake	1008	150°C, 36 hrs	3,002	0	8,663	0	29,606	0	864	0

Table 25A. CMOS T6X/0.35µm Process Flash Memory Reliability Data, Die Related Tests
July 1999 June 2000

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M29F010 M29F102				M29F400	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85% V_{CC} = 5V						
		– 168 hrs	780	0	240	0	720	0
		– 500 hrs	720	0	240	0	720	0
		– 1000 hrs	720	0	240	0	600	0
		– 2000 hrs	-	-	-	-	-	-
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V						
		– 48 hrs	325	0	100	0	300	0
		– 96 hrs	325	0	100	0	300	0
		– 168 hrs	325	0	100	0	300	0
		– 240 hrs	325	0	100	0	125	0
Pressure Pot		121°C, 2Atm,						
		– 48 hrs	900	0	240	0	720	0
		– 96 hrs	900	0	240	0	720	0
		– 168 hrs	900	0	240	0	720	0
		– 240 hrs	900	0	240	0	720	0
Temperature Cycling	1010	65°C to 150°C,						
		– 100 cycles	900	0	240	0	719	0
		– 500 cycles	900	0	240	0	719	0
		– 1000 cycles	895	0	240	0	719	0
Solderability								
– TSOP/PLCC Packages	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	(See cumulative data on Table 25B)					

Table 25B. CMOS T6X/0.35µm Process Flash Memory Reliability Data, Die Related Tests
July 1999 June 2000

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M29W400 M29W004		M29F080		M29W008			
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85% V_{CC} = 5V								
		– 168 hrs	60	0	780	0	810	0	-	-
		– 500 hrs	60	0	780	0	810	0	-	-
		– 1000 hrs	60	0	780	0	810	0	-	-
		– 2000 hrs	-	-	-	-	-	-	-	-
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V								
		– 48 hrs	25	0	325	0	371	0	-	-
		– 96 hrs	25	0	325	0	371	0	-	-
		– 168 hrs	25	0	325	0	371	0	-	-
		– 240 hrs	25	0	325	0	346	0	-	-
Pressure Pot		121°C, 2Atm,								
		– 48 hrs	60	0	780	0	1,425	0	-	-
		– 96 hrs	60	0	780	0	825	0	-	-
		– 168 hrs	60	0	780	0	825	0	-	-
		– 240 hrs	60	0	780	0	825	0	-	-
Temperature Cycling	1010	65°C to 150°C,								
		– 100 cycles	60	0	780	0	885	0	164	0
		– 500 cycles	60	0	780	0	885	0	164	0
		– 1000 cycles	60	0	780	0	821	0	164	0
Solderability										
– TSOP/PLCC Packages	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	Cumulative Sample/Fail = 1,235/0							

Table 26. CMOS F4/1.2µm Process EEPROM Reliability Data, Die Related Tests
July 1999 June 2000

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST93Cxxx	
			Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V,		
		– 24 hrs	2,880	0
		– 168 hrs	560	0
		– 500 hrs	560	0
		– 1000 hrs	80	0
		– 2000 hrs	80	0
Retention Bake	1008	150°C,		
		– 168 hrs	350	0
		– 500 hrs	350	0
		– 1000 hrs	350	0
		– 2000 hrs	50	0
Write/Erase Cycling		100,000 cycles	5,932	0
		1,000,000 cycles	-	-
Retention Bake	1008	150°C, 168 hrs	-	-

Table 27. CMOS F4/1.2µm Process EEPROM Reliability Data, Package Related Tests
July 1999 June 2000

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST93Cxxx	
			Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs	 280 280 280	 0 0 0
Pressure Pot		121°C, 2Atm, – 48 hrs – 96 hrs – 168 hrs – 240 hrs	 750 750 750 350	 0 0 0 0
Temperature Cycling	1010	–65 to 150°C, – 100 cycles – 200 cycles –40 to 150°C, – 500 cycles – 1000 cycles	 750 350 - -	 0 0 - -
Soderability				
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	(See cumulative data on Table 32B)	
– SO Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	(See cumulative data on Table 32B)	
Resistance to Surface Mount:				
– SO Package			(See cumulative data on Table 32B)	

Table 28A. CMOS F4S/1.0µm Process EEPROM Reliability Data, Die Related Tests
July 1999 June 2000

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST24C01 ST24W01		ST24C02 ST24W02		ST24C04 ST24W04		ST24C08		ST24C16 ST25C16		ST24LC21	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V,												
		– 24 hrs	2,880	0	2,880	0	2,880	0	-	-	-	-	-	-
		– 168 hrs	2,880	0	2,880	0	2,880	0	-	-	-	-	-	-
		– 500 hrs	480	0	480	0	480	0	-	-	-	-	-	-
		– 1000 hrs	-	-	-	-	-	-	-	-	-	-	-	-
Retention Bake	1008	150°C,												
		– 168 hrs	300	0	300	0	250	0	-	-	-	-	-	-
		– 500 hrs	300	0	300	0	250	0	-	-	-	-	-	-
		– 1000 hrs	300	0	300	0	250	0	-	-	-	-	-	-
Write/Erase Cycling		100,000 cycles	3,015	1 (a)	5,078	1 (a)	5,736	0	1,568	1 (a)	8,037	2 (a)	3,439	0
		1,000,000 cycles	-	-	-	-	-	-	-	-	-	-	-	-
Retention Bake	1008	150°C, 168 hrs	-	-	-	-	-	-	-	-	-	-	-	-

Note: a. Single bit fail.
Oxide quality improvements are addressed in two directions:
– Continuous quality improvement by fab task force.
– “Build in” robustness through product and process design.

Table 28B. CMOS F4S/1.0µm Process EEPROM Reliability Data, Die Related Tests
July 1999 June 2000

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M93C06		M93C46 M93S46		M93C56 M93S56		M93C66 M93S66		M28C16 (F)		M28C64D M28C64	
			Samp	Fail	Samp	Fail	Samp	Fail	Samp	Fail	Samp	Fail	Samp	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V,												
		– 24 hrs	-	-	5,280	0	-	-	1,920	0	80	0	560	0
		– 168 hrs	-	-	880	0	-	-	1,920	0	80	0	560	0
		– 500 hrs	-	-	880	0	-	-	320	0	80	0	560	0
		– 1000 hrs	-	-	-	-	-	-	-	-	-	-	560	0
Retention Bake	1008	150°C,												
		– 168 hrs	-	-	550	0	-	-	200	0	-	-	-	-
		– 500 hrs	-	-	550	0	-	-	200	0	-	-	-	-
		– 1000 hrs	-	-	550	0	-	-	200	0	-	-	-	-
Write/Erase Cycling		100,000 cycles	1,215	0	7,854	0	1,742	0	1,710	0	-	-	-	-
		1,000,000 cycles	-	-	-	-	-	-	-	-	-	-	-	-
Retention Bake	1008	150°C, 168 hrs	-	-	-	-	-	-	-	-	-	-	-	-

Table 29A. CMOS F4S/1.0µm Process EEPROM Reliability Data, Package Related Tests
July 1999 June 2000

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST24C01 ST24W01		ST24C02 ST24W02		ST24C04 ST24W04		ST24C08	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,								
		– 168 hrs	280	0	240	0	120	0	-	-
		– 500 hrs	280	0	240	0	120	0	-	-
		– 1000 hrs	280	0	240	0	120	0	-	-
Pressure Pot		121°C, 2Atm,								
		– 48 hrs	750	0	700	0	550	0	50	0
		– 96 hrs	750	0	700	0	550	0	50	0
		– 168 hrs	750	0	700	0	550	0	50	0
		– 240 hrs	350	0	300	0	150	0	-	-
Temperature Cycling	1010	–65 to 150°C,								
		– 100 cycles	800	0	750	0	550	0	50	0
		– 200 cycles	350	0	300	0	150	0	50	0
		–40 to 150°C,								
		– 500 cycles	-	-	-	-	-	-	-	-
		– 1000 cycles	-	-	-	-	-	-	-	-
Solderability										
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	(See cumulative data on Table 32B)							
– SO Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	(See cumulative data on Table 32B)							
Resistance to Surface Mount:										
– SO Package			(See cumulative data on Table 32B)							

Table 29B. CMOS F4S/1.0µm Process EEPROM Reliability Data, Package Related Tests
July 1999 June 2000

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST24C16 ST25C16		M93C46 M93S46	
			Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,				
		– 168 hrs	160	0	240	0
		– 500 hrs	160	0	240	0
		– 1000 hrs	160	0	240	0
Pressure Pot		121°C, 2Atm,				
		– 48 hrs	450	0	900	0
		– 96 hrs	450	0	900	0
		– 168 hrs	450	0	900	0
		– 240 hrs	200	0	350	0
Temperature Cycling	1010	–65 to 150°C,				
		– 100 cycles	450	0	1,050	0
		– 200 cycles	200	0	550	0
		– 500 cycles	-	-	-	-
		– 1000 cycles	-	-	-	-
		–40 to 150°C,				
		– 500 cycles	-	-	-	-
		– 1000 cycles	-	-	-	-
Solderability						
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	(See cumulative data on Table 32B)			
– SO Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	(See cumulative data on Table 32B)			
Resistance to Surface Mount:						
– SO Package			(See cumulative data on Table 32B)			

Table 29C. CMOS F4S/1.0µm Process EEPROM Reliability Data, Package Related Tests
July 1999 June 2000

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M93C56 M93S56		M93C66 M93S66		M28C16F		M28C64 M28C64D	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,								
		– 168 hrs	80	0	160	0	50	0	350	0
		– 500 hrs	80	0	160	0	50	0	350	0
		– 1000 hrs	80	0	160	0	50	0	350	0
Pressure Pot		121°C, 2Atm,								
		– 48 hrs	350	0	700	0	500	0	350	0
		– 96 hrs	350	0	700	0	500	0	350	0
		– 168 hrs	350	0	700	0	500	0	350	0
		– 240 hrs	100	0	400	0	50	0	350	0
Temperature Cycling	1010	–65 to 150°C,								
		– 100 cycles	400	0	600	0	50	0	250	0
		– 200 cycles	100	0	200	0	50	0	250	0
		– 500 cycles	-	-	-	-	50	0	250	0
		–1000 cycles	-	-	-	-	-	-	250	0
		–40 to 150°C,								
		– 500 cycles	-	-	-	-	-	-	-	-
		– 1000 cycles	-	-	-	-	-	-	-	-
Solderability										
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	(See cumulative data on Table 32B)							
– SO Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	(See cumulative data on Table 32B)							
– PLCC Package										
– TSOP Package										
Resistance to Surface Mount:										
– SO Package			(See cumulative data on Table 32B)							
– TSOP Package			(See cumulative data on Table 32B)							
– PLCC Package			(See cumulative data on Table 32B)							

Table 30A. CMOS F6-SP, 0,6µm Process EEPROM Reliability Data, Die Related Tests
July 1999 June 2000

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M24C01		M24C02/M34C02		M24C04		M24C08	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V,								
		– 24 hrs	2,400	0	960	0	960	0	960	0
		– 168 hrs	400	0	160	0	160	0	160	0
		– 500 hrs	400	0	160	0	160	0	160	0
		– 1000 hrs	-	-	-	-	-	-	-	-
Retention Bake	1008	150°C,								
		– 168 hrs	250	0	150	0	100	0	50	0
		– 500 hrs	250	0	150	0	100	0	50	0
		– 1000 hrs	250	0	150	0	100	0	50	0
Write/Erase Cycling		100,000 cycles	6,601	0	16,980	0	12,483	1 (a)	19,557	2 (a)
		1,000,000 cycles	-	-	-	-	-	-	-	-
Retention Bake	1008	150°C, 168 hrs	-	-	-	-	-	-	-	-

Note: a. Single bit fail.
Oxide quality improvements are addressed in two directions:
– Continuous quality improvement by fab task force.
– “Build in” robustness through product and process design.

Table 30B. CMOS F6-SP, 0,6µm Process EEPROM Reliability Data, Die Related Tests
July 1999 June 2000

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M24C16 M25C16		M24C32		M24C64		M28C64	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V,								
		– 24 hrs	2,400	0	2,880	0	-	-	2,880	0
		– 168 hrs	400	0	480	0	-	-	2,880	0
		– 500 hrs	400	0	480	0	-	-	2,880	0
		– 1000 hrs	-	-	-	-	-	-	2,880	0
Retention Bake	1008	150°C,								
		– 168 hrs	200	0	350	0	-	-	-	-
		– 500 hrs	200	0	350	0	-	-	-	-
		– 1000 hrs	200	0	350	0	-	-	-	-
Write/Erase Cycling		100,000 cycles	11,892	2 (a)	15,086	3 (a)	4,416	1 (a)	-	-
		1,000,000 cycles	-	-	-	-	-	-	-	-
Retention Bake	1008	150°C, 168 hrs	-	-	-	-	-	-	-	-

Note: a. Single bit fail.
Oxide quality improvements are addressed in two directions:
– Continuous quality improvement by fab task force.
– “Build in” robustness through product and process design.

Table 31A. CMOS F6-SP, 0,6µm Process EEPROM Reliability Data, Package Related Tests
July 1999 June 2000

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M24C01		M24C02		M24C04		M24C08	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,								
		– 168 hrs	40	0	120	0	160	0	40	0
		– 500 hrs	40	0	120	0	160	0	40	0
		– 1000 hrs	40	0	120	0	160	0	40	0
Pressure Pot		121°C, 2Atm,								
		– 48 hrs	200	0	900	0	850	0	400	0
		– 96 hrs	200	0	900	0	850	0	400	0
		– 168 hrs	200	0	900	0	850	0	400	0
		– 240 hrs	50	0	300	0	200	0	50	0
Temperature Cycling	1010	–65 to 150°C,								
		– 100 cycles	550	0	900	0	850	0	400	0
		– 200 cycles	50	0	300	0	200	0	50	0
		–40 to 150°C,								
		– 500 cycles	-	-	-	-	-	-	-	-
		– 1000 cycles	-	-	-	-	-	-	-	-
Soderability										
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	(See cumulative data on Table 32B)							
– SO Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	(See cumulative data on Table 32B)							
Resistance to Surface Mount:										
– SO Package			(See cumulative data on Table 32B)							

Table 31B. CMOS F6-SP, 0,6µm Process EEPROM Reliability Data, Package Related Tests
July 1999 June 2000

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M24C16 M25C16		M24C32		M24C64		M28C64	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,								
		– 168 hrs	4,800	0	200	0	-	-	1,890	0
		– 500 hrs	800	0	200	0	-	-	1,840	0
		– 1000 hrs	800	0	200	0	-	-	1,640	0
Pressure Pot		121°C, 2Atm,								
		– 48 hrs	500	0	550	0	-	-	1,800	0
		– 96 hrs	500	0	550	0	-	-	1,800	0
		– 168 hrs	500	0	550	0	-	-	1,800	0
		– 240 hrs	200	0	250	0	-	-	1,700	0
Temperature Cycling	1010	–65 to 150°C,								
		– 100 cycles	500	0	550	0	-	-	1,750	0
		– 200 cycles	200	0	250	0	-	-	1,700	0
		– 500 cycles	-	-	-	-	-	-	1,700	0
		– 1000 cycles	-	-	-	-	-	-	1,600	0
		–40 to 150°C,								
		– 500 cycles	-	-	-	-	-	-	-	-
		– 1000 cycles	-	-	-	-	-	-	-	-
Solderability										
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	(See cumulative data on Table 32B)							
– SO Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	(See cumulative data on Table 32B)							
– PLCC Package			(See cumulative data on Table 32B)							
– TSOP Package			(See cumulative data on Table 32B)							
Resistance to Surface Mount:										
– PDIP Package			(See cumulative data on Table 32B)							
– SO Package			(See cumulative data on Table 32B)							
– TSOP Package			(See cumulative data on Table 32B)							
– TSSOP Package			(See cumulative data on Table 32B)							
– PLCC Package			(See cumulative data on Table 32B)							

Table 32A. CMOS F6-DP, 0,6µm Process EEPROM Reliability Data, Die Related Tests
July 1999 June 2000

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M24128		M24256		M28256	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V,						
		– 24 hrs	800	0	400	0	400	0
		– 168 hrs	160	0	80	0	400	0
		– 500 hrs	160	0	80	0	400	0
		– 1000 hrs	-	-	-	-	400	0
Retention Bake	1008	150°C,						
		– 168 hrs	100	0	-	-	-	-
		– 500 hrs	100	0	-	-	-	-
		– 1000 hrs	100	0	-	-	-	-
Write/Erase Cycling		100,000 cycles	45	0	135	0	-	-
		1,000,000 cycles	-	-	-	-	-	-
Retention Bake	1008	150°C, 168 hrs	-	-	-	-	-	-

Table 32B. CMOS F6-DP, 0,6µm Process EEPROM Reliability Data, Package Related Tests
July 1999 June 2000

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M24128		M24256		M28256	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,						
		– 168 hrs	40	0	170	0	280	0
		– 500 hrs	40	0	170	0	280	0
		– 1000 hrs	40	0	170	0	280	0
Pressure Pot		121°C, 2Atm,						
		– 48 hrs	150	0	1,700	0	300	0
		– 96 hrs	150	0	1,700	0	300	0
		– 168 hrs	150	0	1,700	0	300	0
		– 240 hrs	50	0	550	0	300	0
Temperature Cycling	1010	–65 to 150°C,						
		– 100 cycles	150	0	1,700	0	300	0
		– 200 cycles	50	0	550	0	300	0
		– 500 cycles	-	-	-	-	300	0
		– 1000 cycles	-	-	-	-	300	0
		–40 to 150°C,						
		– 500 cycles	-	-	-	-	-	-
		– 1000 cycles	-	-	-	-	-	-
Solderability								
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	Cumulative Sample/Fail = 30/0					
– SO Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	Cumulative Sample/Fail = 240/0					
– PLCC Package			Cumulative Sample/Fail = 30/0					
– TSOP Package			Cumulative Sample/Fail = 30/0					
Resistance to Surface Mount:								
– SO Package			Cumulative Sample/Fail = 12,100/0					
– TSOP Package			Cumulative Sample/Fail = 1,800/0					
– TSSOP Package			Cumulative Sample/Fail = 4,750/0					
– PLCC Package			Cumulative Sample/Fail = 2,350/0					

Table 33. HCMOS S3/1.2µm Process ZEROPOWER NVRAM Reliability Data, Die Related Tests
July 1999 June 2000

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M48T08 M48T18	
			Samp.	Fail
Operating Life Test	1005	125°C, V_{CC} = 7V, f = 1MHz, – 168 hrs – 500 hrs – 1000 hrs	 2,336 1,967 1,963	 3 (a) 0 0

Table 34. HCMOS S3/1.2µm Process ZEROPOWER NVRAM Reliability Data, Package Related Tests
July 1999 June 2000

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M48T08 M48T18	
			Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs	 846 688 688	 1 (b) 1 (b) 1 (b)
Temperature Cycling Caphat	1010	–40 to 100°C, – 100 cycles – 500 cycles – 1000 cycles	 875 712 -	 0 1 (c) -

Note: a. Unit 1: Failed Ibat due to incomplete metal 1 etch causing high Ibat current.
Unit 2: Failed OSC start test due to particle at poli 1 gate oxide.
Unit 3: Failed functional test due to silicide residue along a word line gate.
These failures were from the period of ww19 and ww27 of 1999 only. This was during time period of equipment moves in our fab consolisation efforts.

Note: b. Units were over welded. (First samples from weld conversion. Corrections were implemented.)

Note: c.Negative battery lead detached from battery. Corrective actions implemented from Rayovac.

Table 35. HCMOS 4DZ/0.8µm Process ZEROPOWER NVRAM Reliability Data, Die Related Tests
July 1999 June 2000

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M48T59	
			Samp.	Fail
Operating Life Test	1005	125°C, V_{CC} = 6V, f = 1MHz, – 168 hrs – 500 hrs – 1000 hrs	 3,393 3,020 2,576	 1 (a) 0 0

Note: a. Failed for continuity on the battery plus end tab. FA results determined a bod wire bond stich weld.

Table 36. HCMOS 4DZ/0.8µm Process ZEROPOWER NVRAM Reliability Data, Package Related Tests
July 1999 June 2000

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M48T59	
			Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs	 616 616 616	 0 0 0
Hast	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V, – 96 hrs – 168 hrs – 240 hrs	 - - -	 - - -
Temperature Cycling	1010	–65 to 150°C, – 100 cycles – 500 cycles – 1000 cycles	 800 720 640	 0 0 0

Table 37. HCMOS 4DZS/0.7µm Process ZEROPOWER HYBRID MODULE Reliability Data, Die Related Tests
July 1999 June 2000

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M48T37 (5V)	
			Samp.	Fail
Operating Life Test	1005	125°C, V_{CC} = 6V, f = 1MHz, – 168 hrs – 500 hrs – 1000 hrs	 360 360 270	 0 0 0

Note: a. Single bit Failure

Table 38. HCMOS 4DZS/0.7µm Process ZEROPOWER HYBRID MODULE Reliability Data, Package Related Tests
July 1999 June 2000

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M48T37 (5V)	
			Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs	 160 160 120	 0 0 0
Hast	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V, – 96 hrs – 168 hrs – 240 hrs	 - - -	 - - -
Temperature Cycling	1010	–40 to 100°C, – 100 cycles – 500 cycles – 1000 cycles	 160 160 120	 0 0 0

Table 39. HCMOS 4PZ/0.6µm PROCESS ZEROPOWER SRAM Reliability Data, Die Related Tests
July 1999 June 2000

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M48Z35	
			Samp.	Fail
Operating Life Test	1005	125°C, V_{CC} = 6V, f = 1MHz, – 168 hrs – 500 hrs – 1000 hrs	 540 360 360	 0 0 0

Table 40. HCMOS 4PZ/0.6µm PROCESS ZEROPOWER SRAM Reliability Data, Package Related Tests
July 1999 June 2000

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M48Z35	
			Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs	 231 231 231	 0 0 0
Hast	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V, – 96 hrs – 168 hrs – 240 hrs	 - - -	 - - -
Temperature Cycling	1010	–40 to 100°C, – 100 cycles – 500 cycles – 1000 cycles	 240 240 240	 0 0 0

Table 41. ZEROPOWER HYBRID MODULE Reliability Data, Die Related Tests
July 1999 June 2000

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M48Z128 M48Z30	
			Samp.	Fail
Operating Life Test	1005	125°C, V_{CC} = 6V, f = 1MHz, – 168 hrs – 500 hrs – 1000 hrs	 896 896 896	 0 0 0

Table 42. ZEROPOWER HYBRID MODULE Reliability Data, Package Related Tests
July 1999 June 2000

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M48Z128 M48Z30	
			Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs	 216 167 109	 0 0 1 (a)
Hast	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V, – 96 hrs – 168 hrs – 240 hrs	 - - -	 - - -
Temperature Cycling	1010	–40 to 100°C, – 100 cycles – 500 cycles – 1000 cycles	 655 475 237	 0 0 1 (b)

Note: a. Leakage between two user pins. FA results showed solder migration between SRAM leads.

Note: b. FA results showed solder reflo web around SRAM.

Table 43. Statistical Process Control: CMOS E5/0.6µm Process (–35% upgrade) UV EPROM and OTP EPROM, Agrate - Italy F8 Diffusion Line

Key Process Parameters	3Q99	4Q99	1Q00	2Q00
	CPK	CPK	CPK	CPK
Pad Oxide Thickness	1.99	(*)	(*)	(*)
Silicon Nitride Thickness	1.69	(*)	(*)	(*)
Field Oxide Thickness	2.10	(*)	(*)	(*)
Gate Oxide Thickness	1.67	(*)	(*)	(*)
Interpoly Oxide Thickness	2.15	(*)	(*)	(*)
Intermediate Dielectric Thickness	1.70	(*)	(*)	(*)
Polysilicon 1 Thickness	2.46	(*)	(*)	(*)
Active Area Critical Dimensions	1.43	(*)	(*)	(*)
Policide Critical Dimensions	1.55	(*)	(*)	(*)

Key Electrical Parameters	3Q99	4Q99	1Q00	2Q00
	CPK	CPK	CPK	CPK
VT N-Channel Square Tr.	4.65	(*)	(*)	(*)
VT P-Channel Square Tr.	2.75	(*)	(*)	(*)
VT Natural Square Tr.	3.41	(*)	(*)	(*)
VT Memory Cell	2.03	(*)	(*)	(*)
I_{DON} N-Channel	2.29	(*)	(*)	(*)
N+ Active Area Contact Chain	9.29	(*)	(*)	(*)
AL-W Silicide Contact Chain Resistance	4.25	(*)	(*)	(*)

Note: (*) No production data during 4Q99, 1Q00, 2Q00.

Table 44. Statistical Process Control: CMOS E6DM/0.5µm Process (–15% upgrade) UV EPROM and OTP EPROM, Catania - Italy M5 Diffusion Line

Key Process Parameters	3Q99	4Q99	1Q00	2Q00
	CPK	CPK	CPK	CPK
Pad Oxide Thickness	2.35	2.76	3.14	(*)
Silicon Nitride Thickness	1.36	1.33	1.34	(*)
Field Oxide Thickness	1.57	1.78	1.78	(*)
Gate Oxide Thickness	2.09	2.12	1.91	(*)
Interpoly Oxide Thickness	1.80	1.85	3.05	(*)
Intermediate Dielectric Thickness	2.10	1.88	1.99	(*)
Polysilicon 1 Thickness	2.86	2.86	3.60	(*)
Active Area Critical Dimensions	1.71	1.56	1.52	(*)
Policide Critical Dimensions	1.38	0.95 (1)	1.35	(*)

Key Electrical Parameters	3Q99	4Q99	1Q00	2Q00
	CPK	CPK	CPK	CPK
VT N-Channel Square Tr.	1.87	2.2	2.48	(*)
VT P-Channel Square Tr.	2.35	1.81	1.38	(*)
VT Natural Square Tr.	4.10	4.53	3.72	(*)
VT Memory Cell	1.34	4.59	1.36	(*)
I_{DON} N-Channel	3.52	4.97	4.60	(*)
N+ Active Area Contact Chain	7.01	5.67	6.72	(*)
AL-W Silicide Contact Chain Resistance	2.36	2.38	2.94	(*)

Note: (*) No production data during 2Q00.

Note: 1. Fine tuning of measurement equipment software in progress.

Table 45. Statistical Process Control: CMOS E6/0.6µm Process (–10% upgrade) UV EPROM and OTP EPROM, Agrate - Italy F8 Diffusion Line

Key Process Parameters	3Q99	4Q99	1Q00	2Q00
	CPK	CPK	CPK	CPK
Pad Oxide Thickness	2.16	2.45	(*)	(*)
Silicon Nitride Thickness	2.11	1.85	(*)	(*)
Field Oxide Thickness	3.59	4.39	(*)	(*)
Gate Oxide Thickness	1.41	1.95	(*)	(*)
Interpoly Oxide Thickness	2.86	2.31	(*)	(*)
Intermediate Dielectric Thickness	1.95	1.52	(*)	(*)
Polysilicon 1 Thickness	2.52	2.86	(*)	(*)
Active Area Critical Dimensions	2.06	3.44	(*)	(*)
Policide Critical Dimensions	1.40	1.77	(*)	(*)

Key Electrical Parameters	3Q99	4Q99	1Q00	2Q00
	CPK	CPK	CPK	CPK
VT N-Channel 10 x 10µm	3.16	5.20	(*)	(*)
VT P-Channel 10 x 10µm	1.78	3.78	(*)	(*)
VT Natural 10 x 10µm	5.67	5.34	(*)	(*)
VT Memory Cell 0.65 x 0.65µm	2.34	1.50	(*)	(*)
I_{DON} N-Channel 10 x 10µm	1.82	2.81	(*)	(*)
N+ Active Area Contact Chain	4.20	4.39	(*)	(*)
AL-W Silicide Contact Chain Resistance	1.85	4.82	(*)	(*)

Note: (*) No production data during 1Q00, 2Q00.

Table 46. Statistical Process Control: CMOS E6/0.6µm Process (–10% upgrade) UV EPROM and OTP EPROM, Catania - Italy M5 Diffusion Line

Key Process Parameters	3Q99	4Q99	1Q00	2Q00
	CPK	CPK	CPK	CPK
Pad Oxide Thickness	1.65	1.38	1.72	(*)
Silicon Nitride Thickness	1.36	1.78	1.34	(*)
Field Oxide Thickness	1.57	1.34	2.28	(*)
Gate Oxide Thickness	2.09	2.12	1.91	(*)
Interpoly Oxide Thickness	1.61	1.47	1.87	(*)
N-Well Oxidation	3.35	2.62	3.45	(*)
Polysilicon 1 Thickness	1.85	1.33	1.56	(*)
Active Area Critical Dimensions	3.02	1.81	2.4	(*)
Policide Critical Dimensions	1.52	1.43	1.41	(*)

Key Electrical Parameters	3Q99	4Q99	1Q00	2Q00
	CPK	CPK	CPK	CPK
VT N-Channel Square Tr.	4.63	3.97	2.26	(*)
VT P-Channel Square Tr.	3.41	3.62	2.76	(*)
VT Natural Square Tr.	2.9	4.10	1.35	(*)
VT Memory Cell	1.86	2.05	1.9	(*)
I_{DON} N-Channel	4.07	3.20	2.02	(*)
N+ Active Area Contact Chain	8.92	6.20	4.42	(*)
AL-W Silicide Contact Chain Resistance	2.73	3.24	1.48	(*)

Note: (*) No data due to low production during 2Q00.

Table 47. Statistical Process Control: CMOS E6/0.35µm Process (–30% upgrade) UV EPROM and OTP EPROM, Agrate - Italy F8 Diffusion Line

Key Process Parameters	3Q99	4Q99	1Q00	2Q00
	CPK	CPK	CPK	CPK
Pad Oxide Thickness	1.95	2.81	2.13	1.44
Silicon Nitride Thickness	1.84	1.73	2.09	1.97
Field Oxide Thickness	3.43	3.81	2.96	3.31
Gate Oxide Thickness	1.83	1.77	1.90	1.92
Interpoly Oxide Thickness	2.86	2.31	2.14	2.53
N-Well Oxidation	1.85	1.52	1.61	1.42
Polysilicon 1 Thickness	2.83	2.51	2.89	1.57
Active Area Critical Dimensions	(*)	3.34	4.13	4.64
Policide Critical Dimensions	1.97	2.62	3.68	3.44

Key Electrical Parameters	3Q99	4Q99	1Q00	2Q00
	CPK	CPK	CPK	CPK
VT N-Channel Square Tr.	3.99	4.72	4.59	5.62
VT P-Channel Square Tr.	1.56	1.96	2.71	2.01
VT Natural Square Tr.	3.06	4.95	4.58	5.28
VT Memory Cell	1.35	1.33	1.38	1.45
I_{DON} N-Channel	5.41	4.90	4.49	3.95
N+ Active Area Contact Chain	10.42	13.24	6.37	5.82
AL-W Silicide Contact Chain Resistance	9.93	7.14	6.25	7.77

Note: (*) No data due to low production.

Table 48. Statistical Process Control: CMOS E6/0.35µm Process (–30% upgrade) UV EPROM and OTP EPROM, Catania - Italy M5 Diffusion Line

Key Process Parameters	3Q99	4Q99	1Q00	2Q00
	CPK	CPK	CPK	CPK
Pad Oxide Thickness	1.67	1.62	1.75	1.41
Silicon Nitride Thickness	2.22	1.78	1.78	1.95
Field Oxide Thickness	1.57	1.75	1.75	1.89
Gate Oxide Thickness	1.94	1.93	1.85	1.87
Interpoly Oxide Thickness	1.61	1.48	1.87	1.39
N-Well Oxidation	3.35	2.62	3.45	3.52
Polysilicon 1 Thickness	2.03	2.36	2.04	2.17
Active Area Critical Dimensions	1.81	1.42	2.48	1.75
Policide Critical Dimensions	2.01	2.94	3.17	2.1

Key Electrical Parameters	3Q99	4Q99	1Q00	2Q00
	CPK	CPK	CPK	CPK
VT N-Channel Square Tr.	4.65	7.42	1.63	6.15
VT P-Channel Square Tr.	5	4.63	2.45	3.13
VT Natural Square Tr.	7.3	6.71	3.6	5.57
VT Memory Cell	1.34	0.96 (1)	1.37	1.37
I_{DON} N-Channel	3.86	5.71	4.46	3.73
N+ Active Area Contact Chain	9.82	6.03	5.7	5.57
AL-W Silicide Contact Chain Resistance	3.8	2.2	2.41	3.23

Note: 1. Tuning of lithographic condition under evaluation.

Table 49. Statistical Process Control: CMOS T5/0.8µm Process (–20% upgrade) Flash Memory, Agrate - Italy F8 Diffusion Line

Key Process Parameters	3Q99	4Q99	1Q00	2Q00
	CPK	CPK	CPK	CPK
Field Oxide Thickness	2.28	2.82	2.80	2.72
Polysilicon 1 Thickness	2.68	3.70	2.37	2.07
Gate Oxide Thickness	1.54	2.05	2.01	1.98
Tunnel Oxide Thickness	2.53	2.12	1.74	1.91
ONO Bottom Oxide Thickness	1.50	1.34	1.38	1.87
ONO Nitride Thickness	1.50	1.54	1.43	1.47
ONO Top Oxide Thickness	2.38	2.58	1.83	1.43
Active Area Critical Dimensions	2.23	1.55	2.24	(*)
Polysilicon 2 Critical Dimensions	1.54	1.75	3.15	1.84

Key Electrical Parameters	3Q99	4Q99	1Q00	2Q00
	CPK	CPK	CPK	CPK
VT N-Channel 25 x 25 µm	1.53	2.72	2.16	5.08
VT P-Channel 25 x 25 µm	2.12	3.20	2.36	1.55
BV N-Channel 25 x 0.8 µm	1.59	3.00	2.64	2.19
BV P-Channel 25 x 0.9 µm	3.85	4.56	4.44	3.97
VT Memory Cell 0.8 x 0.8 µm	2.46	3.61	4.12	1.34
I_{DON} N-Channel 25 x 0.8 µm	1.44	1.33	1.37	2.53
Al+N+ Contact Chain	3.11	3.44	4.97	1.53
AL-W Silicide Contact Chain Resistance	2.35	4.78	6.09	1.35

Note: (*) No data due to low production during 2Q00.

Table 50A. Statistical Process Control: CMOS T6XU35/0.35µm Process Flash Memory, Agrate - Italy R1 Diffusion Line

Key Process Parameters	3Q99	4Q99	1Q00	2Q00
	CPK	CPK	CPK	CPK
Field Oxide Thickness	3.79	1.35	(*)	(*)
First Poly Thickness Gate	2.51	2.27	(*)	(*)
Gate Oxide HV Thickness	2.3	2.68	(*)	(*)
Tunnel Oxide Thickness	2.48	2.09	(*)	(*)
Gate Oxide LV Thickness	2.11	3.11	(*)	(*)
ONO Nitride Thickness	1.50	1.47	(*)	(*)
ONO Top Oxide Thickness	1.43	1.62	(*)	(*)
Active Area CD	2.64	2.33	(*)	(*)
Second Poly CD	3.06	2.63	(*)	(*)

Note: (*) No data due to low production during 1Q00, 2Q00.

Table 50B. Statistical Process Control: CMOS T6XU35/0.35µm Process Flash Memory, Agrate - Italy R1 Diffusion Line

Key Electrical Parameters	3Q99	4Q99	1Q00	2Q00
	CPK	CPK	CPK	CPK
LV-NCh LVS Saturation Current	5.61	3.22	(*)	(*)
LV-PCh LVS BV	8.5	2.56	(*)	(*)
LV-PCh LVS Saturation Current	5.61	4.16	(*)	(*)
LV-PCh SQ. VTh	4.57	3.31	(*)	(*)
HV-NCh SQ. VTh	4.73	2.49	(*)	(*)
HV-NCh LVS Saturation Current	2.77	3.71	(*)	(*)
HV-PCh BV	4.97	4.83	(*)	(*)
HV-PCh Saturation Current	5.85	5.41	(*)	(*)
HV-NCh LVS BV	4.97	4.81	(*)	(*)
LV-NCh LVS BV	4.57	5.54	(*)	(*)
LV-NCh SQ. VTh	3.42	3.71	(*)	(*)
HV-PCh SQ. VTh	7.80	2.21	(*)	(*)
Word Line Resistant	1.40	1.75	(*)	(*)
UV Erased Cell VTh	1.57	1.44	(*)	(*)
N+ Contact Chain	1.71	1.33	(*)	(*)

Note: (*) No data due to low production during 1Q00, 2Q00.

Table 51A. Statistical Process Control: CMOS T6XU35/0.35µm Process Flash Memory, Catania - Italy M5 Diffusion Line

Key Process Parameters	3Q99	4Q99	1Q00	2Q00
	CPK	CPK	CPK	CPK
Field Oxide Thickness	1.62	4.43	2.4	2.80
First Poly Thickness Gate	1.6	1.86	2.15	2.09
Gate Oxide HV Thickness	1.34	1.49	1.47	2.25
Tunnel Oxide Thickness	1.87	1.45	1.83	1.68
Gate Oxide LV Thickness	2.09	2.07	2.18	1.58
ONO Nitride Thickness	2.22	2.36	2.04	2.41
ONO Top Oxide Thickness	1.34	1.5	1.41	1.69
Active Area CD	1.37	1.49	1.34	1.48
Second Poly CD	0.65 (1)	1.05 (2)	0.85 (3)	0.91 (4)

Note: 1. Equipment alignement in progress.
2. Fine tuning on energy under evaluation.
3. Fine tuning of target in progress.
4. Fine tuning of measurement equipment software in progress.

Table 51B. Statistical Process Control: CMOS T6XU35/0.35µm Process Flash Memory, Catania - Italy M5 Diffusion Line

Key Electrical Parameters	3Q99	4Q99	1Q00	2Q00
	CPK	CPK	CPK	CPK
LV-NCh LVS Saturation Current	4.27	3.37	1.99	1.98
LV-PCh LVS BV	1.4	1.33	1.37	1.36
LV-PCh LVS Saturation Current	2.62	3.07	2.37	2.42
LV-PCh SQ. VTh	3.7	3.04	2.03	2.08
HV-NCh SQ. VTh	3.38	2.6	2.13	2.09
HV-NCh LVS Saturation Current	3.3	2.7	1.61	1.68
HV-PCh BV	5.02	4.7	1.97	2.53
HV-PCh Saturation Current	3.37	3.8	2.47	2.28
HV-NCh LVS BV	3.43	3.27	2.68	2.78
LV-NCh LVS BV	2.30	2.6	1.48	1.78
LV-NCh SQ. VTh	3.10	2.21	1.79	3.13
HV-PCh SQ. VTh	3.90	3.2	2.85	1.50
Word Line Resistant	1.53	1.9	1.86	1.68
UV Erased Cell VTh	1.84	2.34	1.94	1.52
N+ Contact Chain	2.39	1.52	1.59	1.59

Table 52. Statistical Process Control: CMOS F6 0.6µm Process EEPROM Memory, Agrate - Italy F8 Diffusion Line

Key Process Parameters	3Q99	4Q99	1Q00	2Q00
	CPK	CPK	CPK	CPK
Pad Oxide Thickness	2.16	2.45	2.77	2.45
Silicon Nitride Thickness	2.01	1.97	1.33	1.54
Field Oxide Thickness	2.28	2.82	2.80	2.72
Gate Oxide 1 Thickness	1.59	2.38	3.04	2.10
Gate Oxide 2 Thickness	2.53	2.45	2.80	2.27
Tunnel Oxide Thickness	2.69	2.72	2.62	2.53
Dielectric Thickness	1.93	1.89	2.04	1.99
Active Area Critical Dimensions	2.08	2.53	1.62	1.82
Policide Critical Dimensions	1.67	1.75	1.34	1.73
Poly Front Deposition Thickness	1.46	2.13	1.40	1.74
Contacts Critical Dimension	1.44	1.81	2.15	1.81

Key Electrical Parameters	3Q99	4Q99	1Q00	2Q00
	CPK	CPK	CPK	CPK
VT N-Channel 10 x 10µm	1.96	3.95	(*)	2.47
VT P-Channel 10 x 10µm	1.54	1.80	(*)	4.83
VT Natural 10 x 10µm	2.34	1.78	(*)	2.62
BV N-Channel 10 x 10µm	2.13	2.15	(*)	1.73
BV P-Channel 10 x 10µm	1.41	2.14	(*)	1.45
EBD-LVN	4.79	4.91	(*)	6.56
N+ Active Area Contact Chain	3.41	4.24	(*)	2.53
EBD-TUN	5.48	5.20	(*)	5.37

Note: (*) No data due to low production during 1Q00.

Table 53A. Statistical Process Control: CMOS M4S40-F-DLM/0.7µm Process Smartcard Product, Rousset - France Diffusion Line

Key Process Parameters	3Q99	4Q99	1Q00	2Q00
	CPK	CPK	CPK	CPK
Field Oxide Thickness	3.55	3.66	3.53	3.88
Gate Oxide Thickness	1.68	1.84	1.57	2.29
Tunnel Oxide Thickness	1.43	1.61	1.99	1.70
Polysilicium	1.97	2.05	1.78	2.48
Poly for Logic	2.35	2.56	2.68	2.73
Vapox	2.73	2.57	2.64	2.75
TEOS IMD1	2.34	1.94	2.07	2.67
USG IMD1	2.9	2.81	2.69	2.65

Table 53B. Statistical Process Control: CMOS M4S40-F-DLM/0.7µm Process Smartcard Product, Rousset - France Diffusion Line

Key Electrical Parameters	3Q99	4Q99	1Q00	2Q00
	CPK	CPK	CPK	CPK
Resist N+	1.63	1.63	3.25	2.22
Resist P+	2.72	2.72	2.42	3.13
Contact AL/N+	4.25	4.25	3.88	2.83
Contact AL/P+	2.82	2.82	1.77	1.92
Contact AL/POLY	3.37	3.37	3.77	3.29
VT En (25x25)	1.84	1.84	1.53	1.72
VT Ep (25x25)	1.31	1.34	0.72 (2)	1.38
VT Mc Erase	1.71	1.71	1.39	1.33
VT Mc Write	3.41	3.41	2.77	2.98
BV Diode N+/P-	2.53	2.53	2.87	2.66
BV Diode P+/N-	4.6	4.6	4.34	4.86
IDS En (25x0.8)	1.74	1.74	2.24	2.23
IDS Ep (25x0.8)	1.65	1.65	1.34	1.33
QBD Tunnel	1.34	0.78 (1)	1.35	1.52

Note: 1. Fine tuning in progress.
2. Fine tuning of the target in progress.

Table 54. Statistical Process Control: UV EPROM Ceramic Frit-Seal Package Assembly Line, Singapore

Key Process Parameters	3Q99	4Q99	1Q00	2Q00
	CPK	CPK	CPK	CPK
Shear Test (D.A.)	7.34	4.03	4.20	4.04
Stud Pull	1.84	1.86	1.82	1.92
Bond Strength (W.B.)	7.80	7.34	5.78	5.24
SN Thickness (Tin Plate)	1.74	2.17	1.94	1.67

Table 55. Statistical Process Control: TSOP Package Assembly Line, Singapore

Key Process Parameters	3Q99	4Q99	1Q00	2Q00
	CPK	CPK	CPK	CPK
Shear Test (D.A.)	2.73	2.97	3.73	4.69
Ball Shear (W.B.)	3.80	3.83	4.14	4.48
Bond Strength (W.B.)	2.91	2.70	4.20	3.44
Coplanarity	4.84	5.89	7.02	6.70
Plating Thickness	2.94	3.02	2.59	2.14

Table 56. Statistical Process Control: PLCC Package Assembly Line, Singapore

Key Process Parameters	3Q99	4Q99	1Q00	2Q00
	CPK	CPK	CPK	CPK
Shear Test (D.A.)	3.87	4.39	4.52	4.22
Ball Shear (W.B.)	3.24	3.15	3.63	3.85
Bond Strength (W.B.)	2.81	3.00	2.80	2.60
Plating Thickness	2.52	2.97	11.38	2.14
Coplanarity	8.40	7.78	2.28	11.40

If you have any questions or suggestion concerning the matters raised in this document please send them to the following electronic mail address:

ask.memory@st.com (for general enquiries)

Please remember to include your name, company, location, telephone number and fax number