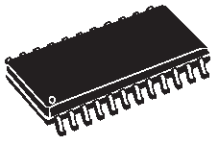
L6670

ANGULAR ACCELEROMETER

PRODUCT PREVIEW

- HIGH SENSITIVITY
- 7 BIT A/D CONVERTER (+ 1 SIGN BIT)
- 800HZ BANDWIDTH
- 300 rad/sec^2 FULL SCALE VALUE
- DIGITAL DECIMATOR FILTER
- SERIAL PORT OUTPUT

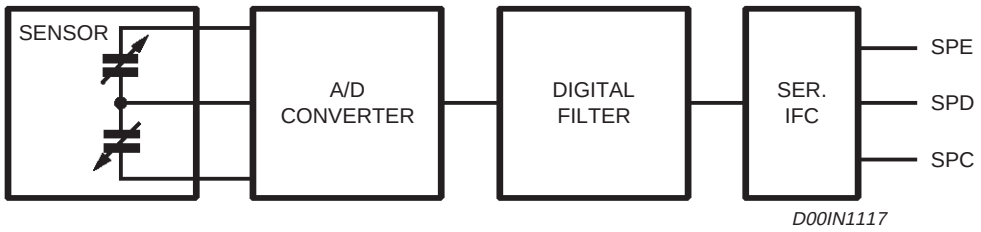


PACKAGE
ORDERING NUMBER: L6670

DESCRIPTION

The L6670 is a complete rotational accelerometer system based on a Σ-Δ architecture, followed by a digital decimator filter, featuring high sensitivity, 800Hz signal bandwidth and a complete serial port interface for a direct connection to microprocessor environment.

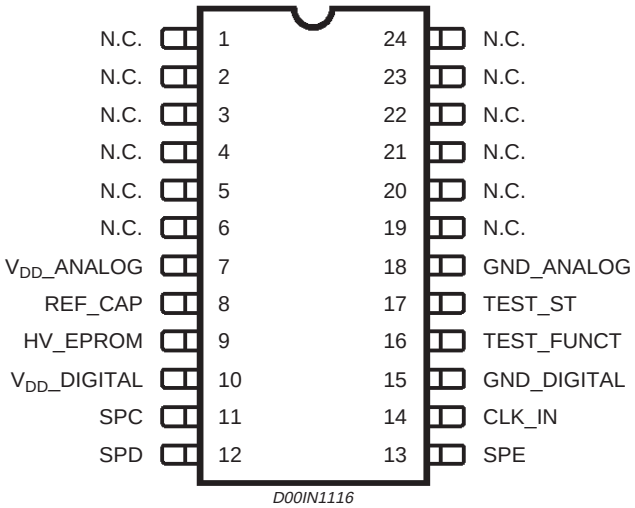
BLOCK DIAGRAM



PIN FUNCTION

N°. Pin	Name	Function Typ.	Condition
1 to 6	NC	Not Connected	
7	Vdd_Analog	Analog Voltage Supply	5V Typ.
8	Ref_Cap	Reference Voltage Bypass	
9	HV_Eprom	EPROM Programming Voltage (test mode only)	Tied to GND
10	Vdd_Digital	Digital Voltage Supply	5V Typ.
11	SPC	Serial Port Clock Signal	
12	SPD	Serial Port Data Signal	
19 to 24	NC	Not Connected	
13	SPE	Serial Port Enable Signal	
14	CLK_In	External Clock Input	
15	Gnd_Digital	Digital Ground Pin	
16	Test_Funct	Self Test	
17	Test_ST	Test Pin	Tied to GND
18	Gnd_Analog	Analog Ground Pin	

PIN CONNECTIONS (Top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$Vdd_{Analog\ Max}$	Maximum analog supply voltage	7	V
$Vdd_{Digital\ Max}$	Maximum digital supply voltage	7	V
V_{in}	Voltage Range on SPC, SPE, SPD, CLK_In, Test_Funct	-0.3 to Vdd_{Dig} + 0.3	

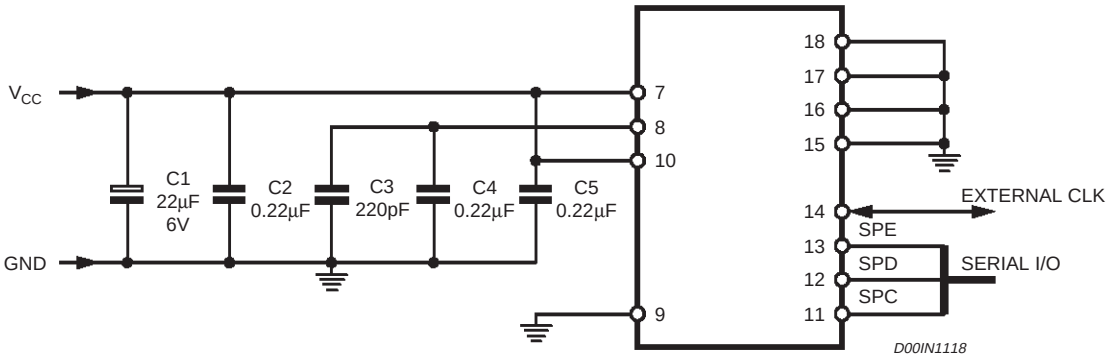
ELECTRICAL CHARACTERISTCS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
DC						
Vdd_{Analog}	Analog Supply Voltage		4.5	5.0	5.5	V
$Vdd_{Digital}$	Digital Supply Voltage		4.5	5.0	5.5	V
Idd_{Analog}	Analog Circuitry Supply Current			10		mA
$Idd_{Digital}$	Digital Circuitry Supply Current			10		mA
V_{ref}	Voltage on Ref_Cap pin			2.285		V
V_{oh}		(on SPD and Test_Funct) @ I_{oh} = 5mA		>4.0		V
V_{ol}		(on SPD and Test_Funct) @ I_{ofl} = 5mA		<1.0		V
V_{ih}		(on SPC, SPD, SPE, CLK_In and Test_Funct)		TBD		V
V_{il}		(on SPC, SPD, SPE, CLK_In and Test_Funct)		TBD		V
ADC						
	ADC SNR (30-800Hz, 4.48MHz Ext.Clk)			40		dB
	ADC Full Scale			300		rad/ sec2
	ADC Bandwidth			30-800		Hz
	ADC Dynamic Range			40		dB
	ADC Differential Linearity			TBD		
	ADC Integral Linearity			<5%		Full Scale
Mclk	Clock Frequency on CLK_In pin				6	MHz

SERIAL PORT TIMINGS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Pin SPC						
Fpc	SPC frequency		Mclk		11	MHz
Pin SPE						
Tec	SPE to SPEC		30		45	ns
Tce	SPC to SPE		30		45	ns
Twe	SPE low		1 SPC Period			
Pin SPD (input)						
Tds	SPD to SPC		10			ns
Tdh	SPC to SPD		5			ns
Pin SPD (output)						
Tpd	SPC to SPD		40ns (C_L = 20pF)			

Figure 1. Application Diagram

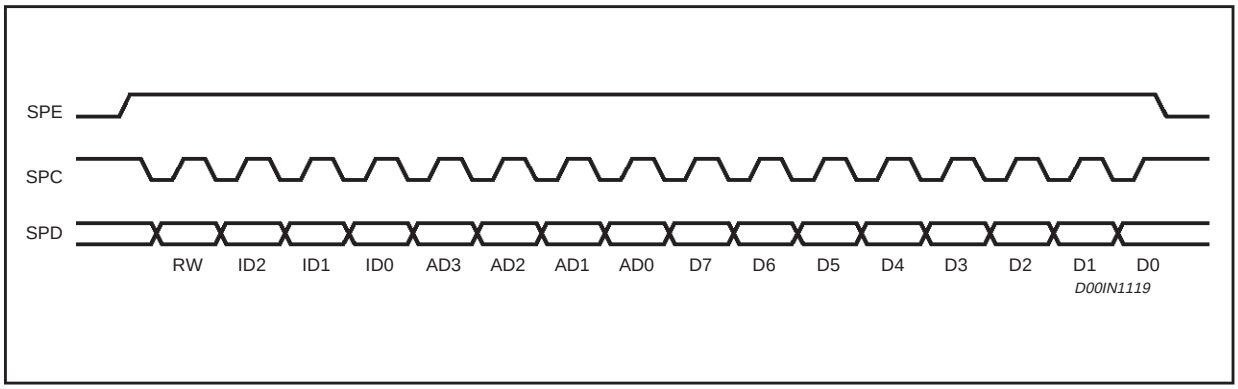


SERIAL PORT, REGISTERS, EPROM and TEST MODES

1. SERIAL PORT

1.1 READ & WRITE REGISTER

Figure 2.



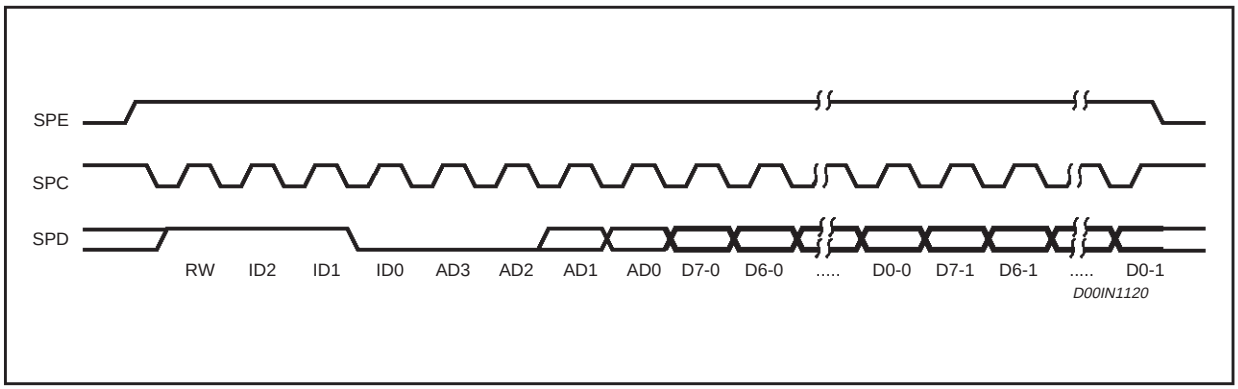
SPE is the Serial Port Enable. It goes high at the start of the transmission and goes back low at the end. SPC is the Serial Port Clock. It is stopped high when SPE is low (no transmission). SPD is the Serial Port Data. It is driven by the falling edge of SPC. It should be captured at the rising edge of SPC.

The Read Register or Write Register command consists of 16 clocks or bits. A bit duration is the time between two falling edges of SPC. The first bit (bit 0) starts at the first falling edge of SPC after the rising edge of SPE and the last bit (bit 15) starts at the last falling edge of SPC just before the falling edge of SPE.

- bit 0 : RW bit. When 0, the data (D7:0) is written into the MU05. When 1, the data (D7:0) from the MU05 is read. In this case, the MU05 will drive SPD at the start of bit 8.
- bit 1-3 : chip ID. The chip ID for the MU05 is ID(2:0)=110. The MU05 accepts the command only when the ID is valid (equal to 110).
- bit 4-7 : address AD(3:0). This is the address field for the registers. See section 2 for more details.
- bit 8-15 : data D(7:0). This is the data that will be written (read) into (from) the register which address is AD(3:0).

1.2 READ FIFO

Figure 3.



The Read FIFO command consists of 24 clocks or bits.

bit 0 : READ bit. The value is 1.

bit 1-3 : chip ID. ID(2:0)=110.

bit 4-7 : FIFO address.

The FIFO has four registers grouped into two banks. The first bank consists of the first and the second register. The first register is the one written first since the last read. The second bank consists of the third and fourth register.

000x: address for the first bank

001x: address for the second bank

bit 8-23: FIFO data.

The MU05 puts out first the data of the first register of the bank with the MSB first.

2. MU05 REGISTERS

The following is the address AD(3:0) of the registers.

AD(3:0) = 0100 CTRL_REG

This is the control register. It has 8 bits. The following gives the description of the bits.

Note: x means don't care value. Note: default value after power on reset is 0000 0000.

xxx1 xxxx: set to internal clock. By default the clock is external via pin VARIE.

xx1x xxxx: low power mode for the EPROM.

1xxx xxxx: clip on. The result of the multiplier is clipped to 0111 1111 when greater than 127 or 1000 0000 when less than -128.

xxxx 0001: bitstream in mode. The bitstream is sent in via pin Test_Funct while CK1M6 (bitstream clock) is sent in via pin VARIE and the output can be checked via the Serial Interface.

xxxx 0010: bitstream out mode. The bitstream is sent out to the pin SPC while CK1M6 is sent out to the pin SPE and phase_16 (digital filter clock) is sent out to the pin SPD. The pin Test_ST
must be set to 9 volts.

xxxx 0100: EPROM write. Writing to a register (see below) also addresses the EPROM and with the pin HV_Eprom = 15 volts, moving the pin Test_funct to 5 volts the EPROM is written with the same contents as with the register.

xxxx 0101: EPROM read. Sending a read register command reads the EPROM instead of the register.

xxxx 0110: sensor offset actuation.

xxxx 0111: sensor offset trim.

xxxx 1000: common mode feed-back trim.

AD(3:0)= 1000 GAIN_LSB

This is the 8 LSB of the gain for the digital filter.

AD(3:0)= 1001 GAIN_MSB

This is the 8 MSB of the gain for the digital filter.

AD(3:0)= 1010 OFFS_LSB

This is the 8 LSB of the offset for the digital filter.

AD(3:0)= 1011 OFFS_MSB

This is the 8 MSB of the offset for the digital filter.

AD(3:0)= 1100 CFB_TRIM

This is the 8 bits for the common mode feedback trim.

AD(3:0)= 1101 CS_ACT

This is the 8 bits for the sensor offset actuation.

AD(3:0)= 1110 CS_TRIM

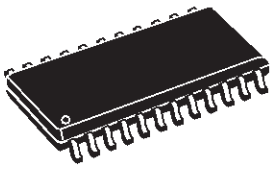
This is the 8 bits for the sensor offset trim.

AD(3:0)= 1111 EPROM_TEST

This is the 8 bits used to store the value of the EPROM threshold voltage.

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.10		0.30	0.004		0.012
A2			2.55			0.100
B	0.33		0.51	0.013		0.0200
C	0.23		0.32	0.009		0.013
D	15.20		15.60	0.598		0.614
E	7.40		7.60	0.291		0.299
e		1.27			0,050	
H	10.0		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
k	0° (min.), 8° (max.)					
L	0.40		1.27	0.016		0.050

OUTLINE AND MECHANICAL DATA



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