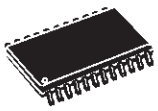
L6660

MILLI-ACTUATOR DRIVER

PRODUCT PREVIEW

- 90V BCD MIXED TECHNOLOGY
- SO24 PLASTIC SMD PACKAGE
- 4.5 TO 13.2V OPERATIVE VOLTAGE
- ±25 TO ±35V OUTPUT VOLTAGE RANGE SELECTABLE BY EXTERNAL RESISTORS
- FULL-WAVE RESONANT DC-DC CONVERTER USING SINGLE COIL FOR DUAL HIGH VOLTAGE GENERATOR WITH OUTPUT SLEW RATE CONTROL AND SELF CURRENT LIMITING FOR LOW EMI
- ±35V OR 0/+70V OPERATIVE VOLTAGE
- DRIVING CONFIGURATION MODES:
  1. SINGLE ENDED VOLTAGE MODE
  2. DIFFERENTIAL VOLTAGE MODE
  3. SINGLE ENDED CHARGE MODE
- DOUBLE OPERATIONAL AMPLIFIERS WITH 500KHZ GAIN BANDWIDTH PRODUCT AND LOAD DRIVING CAPABILITY FROM 0.4nF UP TO 24nF
- ANALOG VOLTAGE SHIFTING CIRCUITRY



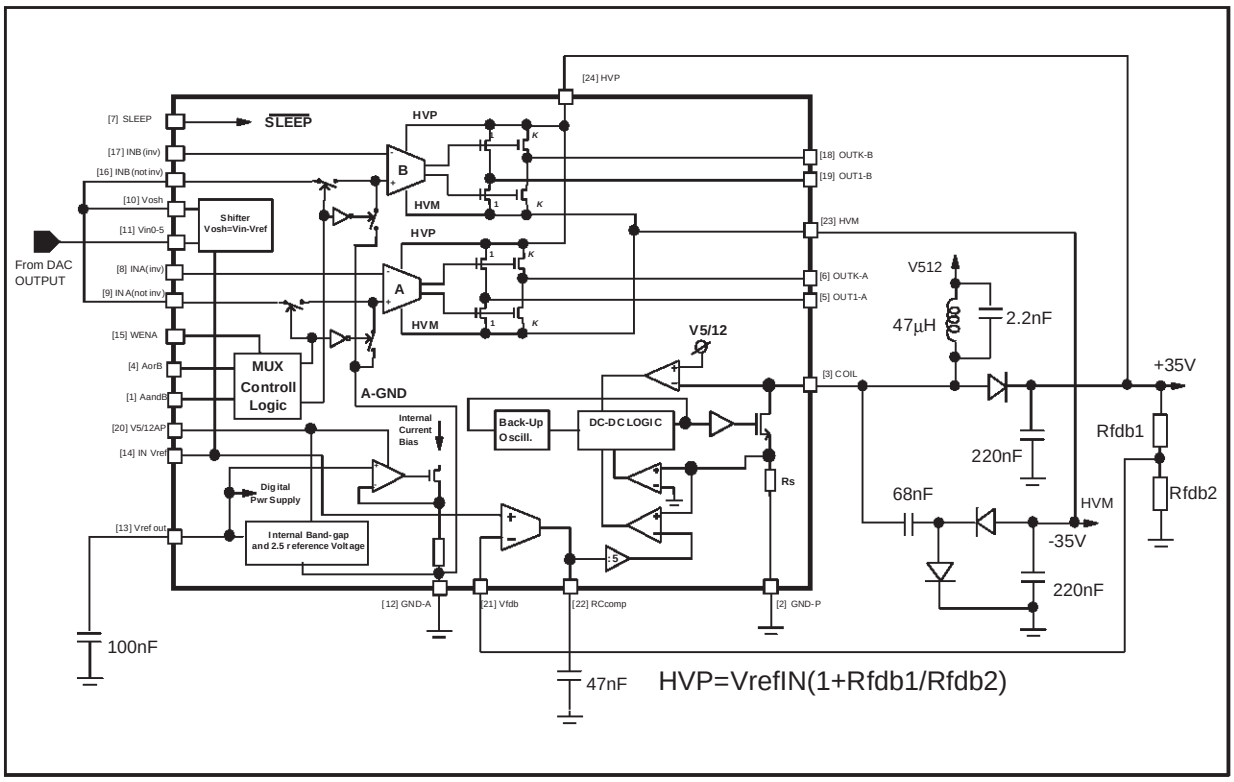
SO24(Shrink)

- INTERNAL 2.5V VOLTAGE REFERENCE
- POWER SAVING SLEEP MODE
- USER SPECIFIED INPUT REFERENCE (2.25V DC)

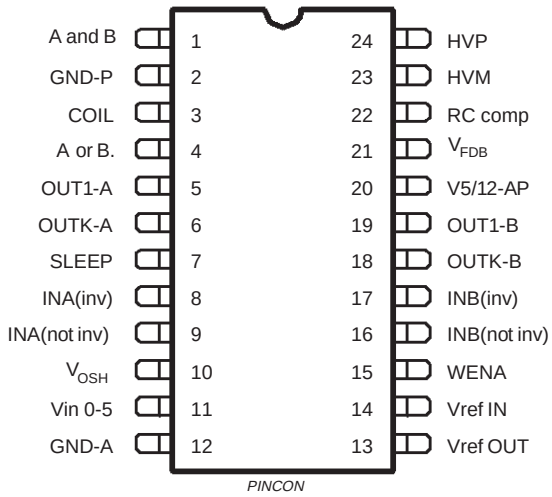
DESCRIPTION

The L6660 is a piezoelectric actuator driver.

BLOCK AND APPLICATION DIAGRAM



PIN CONNECTION SO24-SHIRINK (Top view)



PINCON

PIN FUNCTIONS

N.	Name	Description
1	AandB	MUX Enable (see Tab. 1).
2	GND-P	Power ground.
3	COIL	Coil for positive step UP and capacitor for negative charge.
4	AorB	MUX command Aor B input selection (0 = A; 1 = B).
5	OUT1-A	Output ampl.A.
6	OUTK-A	Hi current output ampl.A.
7	SLEEP	Sleep mode for stand-by condition (0=SLEEP 1=operative).
8	INA (inv)	Inverting input of A-amplifier.
9	INA (not inv)	Non Inverting input of A-amplifier.
10	Vosh	Analog level shifter output Vin-Vref (-2.5 to +2.5 dynamic range)
11	Vin 0-5	Analog level shifter input positive voltage.
12	GND-A	Analog ground.
13	V_{ref} OUT	Precise 2.5V reference voltage.
14	V_{ref} IN	Input for external reference voltage.
15	WENA	Multiplexer Enable, Falling Edge sensitive.
16	INB (not inv)	Non Inverting input of B-amplifier.
17	INB (inv)	Inverting input of B-amplifier.
18	OUTK-B	Hi current output ampl.B.
19	OUT1-B	Output ampl.B.
20	V5/12-AP	Analog&Power voltage supply 5 to 12V.
21	Vfdb	Feedback voltage for HVP regulator.
22	RC comp	DC-DC converter compensation network.
23	HVM	Negative High voltage generated op. amp. supply.
24	HVP	Positive High voltage generated op. amp. supply.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V512	Supply voltage pin 17 referred to Ground	14	V
HVP	Positive high voltage referred to HVM	75	V
HVM	Negative high voltage referred to Ground	-38	V
IN A&B	Amplifier input voltage common mode	±6	V
ΔV	Maximum difference between pin 20 and pins 8, 9, 16 & 17	17	V
T_{amb}	Operative Ambient Temperature	-20 to +80	°C
T_{stg}	Storage Temperature	-40 to +125	°C

All the voltage value are referred to ground unless otherwise specified.

ELECTRICAL CHARACTERISTICS

(All the following parameters are specified @ 27°C and V5/12 = 12V ±5%, unless otherwise specified.)

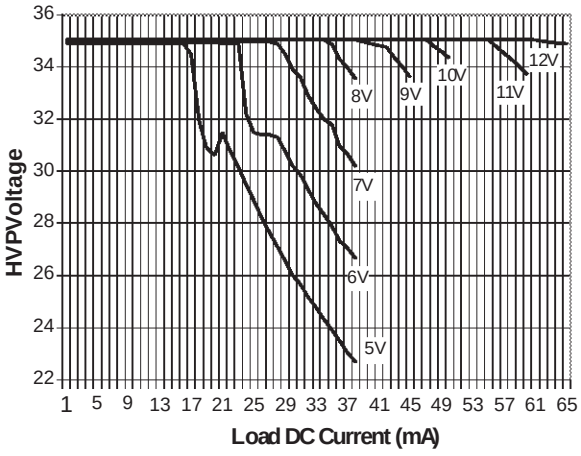
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$V_{5/12}$	Main power supply		4.5		13.2	V
HVP (1)	Output positive Voltage	Double Supply Voltage $V_{512} \geq 8$ Double Supply Voltage $V_{512} < 8$	27 18		35 35	V V
		Single Supply Voltage $V_{512} \geq 8$ Single Supply Voltage $V_{512} < 8$	27 18		70 35	V V
HVripple	HVP, HVM ripple Characterized only, Not Tested	External filter cap. 100nF I_{LOAD} = 0mA			0.8	V
I, hvp	Output current (see figure 1)					
I, hvm						
T_{op}	Time to operating condition				5	ms
F_{switch} (2)	Switching Frequency	Refer to Block diagram page1/10		300		kHz
$R_{ds,on}$	Boost transistor ON resistance				4	Ω
I_{boost}	Boost transistor current limiting				850	mA
V_{sup}	Minimum OpAmp supply Voltage (HVP if externally given)	Double Supply	V512 +4			V
		Single Supply	V512 +4			V
DC gain	OpAmp DC gain			130		dB
GBW	OpAmp Gain Bandwidth product	Cload 0.4nF to 24nF Double Supply Voltage		500		KHz
DCinp	OpAmp Input dynamic voltage	Double supply	-3.5		4.5	V
		Single supply	1.2		5	V
V_{out}	OpAmp Output dynamic voltage	Capacitive load	HVM		HVP	V
DC, I_{bias}	OpAmp Bias supply current (both)	|HVP| = |HVM| = 35V			9	mA
I_{out} (3)	OpAmp Dynamic Output Average current with external supply		-75		+75	mA
PSRR,P	OpAmp Positive power supply rejection ratio	@ 50kHz not tested in production		-50		dB
PSRR,N	OpAmp Negative power supply rejection ratio	@ 50kHz not tested in production		-50		dB
C_{load}	OpAmp Load capacitance range	Voltage mode Gain min 20dB	0.4		24	nF
C_{int}	OpAmp Integration capacitance	Charge mode Gain min 20dB	0.4		24	nF
K	OpAmp Current ratio OUTK/OUT1		9.8	10	10.2	

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Vout0	OpAmp Output Voltage with 0V Input Voltage	External feedback programmed for DC gain value <30V/V	-1		+1	V
$V_{ref}OUT$	Reference Voltage PIN13		2.4	2.5	2.6	V
I_{vref}	Reference Voltage Output Current		-1		+1	mA
$V_{ref, cap}$	Filter capacitor at PIN13		10		100	nF
$V_{shifted}$	Voltage shift value (V_{PIN11} - V_{PIN10})	1.0V ≤ Vin0-5 ≤ 3.5V	V_{ref}IN -2%	V_{ref}IN	V_{ref}IN +2%	V
Shifter Gain	Analog Voltage Shifter DC Voltage Gain $\frac{\Delta V_{10}}{\Delta V_{11}}$	$V_{PIN11} = V_{REFIN} \rightarrow V'_{10}$ $V_{PIN11} = V_{REFIN} + 0.1V \rightarrow V''_{10}$ $G = \frac{V'_{10} - V'_{10}}{0.1}$	0.975	1.00	1.025	
BW_{Vshift}	Shifter circuitry Band Width	3dB amplitude drop		2		MHz
V_{ref}IN	External reference voltage (PIN14)		2.0		2.6	V
I_{sleep}	Total current in Sleep Mode	PIN7 at 0 logic			800	µA
EAoff	DC-DC converter Error Amplifier Input voltage Offset (V_{PIN14}-V_{PIN21})	V_{ref}IN = 2.25V	-12		+12	mV
I_{EA}	Error amplifier Current Capability			±100		µA
HVP%	Total HVP precision	V_{ref} = 2.25V±0%	-4		+4	%
V_{logic0}	Voltage level for 0 logic at digital input pin (Pin 1-4-7-15)				0.9	V
V_{logic1}	Voltage level for 1 logic at digital input pin (Pin 1-4-7-15)		1.6			V
Z_{time}	Decay period for ΔV = |19V|	V_{ref} (Pin14) = 2.25V See Fig. 3 0°C < T_{case} < 80°C	140		340	µs
T_{op}	Operative period from Not Selected phase to Selected phase for each driver				4	µs

Note 1: Selectable by external resistors.
Note 2: Set by external Coil and Capacitor from 80 to 550KHz.
Note 3: Take into account the total power dissipation.

Figure 1. Load Regulation



OPERATIONAL AMPLIFIERS DESCRIPTION

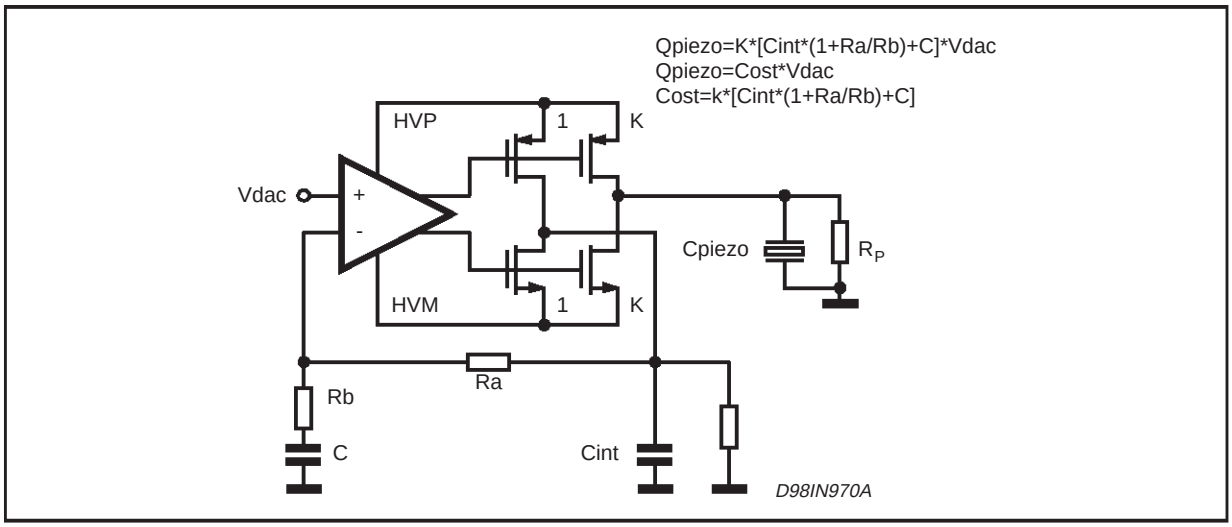
Each driver has two output stages scaled in current by a factor K = 10.
In voltage mode configuration the two outputs are shorted.
In charge mode configuration OUT1 drives a capacitor Cint and is closed in feedback, while OUTK drives the piezo, mirroring the current supplied to Cint, with a current multiplied by a K factor (see Fig.2).
The supply voltage can be internally generated by the DC-DC converter, or external, maintaining the DC-DC converter in sleep mode (PIN3 shorted to ground), in this case the supply voltage can be 0 to V5/12+4 minimum value up to 70V in single supply or V5/12+4 to 35V symmetrical to ground.

The drivers have 130dB DC gain and the Bandwidth is 500KHz. Stability is guaranteed with a minimum gain of 20dB, for a capacitive load in the range 0.4nF up to 24nF.

The drivers can be supplied with HVP-HVM (double supply mode) or with HVP-Ground (single supply mode). In both cases they can achieve a rail-to rail output dynamic range with an average load current up to ±75mA.

In double supply mode the input stage has -5V/+5V common mode dynamic range, while in single supply configuration it has 1.2V up to 10V input common mode dynamic range.

Figure 2. Charge Mode Configuration (configuration example; the final application depends on user needs according with Electrical Characteristics).



Input Multiplexer

MULTIPLEXER is controlled by internal logic with 3 digital inputs, supplied by IntVref (2.5V), it is compatible to 3.3V and 5V logic command signals, it allows to perform the following configuration:

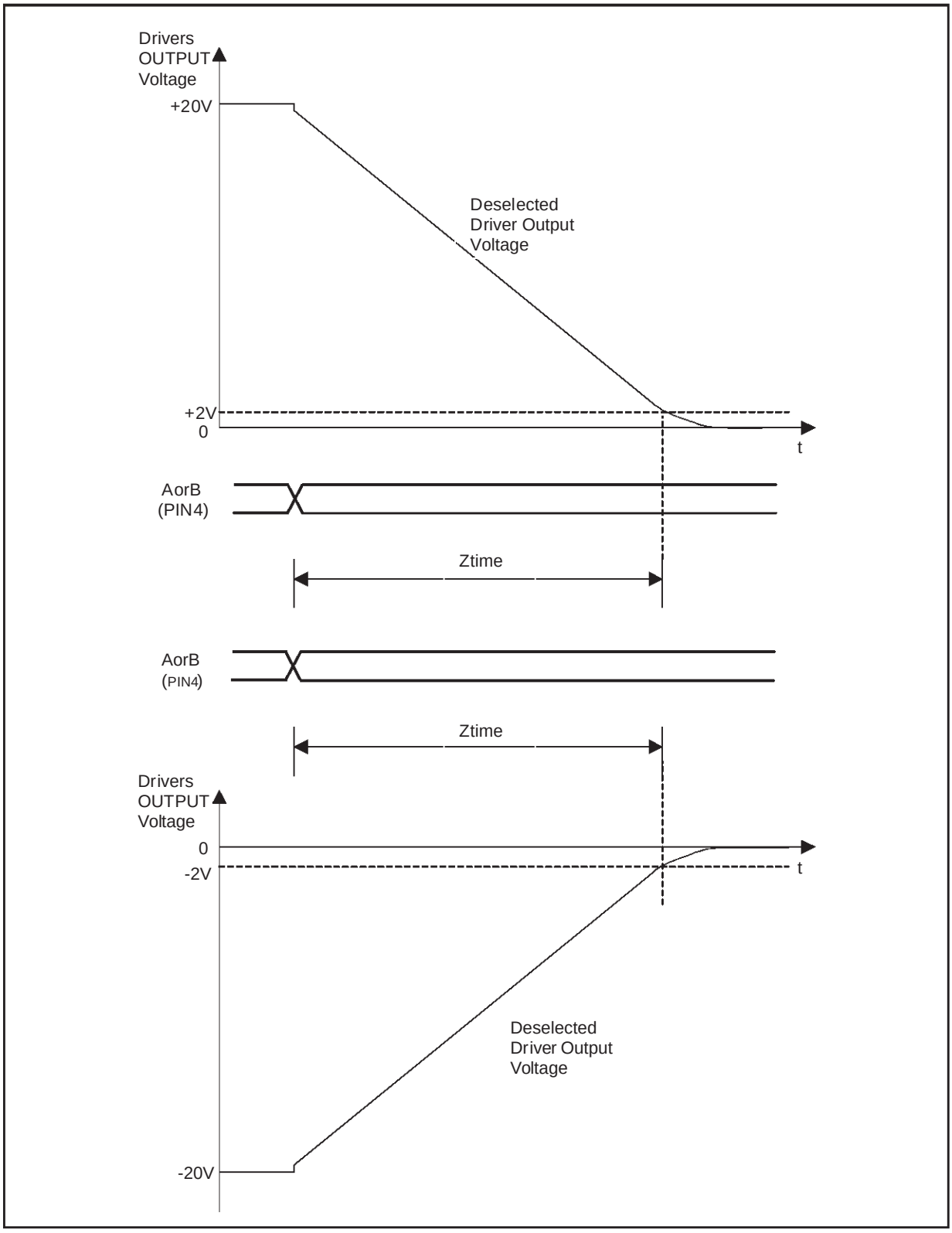
Table 1.

AandB (PIN1)	AorB (PIN4)	WENA (PIN15)	INA+Status	INB+Status	Comment
0	1	X	INA+ connected to AGND	INB+ connected to AGND	Both drv. inp. are disconnected from ext PIN and are connected to AGND
0	0	X	INA+ connected to PIN9	INB+ connected to PIN16	Both drv. inp. are accesible (MUX is transparent)
1	1	1	INA+ connected to PIN9	INB+ connected to AGND	INA is selected
1	0	1	INA+ connected to AGND	INB+ connected to PIN16	INB is selected
1	1	(F.E.)	INA+ connected to PIN9	INB+ connected to AGND	From WENA Falling Edge, changes on AorB (pin 4) will not change MUX state.
1	0	(F.E.)	INA+ connected to AGND	INB+ connected to PIN16	From WENA Falling Edge, changes on AorB (pin 4) will not change MUX state.

F.E. = Falling Edge

The MUX is at NOT inv. Inputs, and NO current flows through the MUX switches, because the driver input stage is designed with high impedance stage.

Figure 3. Not selected driver return to Zero Output voltage. Both drivers have the same behavior. The device is in operative condition and AandB (Pin1) and WENA (Pin15) are at 1 logic condition. The external feedback programmed for a DC gain value <30V/V.



Not selected Output return to 0V

Using the Multiplexer features and selecting just one driver, the second one, leaves its output voltage and "goes" to 0V (have showed in Fig. 3), in "long time" with controlled slope see table 1.

Voltage reference

An internal 2.5V voltage reference generator is connected to PIN13 (VrefOUT); it is based on an internal Band-Gap reference with a total precision of ±4% and a current capability of ±1.0mA, it is always present even in sleep mode condition.

This voltage is used to supply the internal MUX logic, allowing both 3.3V or 5V logic input signals, also the internal bias current is based on this reference.

The DC-DC converter reference voltage comes from PIN14 (VrefIN), so that the user can use an external voltage reference (from 2.0V up to 2.6V) or the internal one, in this case, just shorting together VrefOUT and VrefIN (PIN13 and PIN14).

Voltage Shifter

A voltage shifter is inserted to allow a ground symmetrical driving voltage on the piezo, starting from a positive (0V up to 5V) input signal coming from a positive supplied DAC. The DC Input-Output typical tranfer function is plotted in Fig. 4. This block works only in Double Supply mode, obviously it doesn't work if no negative supply is present. The voltage shifter output has not DC-current capability.

For more details see the application note.

DC-DC CONVERTER DESCRIPTION

The DC-DC converter inside the chip can be supplied from 5V up to 12V and has two parts, one to supply the positive and one to supply the negative voltage.

The DC-DC converter loop "measures" the HVP voltage by the EXTERNAL voltage divider and PIN21. The HVP voltage is programmed by two external resistors as shown in the block diagram, its value is:

$$V_{HVP} = V_{PIN21} \cdot (1 + \frac{R_{fdb1}}{R_{fdb2}})$$

The DC-DC control loop precision will be improved lower than ±4% respect external reference voltage and resistor voltage divider.

In Sleep Mode HVM is shorted to GND. When in single supply, HVM must be connected to GND.

The topology is a standard resonant full-wave boost one: the LC oscillation is kept running all the time and a set of comparators is used to synchronize turning on and off of the power MOS in order to have zero current and zero voltage switching and furthermore controlled rectification.

The step-up converter is designed to work in Linear mode, and an AC compensation network is required (RC-comp) to guarantee the stability in a wide operative range (i.e. changing coil, load, output and input voltage...).

According to the ouput voltage, the current loaded into the coil is changing like a Voltage Loop-Current Controlled system, and in every pulse there is a regulated power transfer to the load.

The resonant LC topology has been chosen in order to limit the voltage slew-rate across the coil within reasonable values and so, to minimize radiation problems.

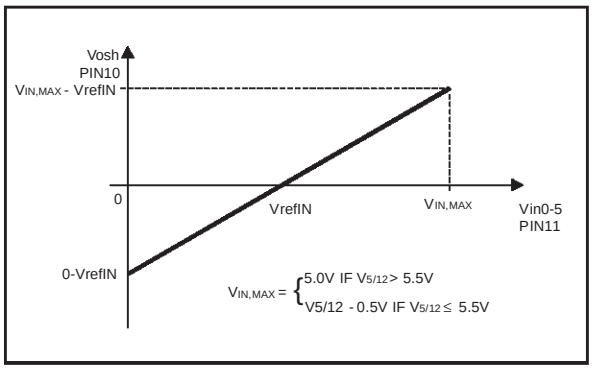
The negative converter is a simple charge transfer: it is supplied by the positive high voltage and it capacitively translates this positive voltage down to a negative one, obviously to limit radiation problems also the charge output has a limited slew-rate; moreover to reduce intermodulation phoenomenas the charge output is synchronized with the LC oscillations of the resonant boost.

This negative voltage is (not counting drops on external rectification diodes) in tracking with the positive one and so the negative output controller is not required.

If the drivers are supplied by HVP & HVM generated by external power supply the error amplifier output has to be connected to V5/12.

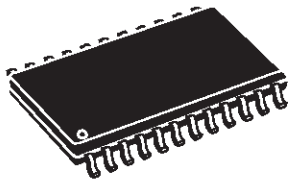
In the external supply configuration the maximum voltage between HVP and HVM (|HVP| + |HVM|) must not exceed 70V and maximum voltage between GND and HVM must be lower than 35V.

Figure 4. Shifter DC transfer function



DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.00			0.079
A1			0.25			0.010
A2	1.51		2.00	0.060		0.079
B	0.25	0.30	0.35	0.010	0.012	0.014
C	0.10		0.35	0.004		0.014
D	8.35		9.35	0.33		0.37
E	7.60		8.70	0.30		0.34
E1	5.02	6.10	6.22	0.20	0.24	0.244
e		0.65			0.025	
k	0° (min), 10° (max)					
L	0.25	0.50	0.80	0.010	0.020	0.031

OUTLINE AND MECHANICAL DATA



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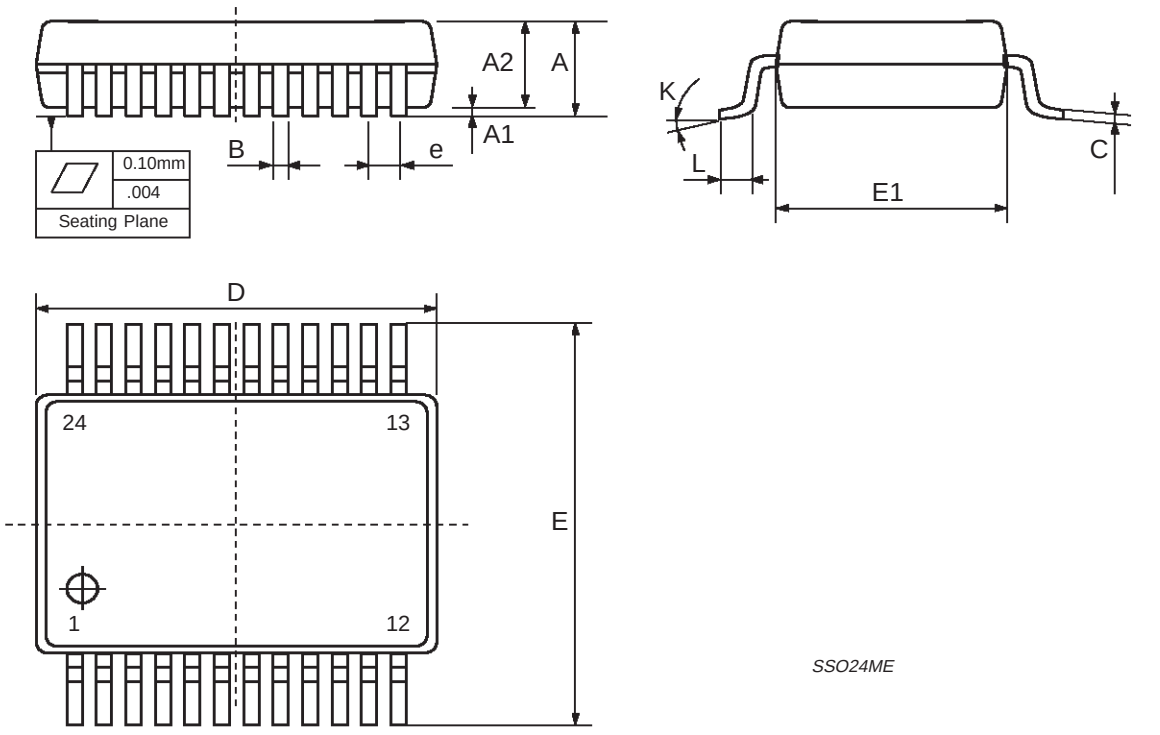

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