AN1235
APPLICATION NOTE

A.S.D.™

FLIP-CHIP CSP:PACKAGE DESCRIPTION AND RECOMMENDATIONS FOR USE

INTRODUCTION

The competitive market of portable equipment, notably the mobile phone market, is driven by a challenging development of highly integrated products. To allow manufacturers of portable equipment to reduce the dimension of their products, **STMicroelectronics** has developped packages with reduced size, thickness and weight in the form of the Flip-Chip CSP (Chip Scale Package).
The electrical performances of such components in Flip-Chip CSPs are improved thanks to shorter connections than the ones in standard plastic packages (as TSSOP, SSOP or BGA).

This **Flip-Chip CSP** family has been designed to fulfill the same quality levels and the same reliability performances as standard semiconductor plastic packages. That means these new flip-chip packages have to be considered as new surface mount devices which will be assembled on a printed circuit board without any special or additionnal process steps required. In particular this package does not require any extra underfill to increase reliability performances or to protect the device.
This package is reworkable and is compatible with existing pick and place equipment for board mounting.

The purpose of this document is to describe the Flip-Chip CSP features and to specify how our customers can use them.

This application note will address the following items :

- Product description
- Mechanical description
- Packing specifications and labelling description
- Recommended storage and shipping instructions
- Soldering assembly recommendations
- User responsability and returns
- Changes
- Delivery quantity
- Quality

PRODUCT DESCRIPTION

The wafer level process that **STMicroelectronics** has developped by attaching solder balls on I/Os pads of the active wafer side allows bumped dice to be produced the Flip-Chip CSPs. The I/O contact layout can be either matrix shape or set in periphery. No redistribution layer is used. This allows parasitic inductances coming from the redistribution metal tracks to be minimized.

The eutectic Sn63Pb37 bumps make this package compatible with standard reflow processes. The Bumps' dimension (315 µm bumps diameter) allows the pick and place process to be compatible with existing equipment (in particular with equipment used for BGA packages) and makes it compatible with the PCB design rules used for standard ICs.

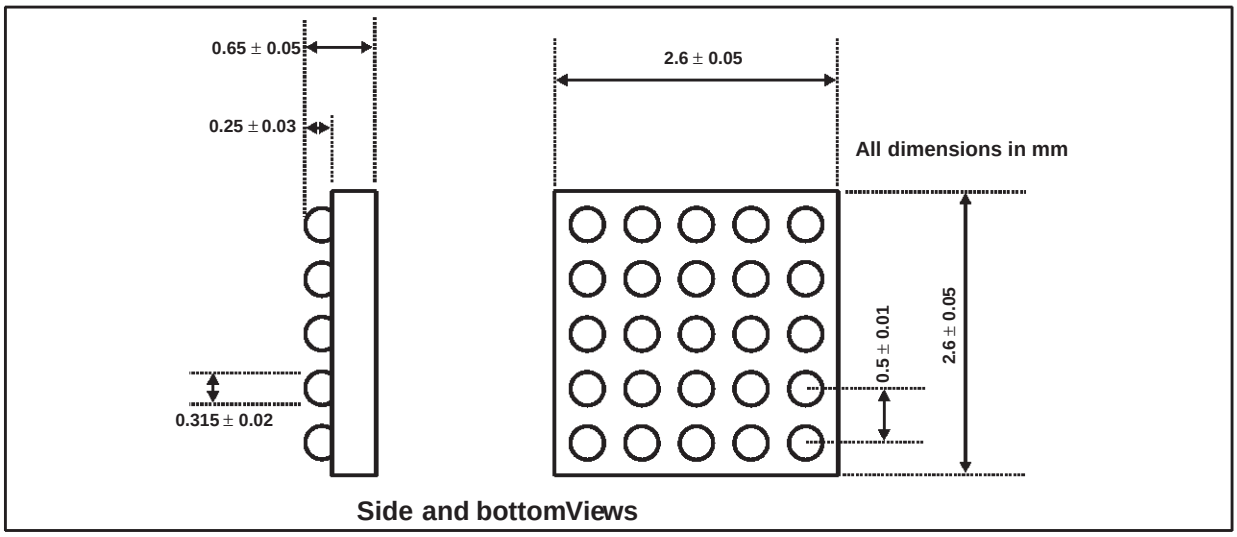
These components are delivered in tape&reel with the bumps turned down (placed on the bottom of the carrier tape cavity). The other face of the component is flat and allows picking as in the standard SMD packages.

Devices are 100% electrically tested before packing. The product references are marked on the flat side of the Flip-Chip CSP.

MECHANICAL DESCRIPTION

Mechanical dimensions of Flip-Chip CSPs are provided through a product example in the figure 1 below. Bumps are in Sn63Pb37 alloy with an eutectic melting point of 183°C. Die size and bumps count are adapted to the connection requirements.

Fig. 1: Mechanical dimensions of a 5 x 5 bumps matrix array (sample)

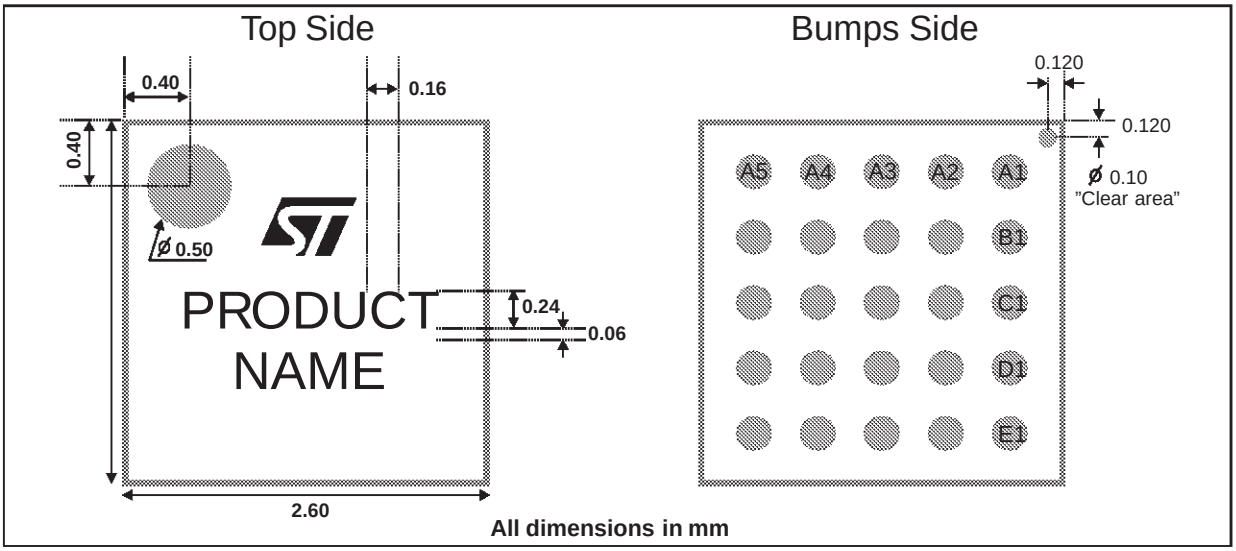


The Flip-Chip CSPs' tolerance on bumps diameter and bumps height are very narrow. This constant bumps shape insures a good coplanarity between bumps. Optical measurements performed through vertical focuses show a 60µm maximum bumps coplanarity.

The product marking for both bumps side and top side is shown on figure 2 below (product example). The Flip-Chip CSP has a pin marker (A1) on both the top and bottom sides so that the face of the component can be easily determined before and after assembly.The dots marked both on the top side and on the bumps side have been designed so that they can be detected by standard vision systems.

Marking dimensions are, of course, linked to the die size.

Fig. 2: Flip-Chip CSP marking example



PACKING SPECIFICATIONS & LABELLING DESCRIPTION

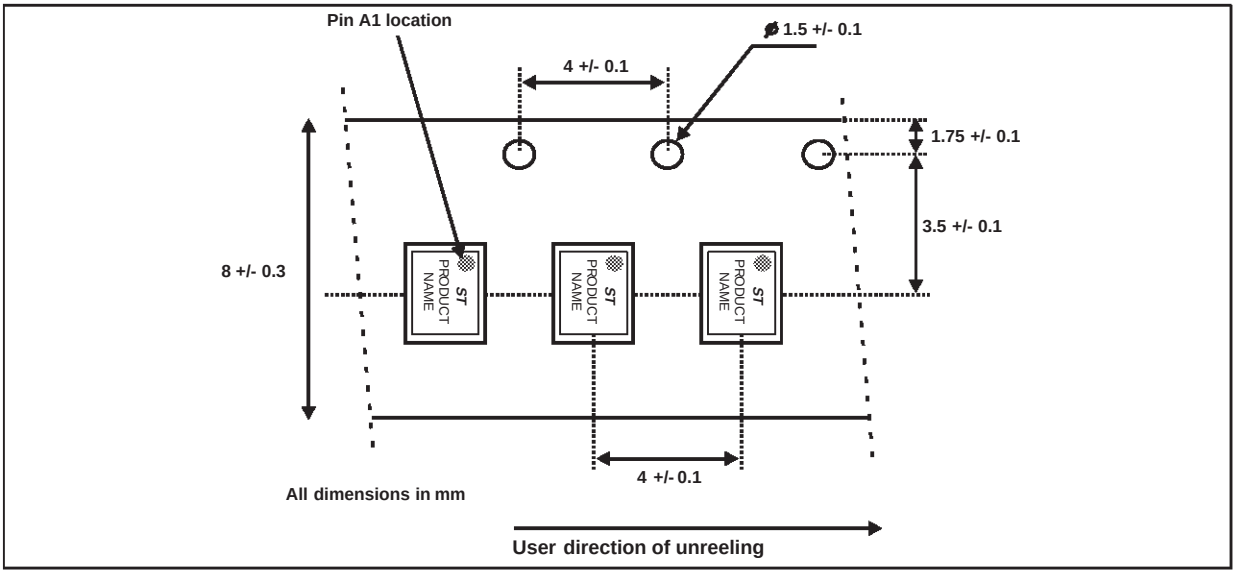
The Flip-Chip CSP is delivered in tape & reel to be fully compatible with standard high volume SMD components. The features of tape & reel materials are in accordance with standards EIA-481. All features not specified in this section are in accordance with EIA-481 standards.

1. Carrier tape

The Flip-Chip CSPs are placed in carrier tape with bumps side facing the bottom of the cavity so that the components can be picked-up by their top side. No flipping of the package is necessary for mounting on PCB. Flip-Chip CSPs are positionned in the carrier tape with pin A1 nearest the round sprocket hole. Carrier tape mechanical dimensions and Flip-Chip CSP positionning is shown in figure 3 below.

Note: 12 mm carrier tape width may be used for a larger die size to be in line with EIA standards.

Fig. 3: Layout of Flip-Chip CSPs in carrier tape (8mm carrier tape sample)



The cavities in the carrier tape have been designed to avoid any damage to the components. No hole is present in the cavity in order to avoid any impact or any external contamination to the solder bumps.

For Flip-Chip CSPs larger than 2 mm x 2 mm, the 8 mm width and 4 mm pitch carrier tape is designed to allow a maximum component tilt of 5° and a maximum lateral movement of 0.3 mm.

The embossed carrier tape is in a black conductive homogeneous polycarbonate material. The presence of water extractable ionics material inside the carrier tape is less than 5 ppm (test method 5011 MIL-STD-883C). This material is guaranteed not have any out-gassing or chemical leaking (especially sulphur or chlorides). Conductivity is guaranteed to be constant and homogeneous and not affected by shelf life or humidity. The material will not break when bent nor will rub off, powder or flake.

The carrier tape tensile break force is 115N (according to test method ATSM-D638)

2. Cover tape

The carrier tape is sealed with a transparent, static dissipative, polyester film cover tape with a heat activated adhesive. The cover tape tensile strength break is 10.6N (according to test method ATSM-D3759).

The peeling force of the cover tape is between 6 gf and 60 gf by performing the testing method EIA 481-1 and IEC 286-3: cover tape is peeled back in the direction opposite to the carrier tape travel ; the angle between the cover tape and the carrier tape is between 165 and 180 degrees and the test is done at a speed of 120 +/- 10 % mm/mn.

3. Reels

The sealed carrier tape with the Flip-Chip CSP is reeled on 7 inch reels (see figure 4 for reel mechanical dimensions). These reels are compliant with EIA 481-1. Each reel contains 5000 components. In compliance with IEC286-3, each reel will contain a maximum 10 empty cavities with no more than 2 successive empty cavities. Each reel may contain components coming from 2 different wafer lots. The reel is made from a white antistatic polystyrene material.

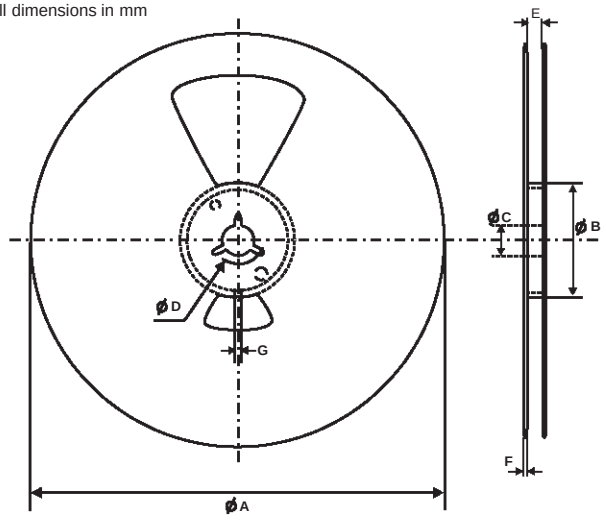
Each reel has a minimum leader of 600 mm and a minimum trailer of 160 mm (compliant with EIA 481-1 & IEC 286-3). The leader makes up a portion of carrier tape with empty cavities and sealed by cover tape at the beginning of the reel (customer side). The leader is affixed to the last turn of the carrier tape by using adhesive tape. The trailer is at the end of the reel and consists of empty, sealed cavities.

Fig. 4: 7” reel mechanical dimensions

Material: WHITE ANTISTATIC POLYSTYRENE

A	B	C	D	E	F	G	Color
ø178 max	ø 60 ± 1	ø13 ± 0.2	ø20.2 min	8.4 ± 1.5	1.6 ± 0.5	3 ± 0.5	White

All dimensions in mm



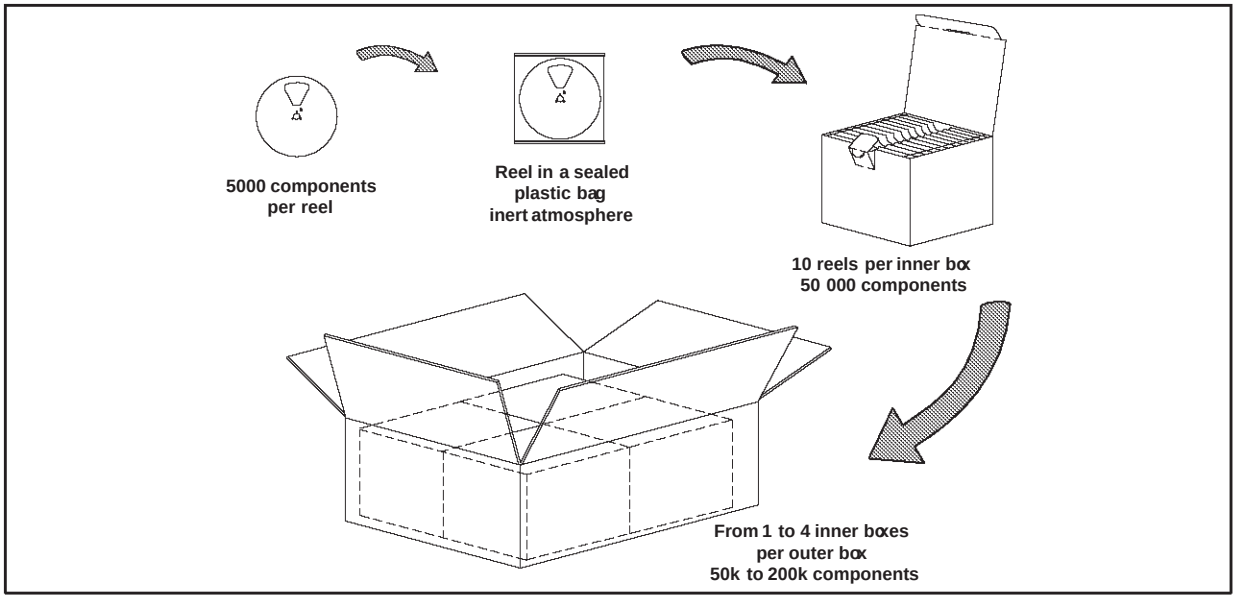
4. Final packing

Each reel is heat sealed under inert atmosphere in a transparent, recyclable and antistatic polyethylene bag (minimum of 4 mils material thickness).

Reels are packed in inner cardboard boxes. Each inner box contains exactly 10 reels i.e. 50 000 components. Inner boxes are delivered in outer cardboard boxes (from 1 to 4 inner boxes per outer box according to delivery quantities). Minimum production delivery quantity is 50 000 components.

The complete description for packing is shown on figure 5.

Fig. 5: Packing flow chart



5. Labelling

To ensure components' traceability labels are stuck on the reels, bags, and the inner and outer boxes. Seven inch reels and bags are identified by a label including component part number, quantity and lot number. Inner boxes are referenced with one inner label (in particular with the traceability number). Outer boxes are identified with an outer label showing the products' partnumber, total quantity and shipment information.

RECOMMENDED STORAGE AND SHIPPING INSTRUCTIONS AND DESCRIPTIONS

Flip-Chip CSP reels are packed under inert N2 atmosphere in a sealed bag. For shipment and handling, reels are protected by inner and outer cardboard boxes.

STMicroelectronics thus recommends the following shipping and storage conditions :

- relative humidity between 15% and 70%
- temperature range from -5°C to 35°C

Components in a non opened sealed bag can be stored 6 months after shipment. Once a bag is opened, the reels have to be used within 24 hours.

Components in tape&reel must be protected from exposure to direct sunlight.

SOLDERING ASSEMBLY RECOMMENDATIONS

1. PCB design recommendations

For optimum electrical performance and highly reliable solder joints, ST Microelectronics recommends the PCB design guidelines listed in table 1.

Table. 1: PCB design recommendations

PCB pad design	Non Solder Mask Defined Micro via under bump allowed
PCB pad size	∅ = 300µm max (circular)
Solder mask opening	∅ = 340µm min (for 300µm diameter pad)
PCB pad finishing	Cu - Ni (2-6µm) - Au (0.2µm max)

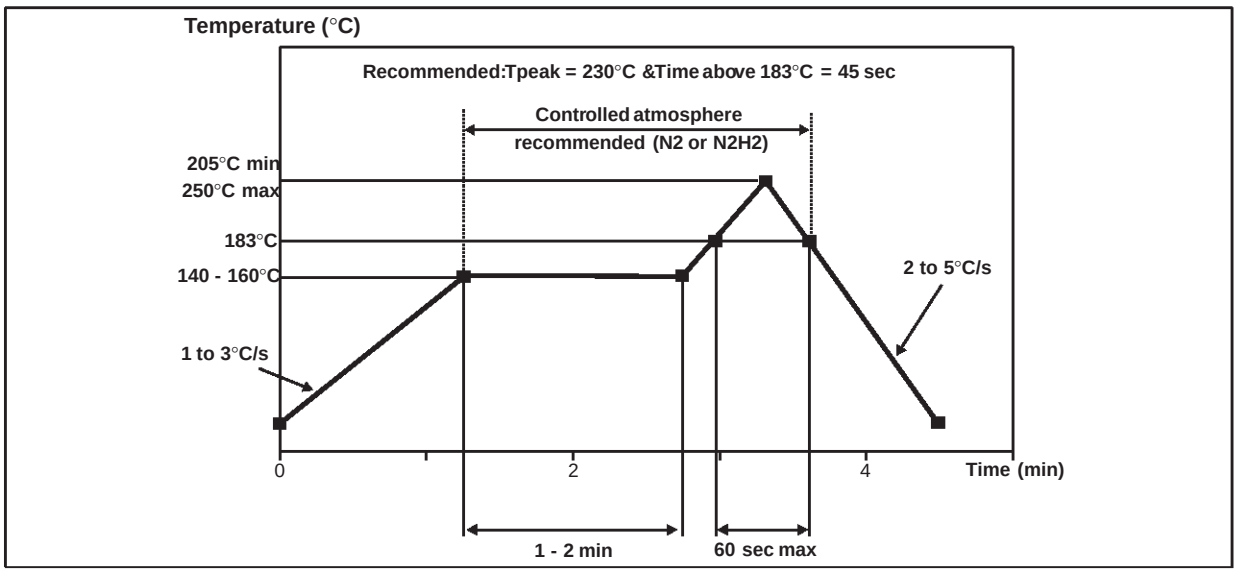
To optimize the natural self centering effect of Flip-Chip CSPs on PCB, PCB pad positionning and size have to be properly designed.

Note: a too thick gold layer finishing on the PCB pad is not recommended (low joint reliability).

2. PCB assembly guidelines

For Flip-Chip CSP mounting on the PCB, ST Microelectronics recommends the use of a solder stencil aperture with a maximum diameter of 320 µm maximum and a stencil thickness of 150µm. Flip-Chip CSPs are fully compatible with the use of eutectic Sn63Pb37 solder paste with no clean flux. ST's recommendations for Flip-Chip CSP board mounting are illustrated on the soldering reflow profile shown in figure 6 below.

Fig. 6: Recommended soldering reflow profile for Flip-Chip CSP mounting on PCB



Dwell time in the soldering zone (with temperature higher than 183°C) has to be kept as short as possible to prevent component and substrate damages. Peak temperature must not exceed 250°C. Controlled atmosphere (N2 or N2H2) is recommended during the whole reflow, specially above 150°C.

Flip-Chip CSPs are able to withstand twice the previous recommended reflow profile to be compatible a with double reflow when SMDs are mounted on both sides of the PCB.
A maximum of two soldering reflows are allowed for these packages.

The use of a no clean flux is highly recommended to avoid any cleaning operation. In order to prevent any bump cracks, ultrasonic cleaning methods are not recommended.

3. Underfilling

Underfilling is not needed for Flip-Chip CSPs but these devices can withstand the dispense of an underfill if the temperature process does not exceed 175°C and if the process time is short (typically 5 minutes).

4. Manual rework

Flip-Chip CSPs are able to tolerate one repair in addition to the two reflows mentionned in section VI.2.

As for other BGA type packages, the use of laser systems is the most suitable form for Flip-Chip CSP repair. Manual hot gas soldering is acceptable but iron soldering is not recommended.

For manual rework, the maximum temperature allowed is 250°C and dwell time must not exceed 30 seconds.
Component replacement is preferred for such packages than manual rework.

USER RESPONSABILITY AND RETURNS

STMicroelectronics guarantees the excellent quality of its Flip-Chip CSPs in respect of the instructions provided in this application note. For more information, the reader can consult the “Sure 7” Quality and Reliability brochure.

In the event that parts are found defective by the customer, the parts should be returned according to the **ST** standard procedure within 60 days after the date of reception.

CHANGES

STMicroelectronics reserves the right to implement minor changes of geometry and manufacturing processes without prior notice. Such changes will not affect electrical characteristics of the die, the pad layout or the maximum die size. However for confirmed orders, no variation will be made without customer’s approval.

DELIVERY QUANTITY

Flip-Chip CSPs should be ordered in multiples of 10 reels (or multiples of 50 000 components). For more information, please contact ST Customer Services.

QUALITY

1. Electrical inspection

Flip-Chip CSPs are 100% electrically probed according to the critical parameters of the ST product specification. The last operation before packing is 100% electrical testing. The other parameters are guaranteed by technology, design rules and by continuous monitoring systems.

2. Visual inspection

A visual control according to the internal ST standard specification is performed on all manufacturing lots.

CONCLUSION

Flip-chip CSPs have been developped by STMicroelectronics for electronic applications where integration and performance are the main concerns of designers.

STMicroelectronics Flip-Chip CSPs offer :

- **remarkable board space saving** (package size equal to die size and total height less than 0.700mm)
- **enhanced electrical performance** (minimized parasitic inductance due to very short electrical paths and absence of redistribution layer)
- **high reliability** due to integration of a whole function traditionally based on discrete interconnected components.

Flip-chip CSPs are delivered in tape and reel and are fully compatible with other high volume SMD components (standard plastic packages or CSP/BGA packages) regarding existing pick and place equipment, standard solder reflow assembly equipment and standard PCB techniques.