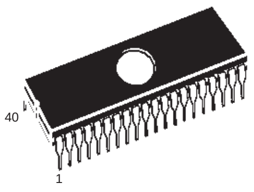
M27V400

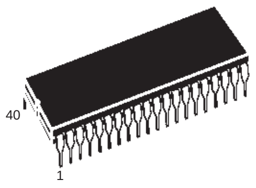
4 Mbit (512Kb x8 or 256Kb x16) UV EPROM and OTP EPROM

NOT FOR NEW DESIGN

- **M27V400 is replaced by the M27W400**
- 3V to 3.6V LOW VOLTAGE in READ OPERATION
- ACCESS TIME: 100ns
- BYTE-WIDE or WORD-WIDE CONFIGURABLE
- 4 Mbit MASK ROM REPLACEMENT
- LOW POWER CONSUMPTION
  - Active Current 30mA at 8MHz
  - Stand-by Current 20µA
- PROGRAMMING VOLTAGE: 12.5V ± 0.25V
- PROGRAMMING TIME: 50µs/word
- ELECTRONIC SIGNATURE
  - Manufacturer Code: 20h
  - Device Code: B8h



FDIP40W (F)



PDIP40 (B)

DESCRIPTION

The M27V400 is an 4 Mbit EPROM offered in the two ranges UV (ultra violet erase) and OTP (one time programmable). It is ideally suited for microprocessor systems requiring large data or program storage. It is organised as either 512 Kwords of 8 bit or 256 Kwords of 16 bit. The pin-out is compatible with the most common 4 Mbit Mask ROM.

The FDIP40W (window ceramic frit-seal package) has a transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern.

A new pattern can then be written rapidly to the device by following the programming procedure.

For applications where the content is programmed only one time and erasure is not required, the M27V400 is offered in PDIP40 package.

Figure 1. Logic Diagram

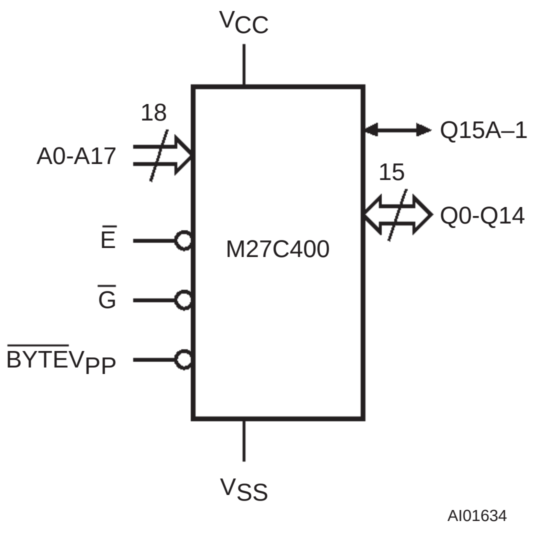


Figure 2. DIP Connections

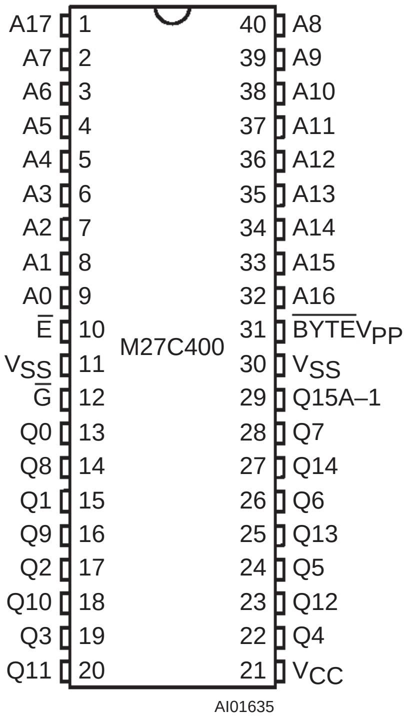


Table 1. Signal Names

A0-A17	Address Inputs
Q0-Q7	Data Outputs
Q8-Q14	Data Outputs
Q15A–1	Data Output / Address Input
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{\text{BYTE}}V_{PP}$	Byte Mode / Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

DEVICE OPERATION

The operating modes of the M27V400 are listed in the Operating Modes Table. A single power supply is required in the read mode. All inputs are TTL compatible except for V_{PP} and 12V on A9 for the Electronic Signature.

Read Mode

The M27V400 has two organisations, Word-wide and Byte-wide. The organisation is selected by the signal level on the $\overline{\text{BYTE}}V_{PP}$ pin. When $\overline{\text{BYTE}}V_{PP}$ is at V_{IH} the Word-wide organisation is selected and the Q15A–1 pin is used for Q15 Data Output. When the $\overline{\text{BYTE}}V_{PP}$ pin is at V_{IL} the Byte-wide organisation is selected and the Q15A–1 pin is used for the Address Input A–1. When the memory is logically regarded as 16 bit wide, but read in the Byte-wide organisation, then with A–1 at V_{IL} the lower 8 bits of the 16 bit data are selected and with A–1 at V_{IH} the upper 8 bits of the 16 bit data are selected.

The M27V400 has two control functions, both of which must be logically active in order to obtain data at the outputs. In addition the Word-wide or Byte- wide organisation must be selected. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27V400 has a standby mode which reduces the supply current from 30mA to 20µA. The M27V400 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature (3)	–40 to 125	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltage (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} (2)	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

Note:
1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.
2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.
3. Depends on range.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	$\overline{BYTE}V_{PP}$	A9	Q7-Q0	Q14-Q8	Q15A–1
Read Word-wide	V_{IL}	V_{IL}	V_{IH}	X	Data Out	Data Out	Data Out
Read Byte-wide Upper	V_{IL}	V_{IL}	V_{IL}	X	Data Out	Hi-Z	V_{IH}
Read Byte-wide Lower	V_{IL}	V_{IL}	V_{IL}	X	Data Out	Hi-Z	V_{IL}
Output Disable	V_{IL}	V_{IH}	X	X	Hi-Z	Hi-Z	Hi-Z
Program	V_{IL} Pulse	V_{IH}	V_{PP}	X	Data In	Data In	Data In
Verify	V_{IH}	V_{IL}	V_{PP}	X	Data Out	Data Out	Data Out
Program Inhibit	V_{IH}	V_{IH}	V_{PP}	X	Hi-Z	Hi-Z	Hi-Z
Standby	V_{IH}	X	X	X	Hi-Z	Hi-Z	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	Codes	Codes	Code

Note: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V.

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	1	0	1	1	0	0	1	0	B8h

Note: Outputs Q15-Q8 are set to '0'.

Table 5. AC Measurement Conditions

	High Speed	Standard
Input Rise and Fall Times	≤ 10ns	≤ 20ns
Input Pulse Voltages	0 to 3V	0.4V to 2.4V
Input and Output Timing Ref. Voltages	1.5V	0.8V and 2V

Figure 3. Testing Input Output Waveform

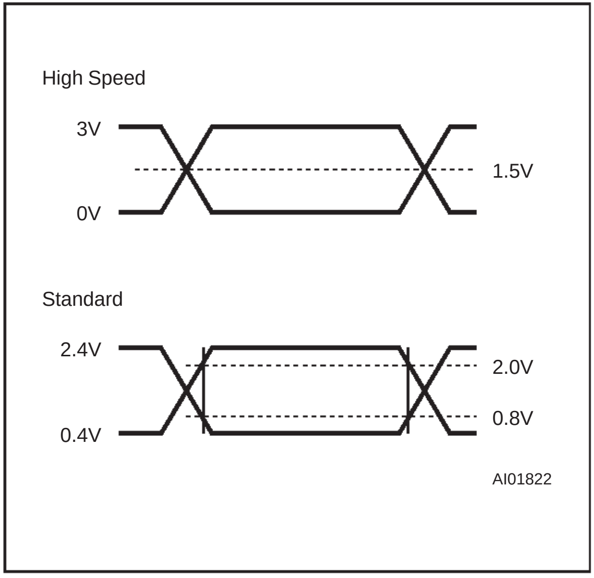


Figure 4. AC Testing Load Circuit

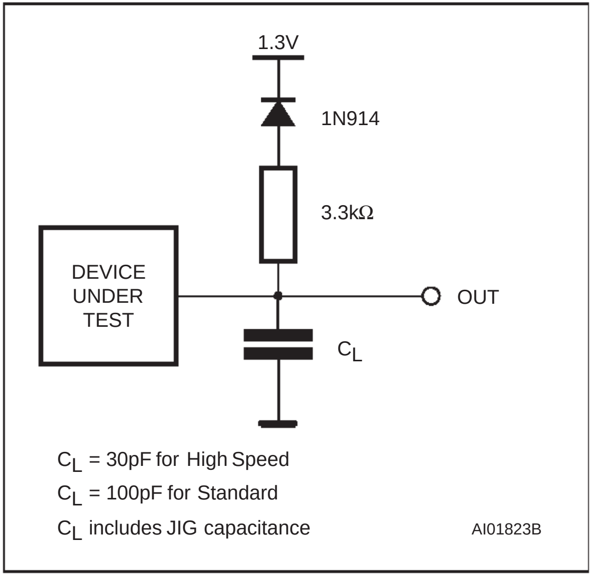


Table 6. Capacitance [(1)] (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (except $\overline{\text{BYTE}}V_{PP}$)	V_{IN} = 0V		10	pF
	Input Capacitance ($\overline{\text{BYTE}}V_{PP}$)	V_{IN} = 0V		120	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, this product features a 2-line control function which accommodates the use of multiple memory connection. The two-line control function allows:

a. the lowest possible memory power dissipation

b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{\text{READ}}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

Table 7. Read Mode DC Characteristics [(1)]
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 3.3V ± 5% or 3.3V ± 10%; $V_{PP} = V_{CC}$)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, I_{OUT} = 0mA, f = 8MHz		30	mA
		$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, I_{OUT} = 0mA, f = 5MHz		20	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E} > V_{CC} - 0.2V$		20	µA
I_{PP}	Program Current	$V_{PP} = V_{CC}$		10	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH} [(2)]	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Maximum DC voltage on Output is V_{CC} +0.5V.

System Considerations

The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the supplies to the devices. The supply current I_{CC} has three segments of importance to the system designer: the standby current, the active current and the transient peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device outputs. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1µF ceramic capacitor is used on every device between V_{CC} and V_{SS}. This should be a high frequency type of low inherent inductance and should be placed as close as possible to the device. In addition, a 4.7µF electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. This capacitor should be mounted near the power supply connection point. The purpose of this capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

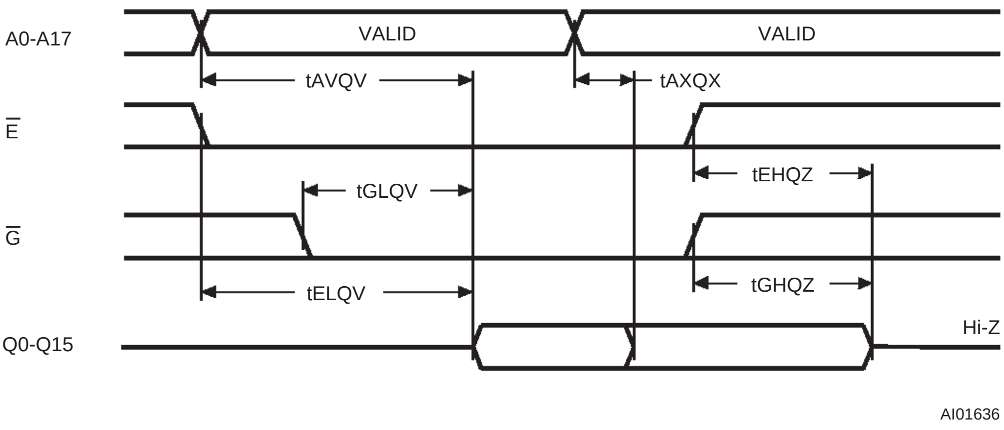
When delivered (and after each erasure for UV EPROM), all bits of the M27V400 are in the ’1’ state. Data is introduced by selectively programming ’0’s into the desired bit locations. Although only ’0’s will be programmed, both ’1’s and ’0’s can be present in the data word. The only way to change a ’0’ to a ’1’ is by die exposition to ultraviolet light (UV EPROM). The M27V400 is in the programming mode when V_{PP} input is at 12.5V, $\overline{G}$ is at V_{IH} and $\overline{E}$ is pulsed to V_{IL}. The data to be programmed is applied to 16 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25V.

Table 8. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 3.3V ± 5% or 3.3V ± 10%; $V_{PP} = V_{CC}$)

Symbol	Alt	Parameter	Test Condition	M27V400		Unit
				-100		
				Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		100	ns
t_{BHQV}	t_{ST}	BYTE High to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		100	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		100	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		50	ns
t_{BLQZ} (2)	t_{STD}	BYTE Low to Output Hi-Z	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		45	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	45	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	45	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	5		ns
t_{BLQX}	t_{OH}	BYTE Low to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	5		ns

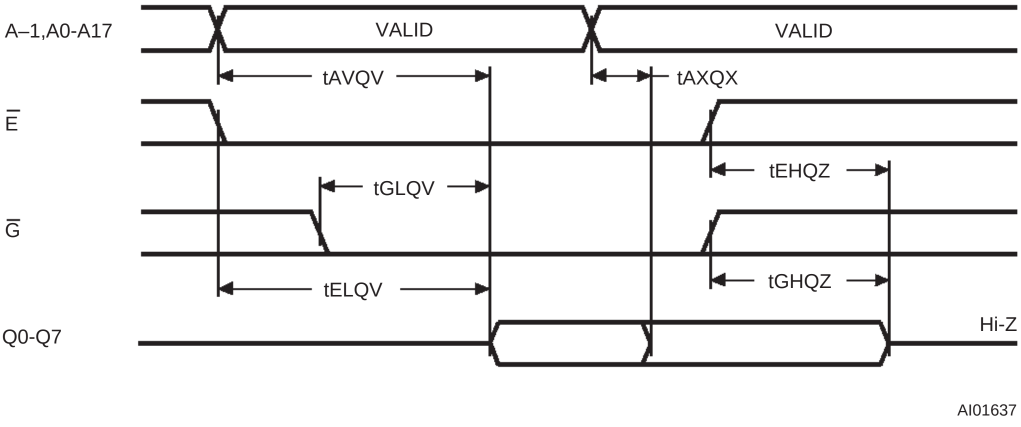
Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}
2. Sampled only, not 100% tested.

Figure 5. Word-Wide Read Mode AC Waveforms



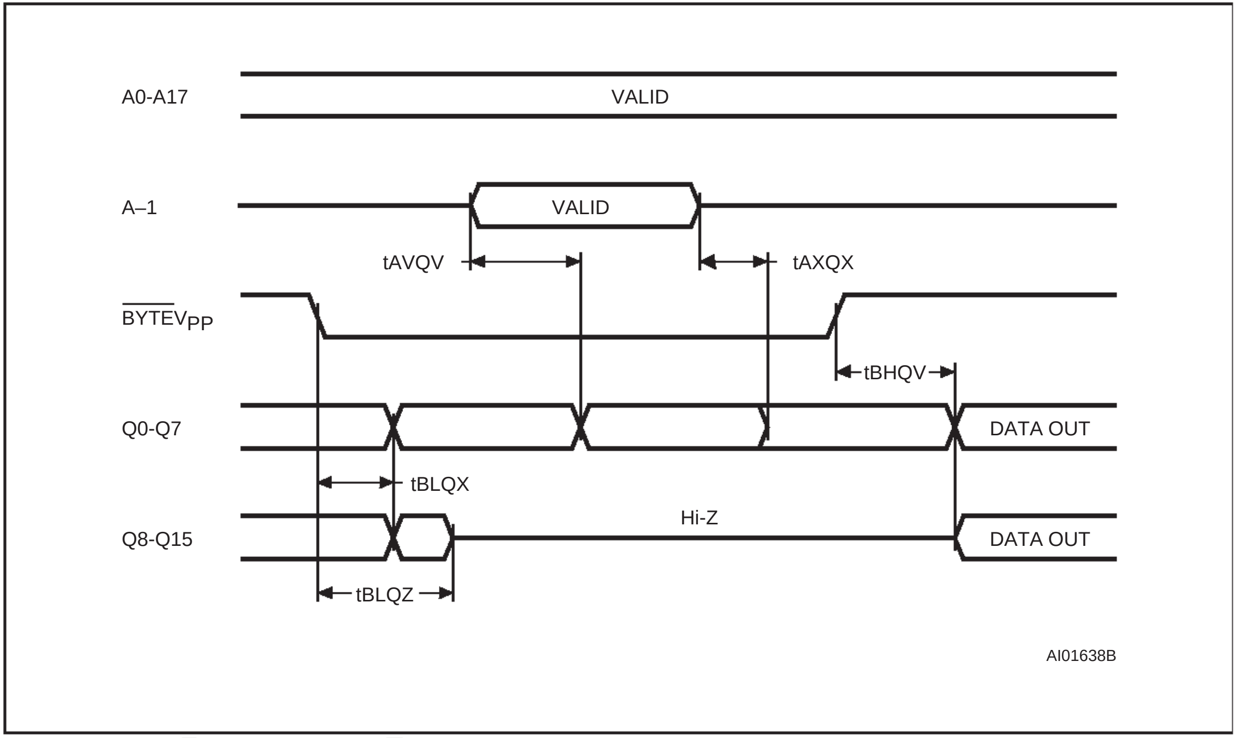
Note: $\overline{\text{BYTE}}\text{V}_{PP} = \text{V}_{IH}$.

Figure 6. Byte-Wide Read Mode AC Waveforms



Note: $\overline{\text{BYTE}}\text{V}_{PP} = \text{V}_{IL}$.

Figure 7. $\overline{\text{BYTE}}$ Transition AC Waveforms



Note: Chip Enable ($\overline{E}$) and Output Enable ($\overline{G}$) = V_{IL}.

Table 9. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.5V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0 \leq V_{IN} \leq V_{CC}$		±1	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.4	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –2.5mA	3.5		V
V_{ID}	A9 Voltage		11.5	12.5	V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 10. Programming Mode AC Characteristics [1]

(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.5V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low		2		µs
t_{QVEL}	t_{DS}	Input Valid to Chip Enable Low		2		µs
t_{VPHAV}	t_{VPS}	V_{PP} High to Address Valid		2		µs
t_{VCHAV}	t_{VCS}	V_{CC} High to Address Valid		2		µs
t_{ELEH}	t_{PW}	Chip Enable Program Pulse Width		45	55	µs
t_{EHQX}	t_{DH}	Chip Enable High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			120	ns
t_{GHQZ} [2]	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Figure 8. Programming and Verify Modes AC Waveforms

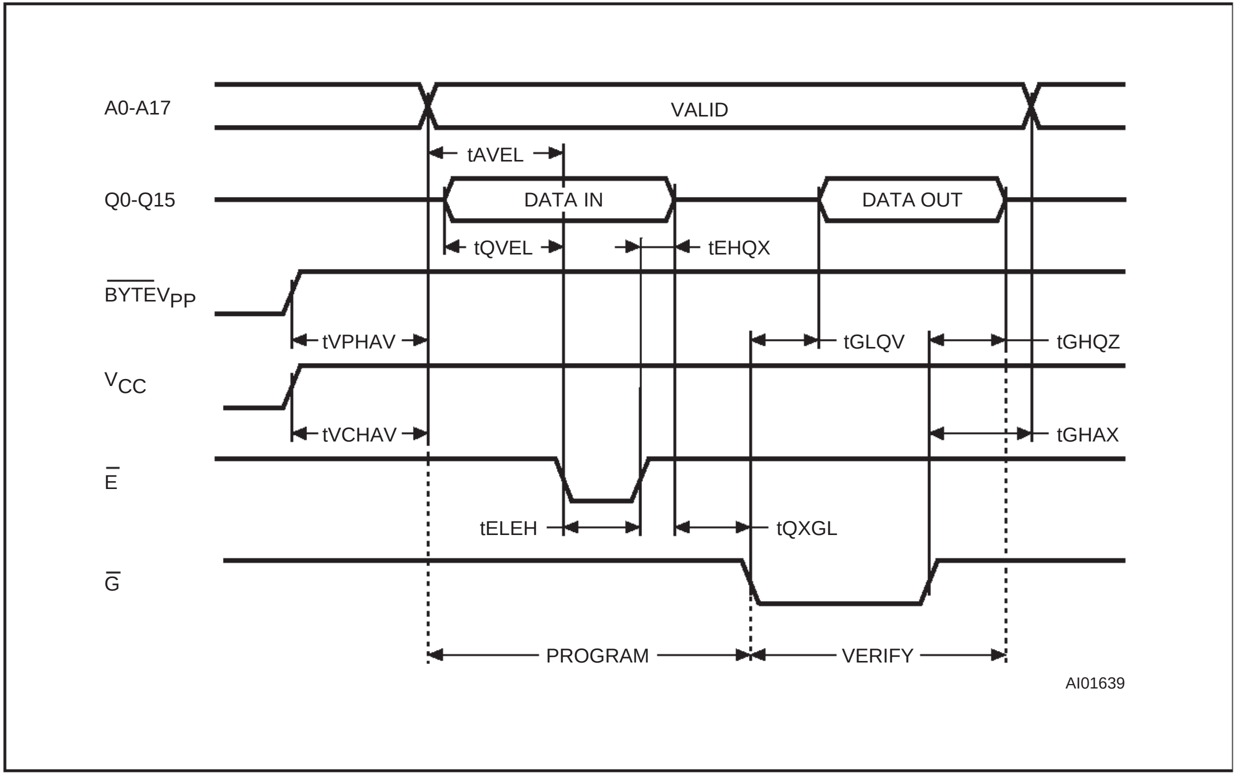
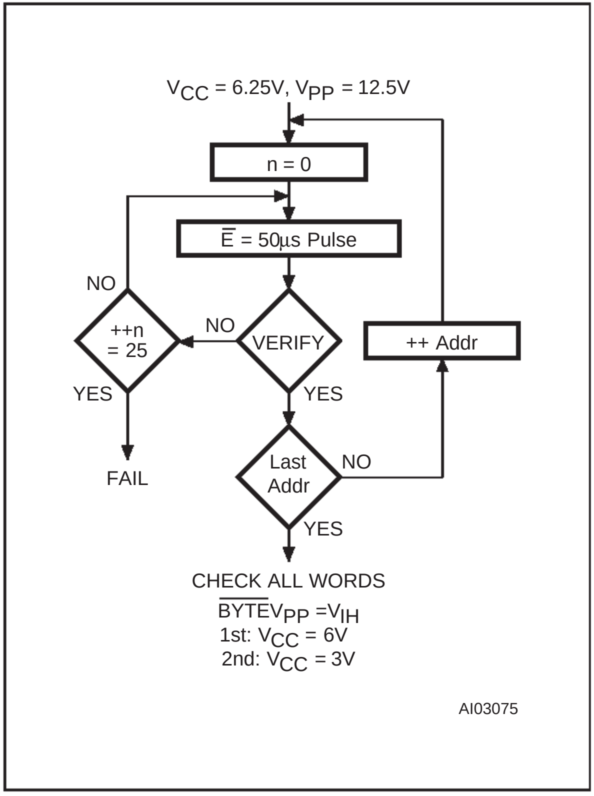


Figure 9. Programming Flowchart



PRESTO III Programming Algorithm

The PRESTO III Programming Algorithm allows the whole array to be programed with a guaranteed margin in a typical time of 13 seconds. Programming with PRESTO III consists of applying a sequence of 50µs program pulses to each word until a correct verify occurs (see Figure 9). During programing and verify operation a MARGIN MODE circuit is automatically activated to guarantee that each cell is programed with enough margin. No overpromise pulse is applied since the verify in MARGIN MODE provides the necessary margin to each programmed cell.

Program Inhibit

Programming of multiple M27V400s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}$ of the parallel M27V400 may be common. A TTL low level pulse applied to a M27V400's $\overline{E}$ input and V_{PP} at 12.5V, will program that M27V400. A high level $\overline{E}$ input inhibits the other M27V400s from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{E}$ at V_{IH} and $\overline{G}$ at V_{IL}, V_{PP} at 12.5V and V_{CC} at 6.25V.

Electronic Signature

The Electronic Signature (ES) mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. The ES mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27V400. To activate the ES mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27V400, with $V_{PP} = V_{CC} = 5V$. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode.

Byte 0 ($A0 = V_{IL}$) represents the manufacturer code and byte 1 ($A0 = V_{IH}$) the device identifier code. For the STMicroelectronics M27V400, these two identifier bytes are given in Table 4 and can be read-out on outputs Q7 to Q0.

ERASURE OPERATION (applies to UV EPROM)

The erasure characteristics of the M27V400 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27V400 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27V400 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27V400 window to prevent unintentional erasure. The recommended erasure procedure for M27V400 is exposure to short wave ultraviolet light which has a wavelength of 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 30 W-sec/cm^2. The erasure time with this dosage is approximately 30 to 40 minutes using an ultraviolet lamp with 12000 µW/cm^2 power rating. The M27V400 should be placed within 2.5cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

Table 11. Ordering Information Scheme

Example: M27V400 -100 X F 1 TR

Device Type

M27

Supply Voltage

V = 3V to 3.6V

Device Function

400 = 4 Mbit (512Kb x8 or 256Kb x16)

Speed

-100 = 100 ns

V_{CC} Tolerance

blank = ± 10%
X = ± 5%

Package

F = FDIP40W
B = PDIP40

Temperature Range

1 = 0 to 70 °C
6 = –40 to 85 °C

Options

TR = Tape & Reel Packing

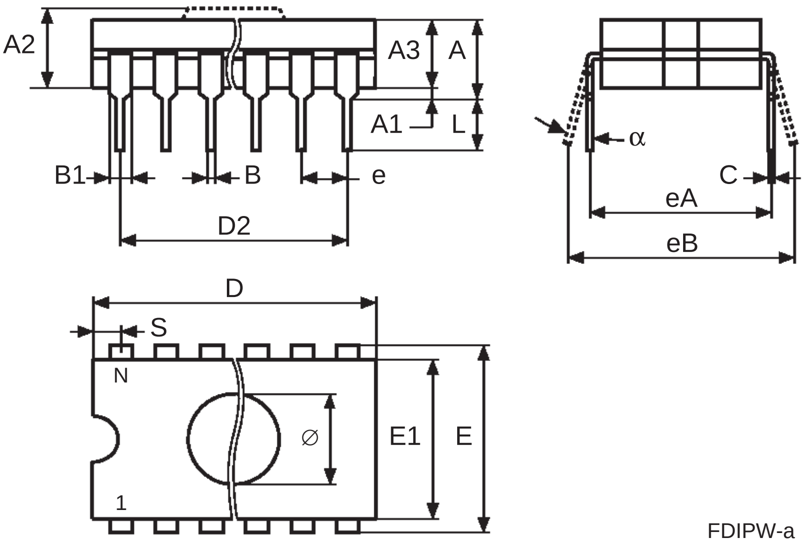
M27V400 is replaced by the M27W400

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

Table 12. FDIP40W - 40 lead Ceramic Frit-seal DIP with window, Package Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			5.72			0.225
A1		0.51	1.40		0.020	0.055
A2		3.91	4.57		0.154	0.180
A3		3.89	4.50		0.153	0.177
B		0.41	0.56		0.016	0.022
B1	1.45	–	–	0.057	–	–
C		0.23	0.30		0.009	0.012
D		51.79	52.60		2.039	2.071
D2	48.26	–	–	1.900	–	–
E	15.24	–	–	0.600	–	–
E1		13.06	13.36		0.514	0.526
e	2.54	–	–	0.100	–	–
ea.	14.99	–	–	0.590	–	–
be		16.18	18.03		0.637	0.710
L		3.18	–		0.125	–
S		1.52	2.49		0.060	0.098
∅	8.13	–	–	0.320	–	–
α		4°	11°		4°	11°
N	40			40		

Figure 10. FDIP40W - 40 lead Ceramic Frit-seal DIP with window, Package Outline

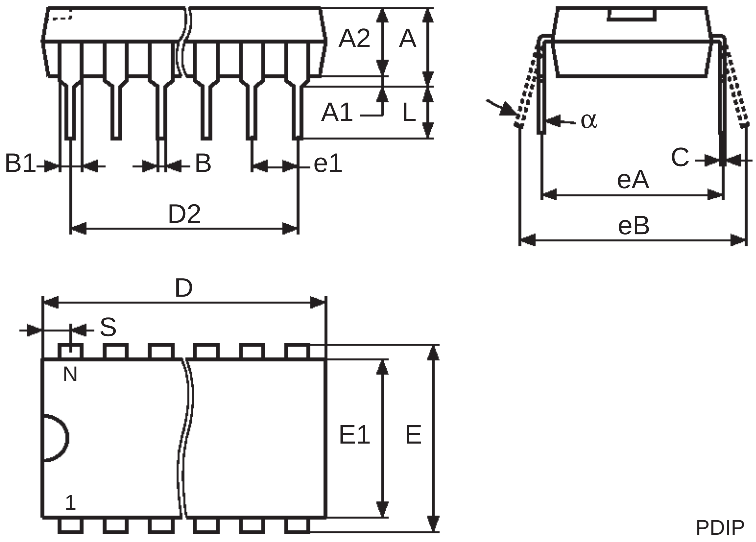


Drawing is not to scale.

Table 13. PDIP40 - 40 pin Plastic DIP, 600 mils width, Package Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A	4.45	–	–	0.175	–	–
A1	0.64	0.38	–	0.025	0.015	–
A2		3.56	3.91		0.140	0.154
B		0.38	0.53		0.015	0.021
B1		1.14	1.78		0.045	0.070
C		0.20	0.31		0.008	0.012
D		51.78	52.58		2.039	2.070
D2	48.26	–	–	1.900	–	–
E		14.80	16.26		0.583	0.640
E1		13.46	13.99		0.530	0.551
e1	2.54	–	–	0.100	–	–
ea.	15.24	–	–	0.600	–	
be		15.24	17.78		0.600	0.700
L		3.05	3.81		0.120	0.150
S		1.52	2.29		0.060	0.090
α		0°	15°		0°	15°
N	40			40		

Figure 11. PDIP40 - 40 lead Plastic DIP, 600 mils width, Package Outline



Drawing is not to scale.

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