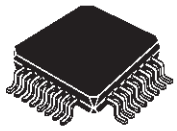
STLVD111

PROGRAMMABLE LOW VOLTAGE 1:10 DIFFERENTIAL LVDS CLOCK DRIVER

- 100ps PART-TO PART SKEW
- 40ps BANK SKEW
- DIFFERENTIAL DESIGN
- MEETS LVDS SPEC. FOR DRIVER OUTPUTS AND RECEIVER INPUTS
- REFERENCE VOLTAGE AVAILABLE OUTPUT V_{BB}
- LOW VOLTAGE V_{CC} RANGE OF 2.375 TO 2.625V
- HIGH SIGNALLING RATE CAPABILITY (EXCEEDS 622MHz)
- SUPPORT OPEN, SHORT AND TERMINATED INPUT FAIL-SAFE (LOW OUPUT STATE)
- PROGRAMMABLE DRIVERS POWER OFF CONTROL



TQFP32

DESCRIPTION

The STLVD111 is a low skew programmable 1 to 10 differential LVDS driver, designed for clock distribution. The select signal is fanned out to 10 identical differential outputs.

The STLVD111 is provided with a 11 bit shift register with a serial in and a Control Register. The purpose is to enable or power off each output clock channel and to select the clock input.

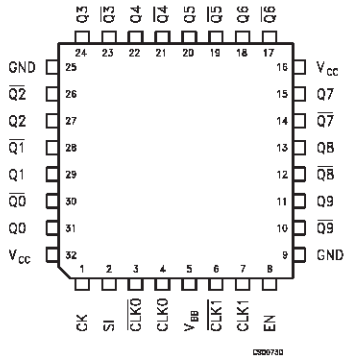
The STLVD111 is specifically designed, modelled and produced with low skew as the key goal. Optimal design and layout serve to minimize gate to gate skew within a device. The net result is a dependable guaranteed low skew device.

The STLVD111 can be used for high performance clock distribution in 2.5V systems with LVDS levels. Designers can take advantage of the device's performance to distribute low skew clocks across the backplane or the board.

ORDER CODES

Type	Temperature Range	Package	Comments
STLVD111BF	-40 to 85 °C	TQFP32 (Tray)	250 parts per Tray
STLVD111BFR	-40 to 85 °C	TQFP32 (Tape & Reel)	2400 parts per Reel

PIN CONFIGURATION



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	CK	Control Register Clock
2	SI	Control Register Serial In/CLK_SEL
3	$\overline{CLK0}$	Differential Input
4	CLK0	Differential Input
5	V_{BB}	Output Reference Voltage
6	$\overline{CLK1}$	Differential Input
7	CLK1	Differential Input
8	EN	Device Enable/Program
9	GND	Ground
10	$\overline{Q9}$	Differential Outputs
11	Q9	Differential Outputs
12	$\overline{Q8}$	Differential Outputs
13	Q8	Differential Outputs
14	$\overline{Q7}$	Differential Outputs
15	Q7	Differential Outputs
16	V_{CC}	Supply Voltage
17	$\overline{Q6}$	Differential Outputs
18	Q6	Differential Outputs
19	$\overline{Q5}$	Differential Outputs
20	Q5	Differential Outputs
21	$\overline{Q4}$	Differential Outputs
22	Q4	Differential Outputs
23	$\overline{Q3}$	Differential Outputs
24	Q3	Differential Outputs
25	GND	Ground
26	$\overline{Q2}$	Differential Outputs
27	Q2	Differential Outputs
28	$\overline{Q1}$	Differential Outputs
29	Q1	Differential Outputs
30	$\overline{Q0}$	Differential Outputs
31	Q0	Differential Outputs
32	V_{CC}	Supply Voltage

ABSOLUTE MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.3 to 2.8	V
V_I	Input Voltage	-0.2 to (V_{CC}+0.2)	V
V_O	Output Voltage	-0.2 to (V_{CC}+0.2)	V
I_{OSD}	Driver Short Circuit Current	Continuos	
ESD	Electrostatic Discharge (HBM 1.5KΩ, 100pF)	>2	KV

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

THERMAL DATA

R_{Tj-c}	Thermal Resistance Junction-Case	13	$^oC/W$

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	TYP	Max	Unit
V_{CC}	Supply Voltage	2.375		2.625	V
V_{IC}	Receiver Common Mode Input Voltage	$0.5\|V_{ID}\|$		$2-0.5\|V_{ID}\|$	V
T_A	Operating Free-Air Temperature	-40		85	^oC
T_J	Operating Junction Temperature	-40		105	^oC

DRIVER ELECTRICAL CHARACTERISTICS (T_A = -40 to 85 ^oC, V_{CC} = 2.5V ± 5% unless otherwise specified (Note1, 2)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{OD}	Output Differential Voltage (Fig. 2)	R_L= 100 Ω	250	450	600	mV
ΔV_{OD}	V_{OD} Magnitude Change				70	mV
V_{OS}	Offset Voltage	$-40 \le T_A \le 85\ ^oC$ $0 \le T_A \le 70\ ^oC$	0.95 0.95	1.2 1.2	1.45 1.35	V V
ΔV_{OS}	V_{OS} Magnitude Change				350	mV
I_{OS}	Output Short Circuit Current	V_O = 0V V_{OD} = 0V		15 7	30 15	mA mA

Note 1: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.
Note 2: All typical values are given for V_{CC} = 2.5V and T_A = 25^oC unless otherwise stated.

RECEIVER ELECTRICAL CHARACTERISTICS (T_A = -40 to 85 ^oC, V_{CC} = 2.5V ± 5% unless otherwise specified (Note1, 2)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IDH}	Input Threshold High				100	mV
V_{IDL}	Input Threshold Low		-100			mV
I_{IN}	Input Current	V_I = 0V V_I = V_{CC}		42 2	100 10	µA µA

Note 1: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.
Note 2: All typical values are given for V_{CC} = 2.5V and T_A = 25^oC unless otherwise stated.

DRIVER ELECTRICAL CHARACTERISTICS (T_A = -40 to 85 °C, V_{CC} = 2.5V ± 5% unless otherwise specified (Note1, 2)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{BB}	Output Reference Voltage	V_{CC} = 2.5V	1.15	1.25	1.35	V
I_{CCD}	Power Supply Current	All driver enabled and loaded		105	130	mA
C_{IN}	Input Capacitance	V_I = 0V to V_{CC}		5		pF
C_{OUT}	Output Capacitance			5		pF
V_{IH}	Logic Input High Threshold	V_{CC} = 2.5V	2			V
V_{IL}	Logic Input Low Threshold	V_{CC} = 2.5V			0.8	V
I_I	Logic Input Current	V_O = 2.5V, V_{IN} = V_{CC} or GND			± 10	µA

Note 1: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.
Note 2: All typical values are given for V_{CC} = 2.5V and T_A = 25°C unless otherwise stated.

LVDS TIMING CHARACTERISTICS (T_A = -40 to 85 °C, V_{CC} = 2.5V ± 5% unless otherwise specified (Note 4)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
t_{TLH}, t_{THL}	Transition time	R_L = 100Ω, C_L = 5 pF, (Fig. 5, 6)		330	450	ps
t_{PLH}, t_{PHL}	Propagation Delay Time	(Fig. 5, 6)		2	3	ns
f_{MAX}	Maximum Input Frequency		700	900		MHz
t_{SKEW}	Bank Skew	(Fig. 1)		40		ps
	Part to part Skew	(Fig. 2)		100		ps
	Pulse Skew	(Fig. 3)		50		ps

Note 4: Generator waveforms for all test conditions: f = 1MHz, Z_O = 50 Ω (unless otherwise specified)

CONTROL REGISTER TIMING CHARACTERISTICS (T_A = -40 to 85 °C, V_{CC} = 2.5V ± 5%, EN=H, unless otherwise specified (Figure 4)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
f_{MAX}	Maximum Frequency of Shift Register	(Fig. 7)	100	150		MHz
t_s	Clock to SI Setup Time	(Fig. 7)			2	ns
t_h	Clock to SI Hold Time	(Fig. 7)			1.5	ns
t_{rem}	Enable to Clock Removal Time	(Fig. 7)			1.5	ns
t_W	Minimum Clock Pulse Width	(Fig. 7)	3			ns

SPECIFICATION OF CONTROL REGISTER

The STLVD111 is provided with a 11 bit shift register with a Serial In and a Control Register. The purpose is to enable or power off each output clock channle and to select the clock input. The STLVD111 provides two working modality:

PROGRAMMED MODE (EN=1)

The shift register have a serial input to load the working configuration. Once the configuration is loaded with 11 clock pulse, another clock pulse load the configuration into the control register. The first bit on the serial input line enables the outputs Q9 and $\overline{Q9}$, the second bit enables the outputs Q8 and $\overline{Q8}$ and so on. The last bit is the clock selection bit. To restart the configuration of the shift register a reset of the state machine must be done with a clock pulse on CK and the EN set to Low. The control register can be configured on time after each reset.

STANDARD MODE (EN=0)

In Standard Mode the STLVD111 isn't programmable, all the clock outputs are enabled. The LVDS clock input is selected from Clock0 or Clock1 with the SI pin as shown in the Truth Table below.

TRUTH TABLE OF STATE MACHINE INPUTS

EN	SI	CK	OUTPUT
L	L	X	All Output Enabled, Clock0 selected, Control Register disabled
L	H	X	All Output Enabled, Clock1 selected, Control Register disabled
H	L	⌐	First stage stores "L", other stages store the data of previous stage
H	H	⌐	First stage stores "H", other stages store the data of previous stage
L	X	⌐	Reset of the state machine, Shift register and Control Register

SERIAL INPUT SEQUENCE

BIT#10	BIT#9	BIT#8	BIT#7	BIT#6	BIT#5	BIT#4	BIT#3	BIT#2	BIT#1	BIT#0
CLK_SEL	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9

TRUTH TABLE OF THE CONTROL REGISTER

BIT#10	BIT#(0-9)	Qn(0-9)
L	H	Clock0
H	H	Clock1
X	L	Qn Output Disabled

X= Don't Care

TRUTH TABLE

CK	EN	SI	CLK0	$\overline{CLK0}$	CLK1	$\overline{CLK1}$	Q(0-9)	$\overline{Q}$(0-9)
L	L	L	L	H	X	X	L	H
L	L	L	H	L	X	X	H	L
L	L	L	Open	Open	X	X	L	H
L	L	H	X	X	L	H	L	H
L	L	H	X	X	H	L	H	L
L	L	H	X	X	Open	Open	L	H
All drivers enable								

LOGIC DIAGRAM

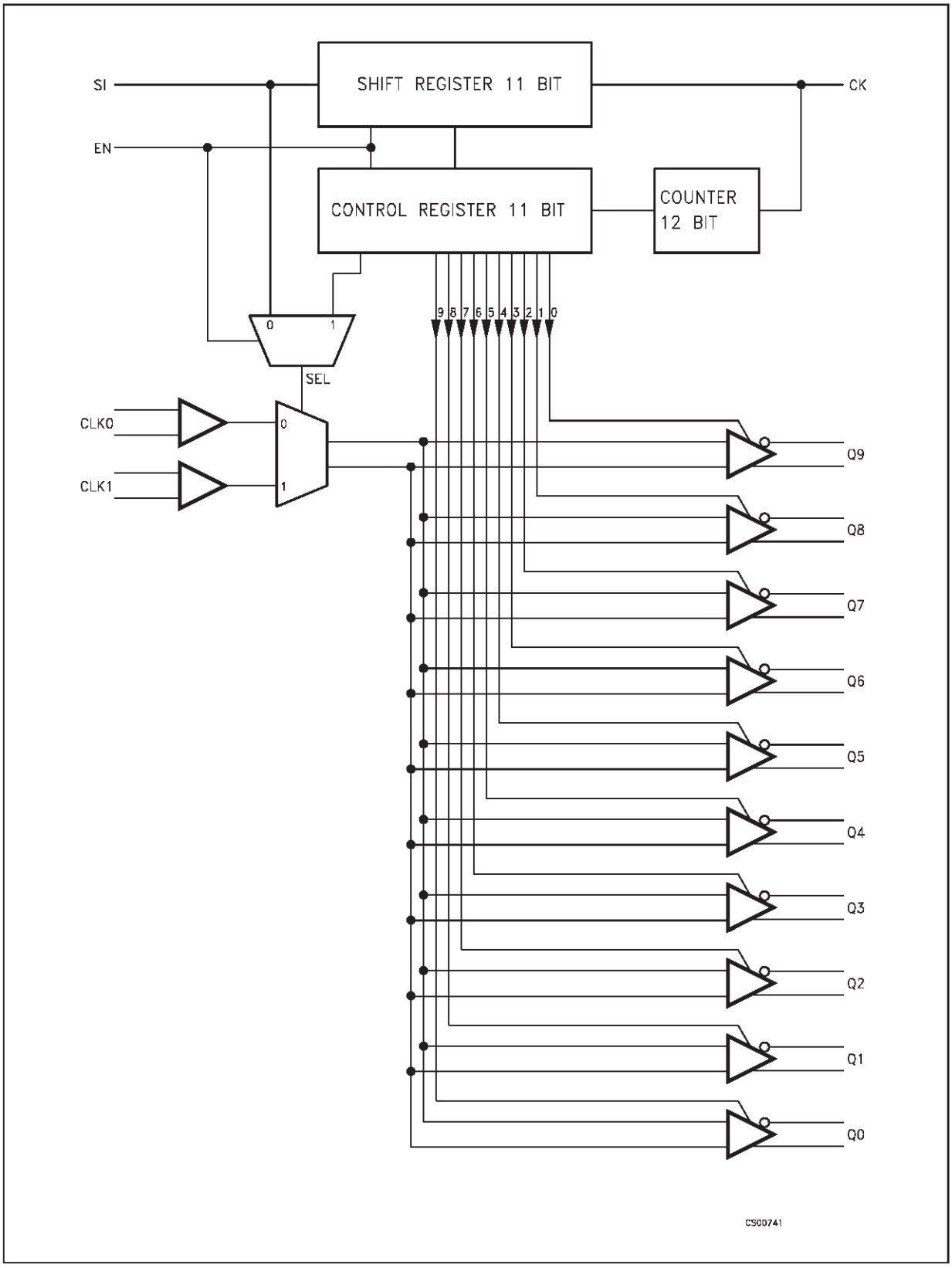


Figure 1: BANK SKEW - $t_{sk(b)}$

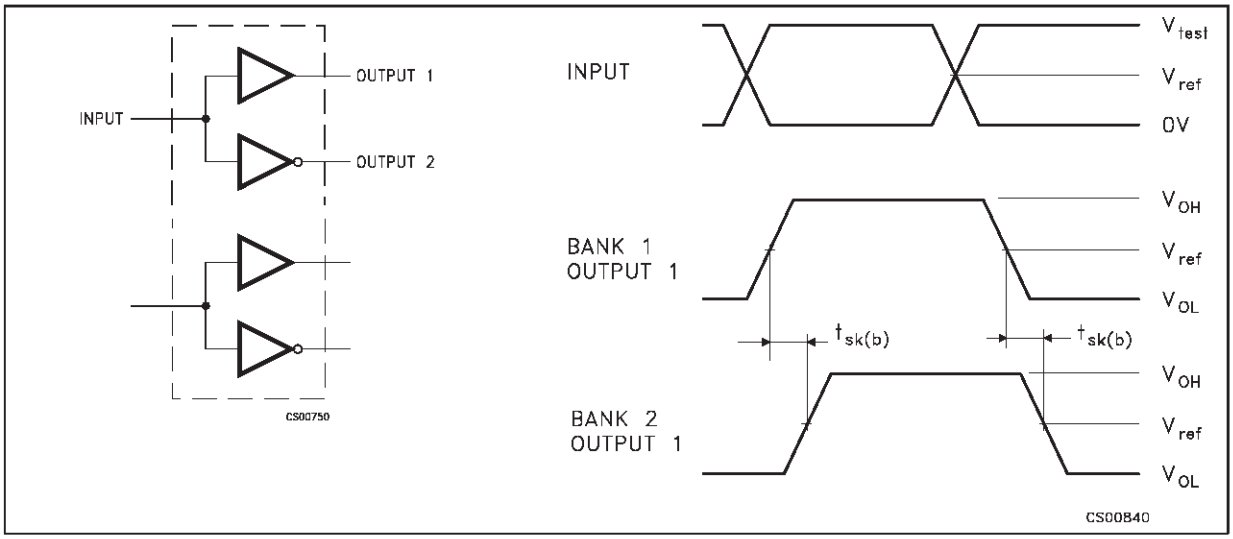


Figure 2: PART TO PART SKEW - $t_{sk(PP)}$

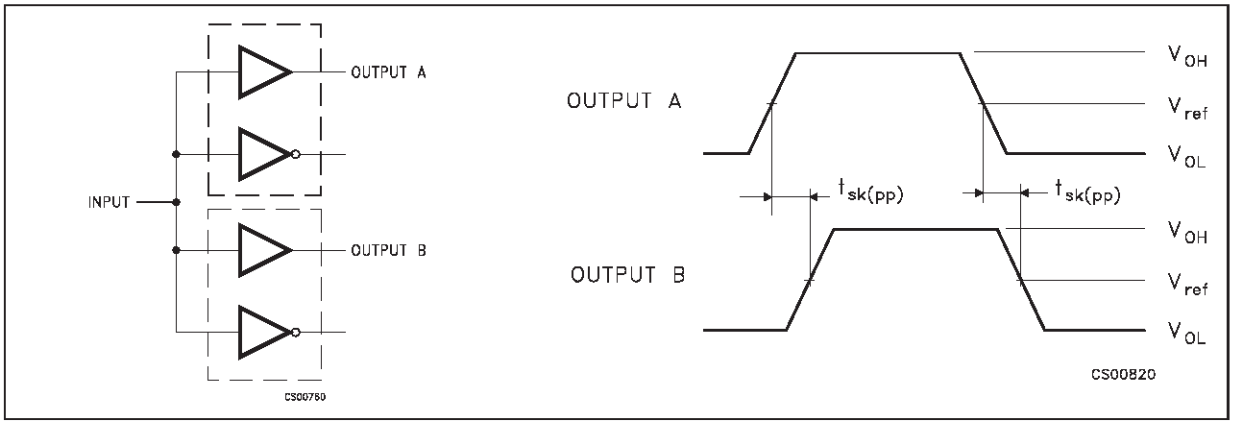
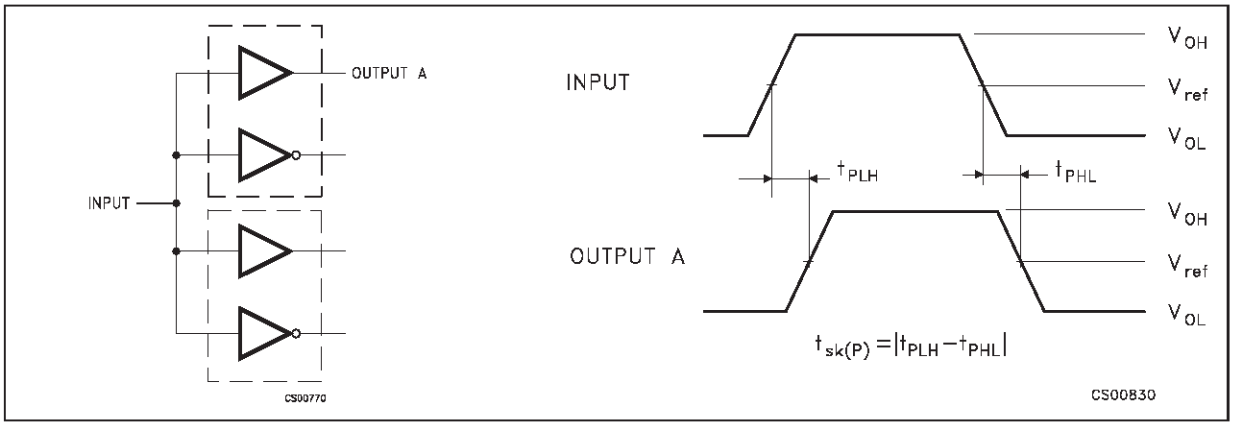


Figure 3: PULSE SKEW - $t_{sk(P)}$



$t_{sk(b)}$: BANK SKEW is the magnitude of the time difference between outputs with a single driving input terminal
$t_{sk(pp)}$: PART TO PART SKEW is the magnitude of the difference in propagation delay times between any specific terminals of two devices when both devices operate with the same input signal, the same supply voltages, at the same temperature, and have identical packages and test circuits.
$t_{sk(b)}$: PULSE SKEW is the magnitude of the time difference between the high to low and low to high propagation delay times at an output.

Figure 4: VOLTAGE AND CURRENT DEFINITION

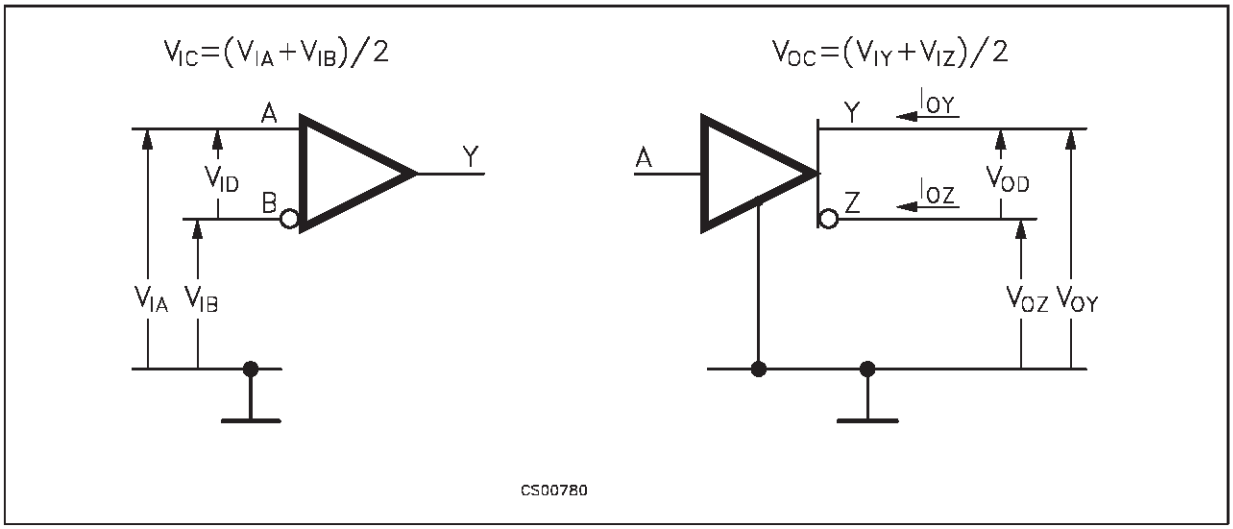


Figure 5: TEST CIRCUIT AND VOLTAGE DEFINITION FOR THE DIFFERENTIAL OUTPUT SIGNAL

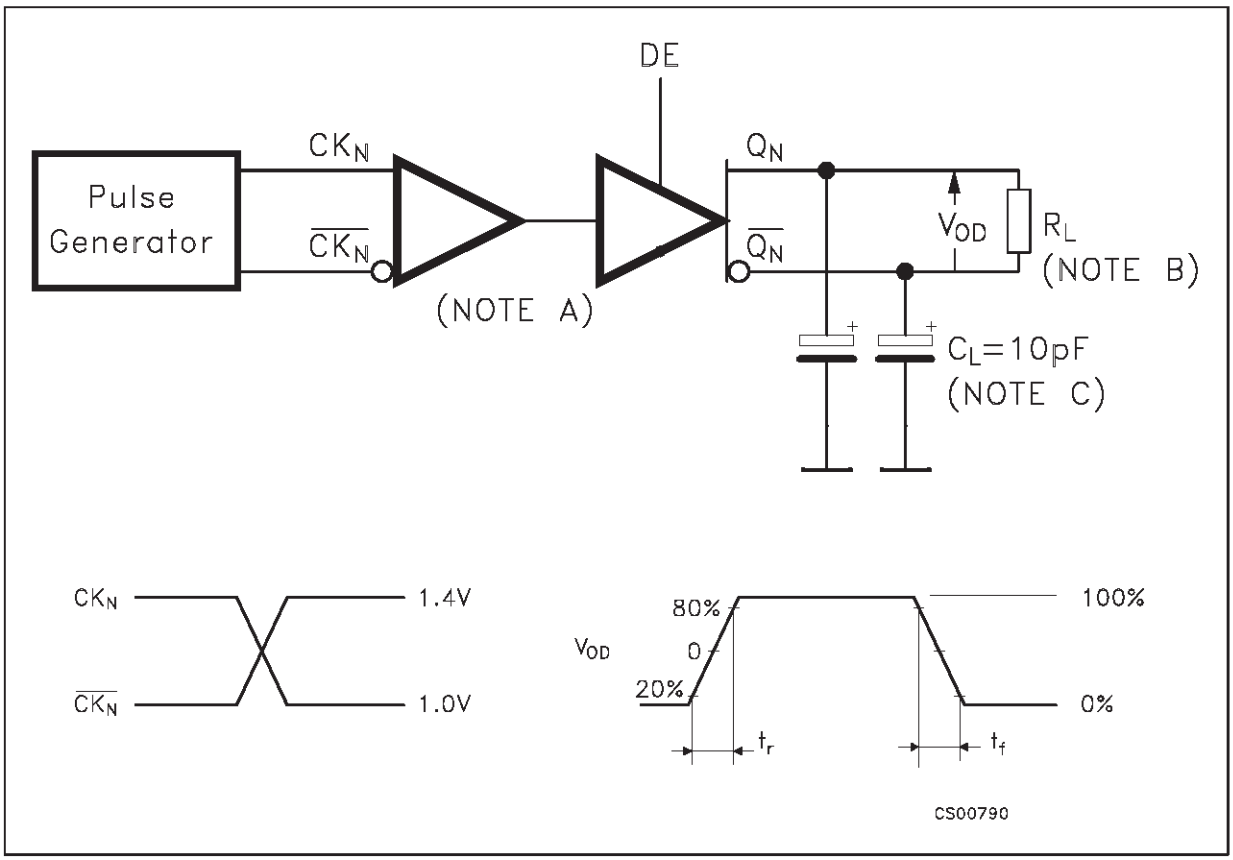


Figure 6: DIFFERENTIAL RECEIVER TO DRIVE PROPAGATION DELAY AND DRIVE TRANSITIO TIME WAVEFORMS

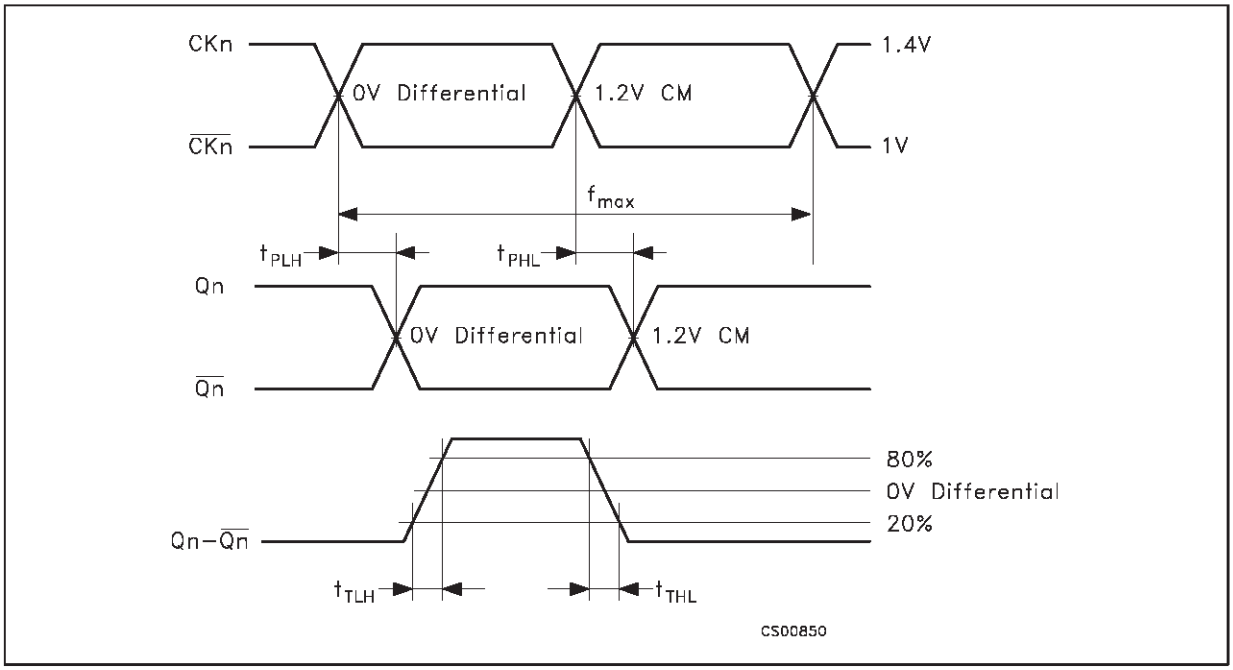
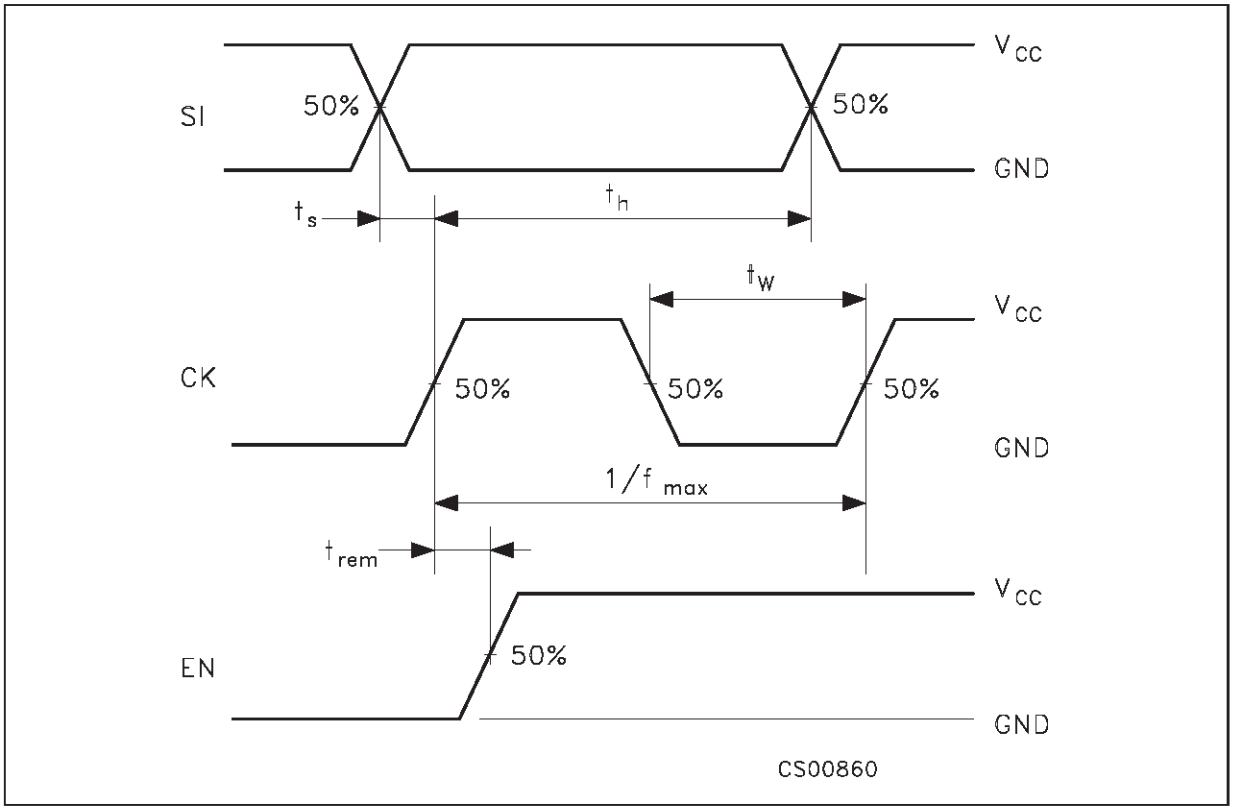
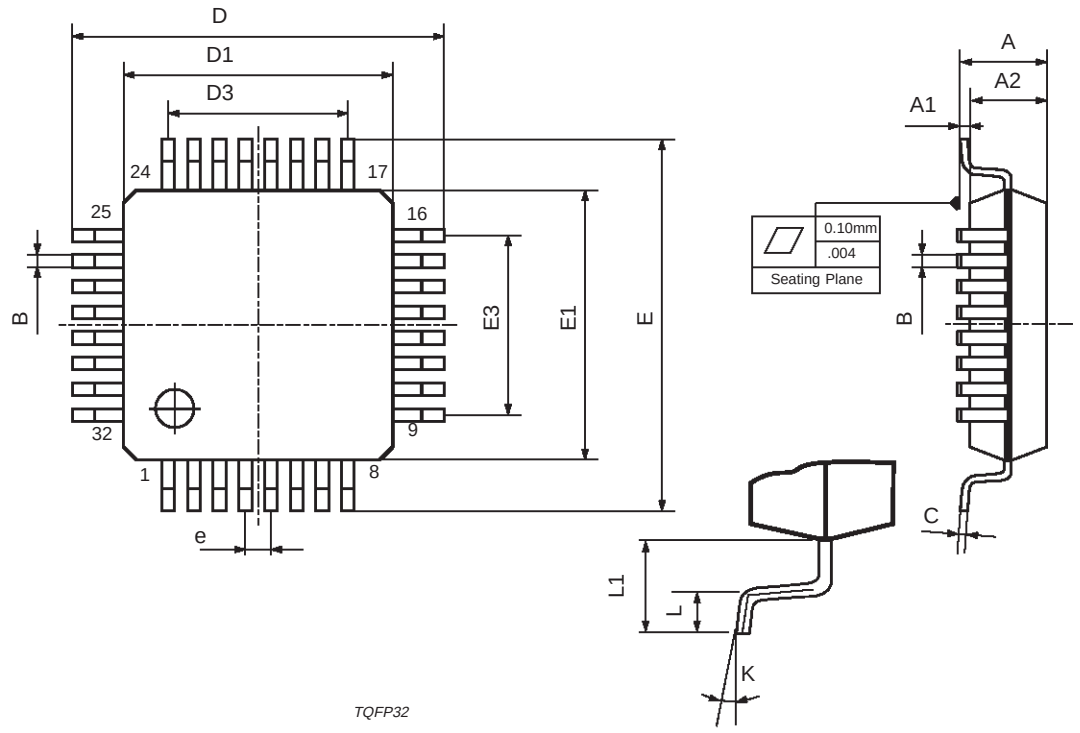


Figure 7: SET-UP, HOLD AND REMOVAL TIME, MAXIMUM FREQUENCY, MINIMUM PULSE WIDTH WAVEFORMS



TQFP32 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.30	0.37	0.45	0.012	0.015	0.018
C	0.09		0.20	0.004		0.008
D		9.00			0.354	
D1		7.00			0.276	
D3		5.60			0.220	
e		0.80			0.031	
E		9.00			0.354	
E1		7.00			0.276	
E3		5.60			0.220	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
K						



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