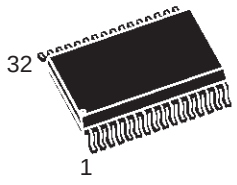
# M68Z512W

## 4 Mbit (512Kb x8) Low Voltage Low Power SRAM with Output Enable

**PRELIMINARY DATA**

- ULTRA LOW DATA RETENTION CURRENT
  - 600nA (typical)
  - 10µA (max)
- OPERATION VOLTAGE: 2.7 to 3.6V
- 512 Kbit x8 SRAM with OUTPUT ENABLE
- EQUAL CYCLE and ACCESS TIMES: 70ns
- LOW $V_{CC}$ DATA RETENTION: 1V
- TRI-STATE COMMON I/O
- CMOS for OPTIMUM SPEED/POWER
- AUTOMATIC POWER-DOWN WHEN DESELECTED
- INTENDED FOR USE WITH ST ZEROPOWER® AND TIMEKEEPER® CONTROLLERS




TSOP II 32 (NC)
10 x 20mm

### DESCRIPTION

The M68Z512W is a 4 Mbit (4,194,304 bit) CMOS SRAM, organized as 524,288 words by 8 bits. The device features fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. It requires a single 3V ±10% supply, and all inputs and outputs are TTL compatible.

This device has an automatic power-down feature, reducing the power consumption by over 99% when deselected.

The M68Z512W is available in a 32 lead TSOP II (10 x 20mm) package.

**Table 1. Signal Names**

| | |
|---|---|
| A0-A18 | Address Inputs |
| DQ0-DQ7 | Data Input/Output |
| $\overline{E}$ | Chip Enable |
| $\overline{G}$ | Output Enable |
| $\overline{W}$ | Write Enable |
| $V_{CC}$ | Supply Voltage |
| $V_{SS}$ | Ground |

**Figure 1. Logic Diagram**

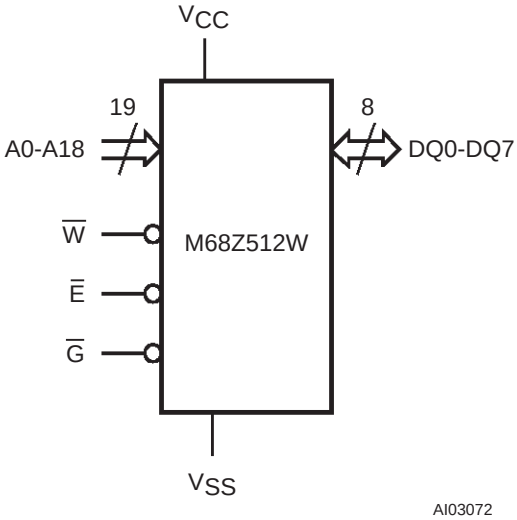
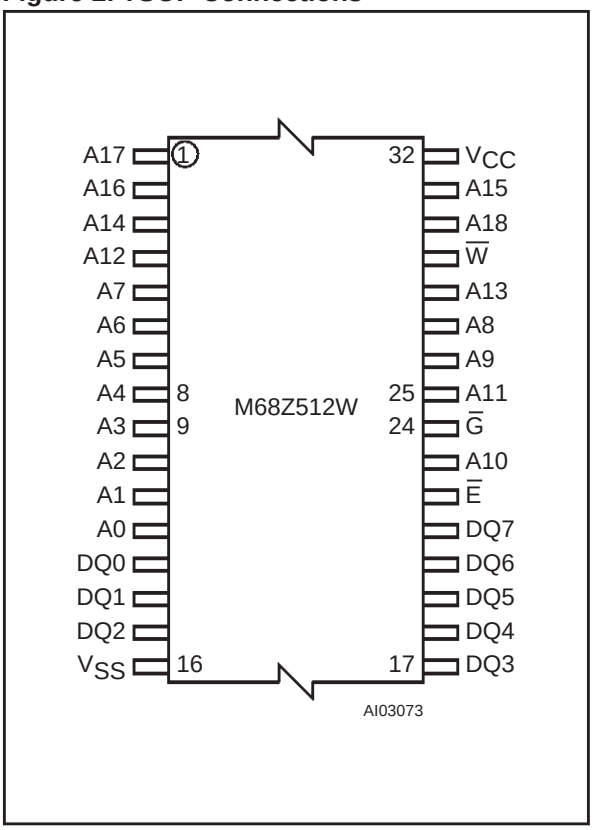


**Table 2. Absolute Maximum Ratings (1)**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $T_A$ | Ambient Operating Temperature | 0 to 70 | °C |
| $T_{STG}$ | Storage Temperature | –65 to 150 | °C |
| $V_{IO}$ (2) | Input or Output Voltage | –0.3 to $V_{CC}$ + 0.3 | V |
| $V_{CC}$ | Supply Voltage | –0.3 to 7.0 | V |
| $I_O$ (3) | Output Current | 20 | mA |
| $P_D$ | Power Dissipation | 1 | W |

Note: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.
2. Up to a maximum operating $V_{CC}$ of 3.6V only.
3. One output at a time, not to exceed 1 second duration.

**Figure 2. TSOP Connections**




## READ MODE

The M68Z512W is in the Read mode whenever Write Enable ($\overline{W}$) is High with Output Enable ($\overline{G}$) Low, and Chip Enable ($\overline{E}$) is asserted. This provides access to data from eight of the 4,194,304 locations in the static memory array, specified by the 19 address inputs. Valid data will be available at the eight output pins within $t_{AVQV}$ after the last stable address, providing $\overline{G}$ is Low and $\overline{E}$ is Low. If Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter ($t_{ELQV}$ or $t_{GLQV}$) rather than the address. Data out may be indeterminate at $t_{ELQX}$ and $t_{GLQX}$, but data lines will always be valid at $t_{AVQV}$.

## WRITE MODE

The M68Z512W is in the Write mode whenever the $\overline{W}$ and $\overline{E}$ pins are Low. Either the Chip Enable input ($\overline{E}$) or the Write Enable input ($\overline{W}$) must be de-asserted during Address transitions for subsequent write cycles. Write begins with the concurrence of Chip Enable being active with $\overline{W}$ low. Therefore, address setup time is referenced to Write Enable and Chip Enable as $t_{AVWL}$ and $t_{AVEH}$ respectively, and is determined by the latter occurring edge.

The Write cycle can be terminated by the earlier rising edge of $\overline{E}$, or $\overline{W}$.

if the Output is enabled ($\overline{E}$ = Low and $\overline{G}$ = Low), then $\overline{W}$ will return the outputs to high impedance within $t_{WLQZ}$ of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data input must be valid for $t_{DVWH}$ before the rising edge of Write Enable, or for $t_{DVEH}$ before the rising edge of $\overline{E}$, whichever occurs first, and remain valid for $t_{WHDX}$ or $t_{EHDX}$.

**Table 3. Operating Modes**

| Operation | $\overline{E}$ | $\overline{W}$ | $\overline{G}$ | DQ0-DQ7 | Power |
|---|---|---|---|---|---|
| Read | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | Hi-Z | Active |
| Read | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | Data Output | Active |
| Write | $V_{IL}$ | $V_{IL}$ | X | Data Input | Active |
| Deselect | $V_{IH}$ | X | X | Hi-Z | Standby |

Note: 1. X = $V_{IH}$ or $V_{IL}$.

**Table 4. AC Measurement Conditions**

| | |
|---|---|
| Input Rise and Fall Times | ≤ 5ns |
| Input Pulse Voltages | 0 to 3V |
| Input and Output Timing Ref. Voltages | 1.5V |

Note: Output Hi-Z is defined as the point where data is no longer driven.

## OPERATIONAL MODE

The M68Z512W has a Chip Enable power down feature which invokes an automatic standby mode whenever Chip Enable is de-asserted ($\overline{E}$ = High). An Output Enable ($\overline{G}$) signal provides a high speed tri-state control, allowing fast read/write cycles to be achieved with the common I/O data bus. Operational modes are determined by device control inputs $\overline{W}$ and $\overline{E}$ as summarized in the Operating Modes table.

**Figure 3. AC Testing Load Circuit**

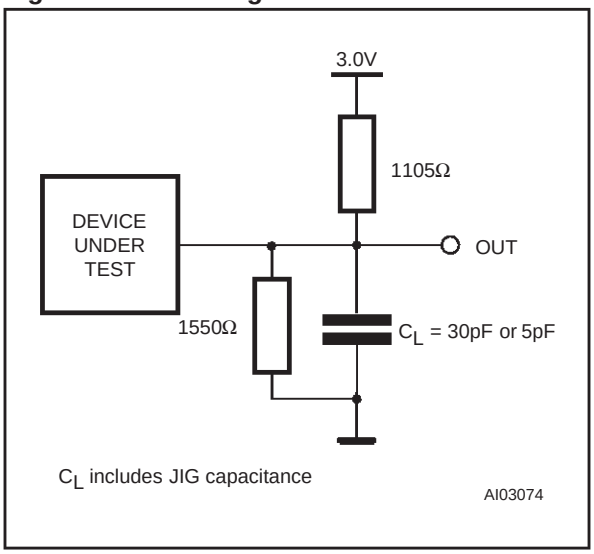



**Table 5. Capacitance** (1) ($T_A$ = 25°C, f = 1 MHz)

| Symbol | Parameter | Test Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance on all pins (except DQ) | $T_A$ = 25°C, f = 1MHz, $V_{CC}$ = 3V | | 6 | pF |
| $C_{OUT}$ (2) | Output Capacitance | $T_A$ = 25°C, f = 1MHz, $V_{CC}$ = 3V | | 8 | pF |

Note: 1. Sampled only, not 100% tested.
2. Outputs deselected.

**Figure 4. Block Diagram**

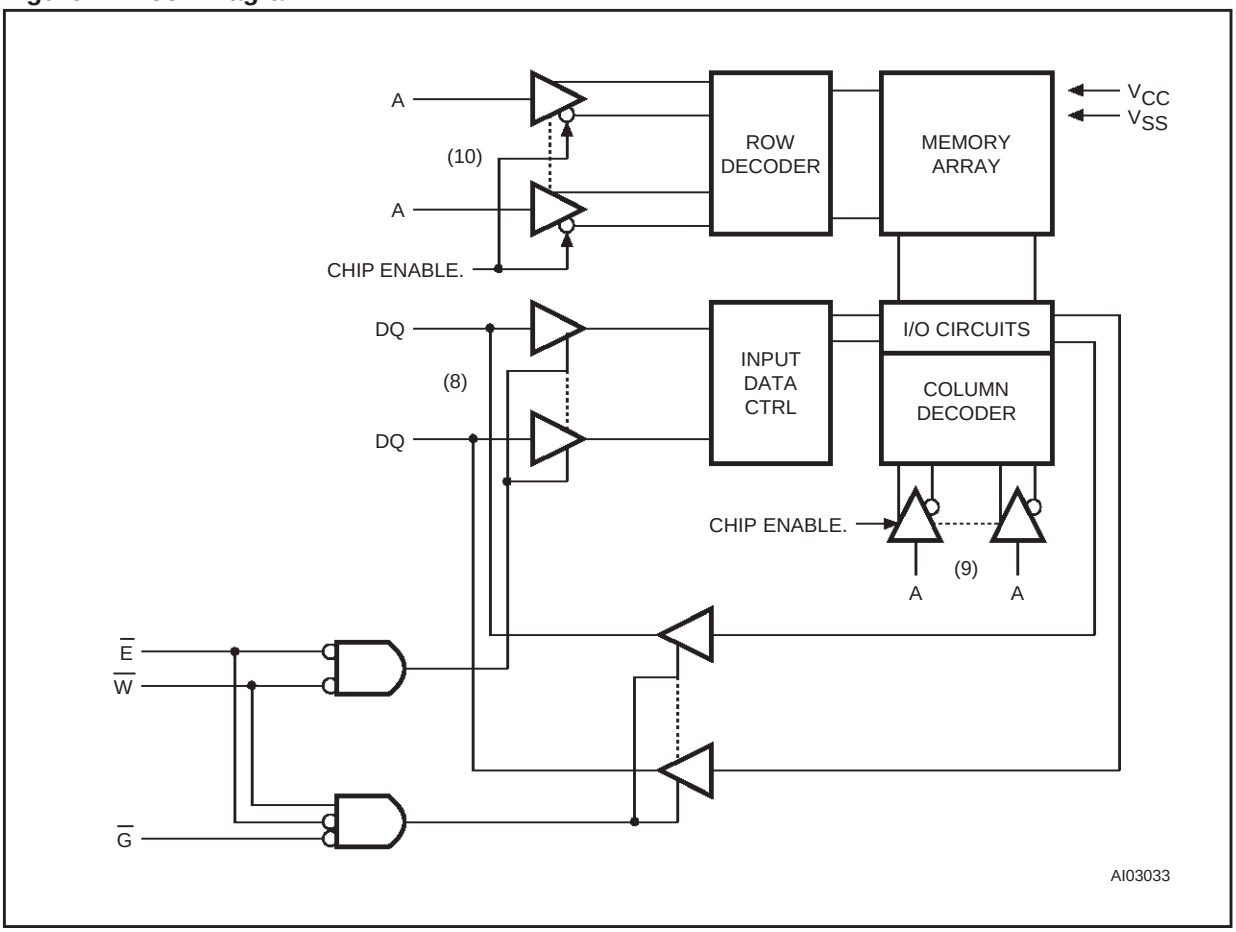



**Table 6. DC Characteristics**
($T_A$ = 0 to 70°C; $V_{CC}$ = 3V ±10%)

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Leakage Current | $0V \le V_{IN} \le V_{CC}$ | | | ±1 | µA |
| $I_{LO}$ | Output Leakage Current | $0V \le V_{OUT} \le V_{CC}$ | | | ±1 | µA |
| $I_{CC1}$ (1) | Supply Current | $V_{CC}$ = 3.6V | | 7 | 15 | mA |
| $I_{CC2}$ (2) | Supply Current (Standby) TTL | $V_{CC}$ = 3.6V, $\overline{E} = V_{IH}$ | | | 100 | µA |
| $I_{CC3}$ (3) | Supply Current (Standby) CMOS | $V_{CC}$ = 3.6V, $\overline{E} \ge V_{CC}$ – 0.3V, f = 0 | | 2 | 20 | µA |
| $V_{IL}$ | Input Low Voltage | | –0.3 | | 0.8 | V |
| $V_{IH}$ | Input High Voltage | | 2.2 | | $V_{CC}$ + 0.3 | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 2.1mA | | | 0.4 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = –1mA | 2.4 | | | V |

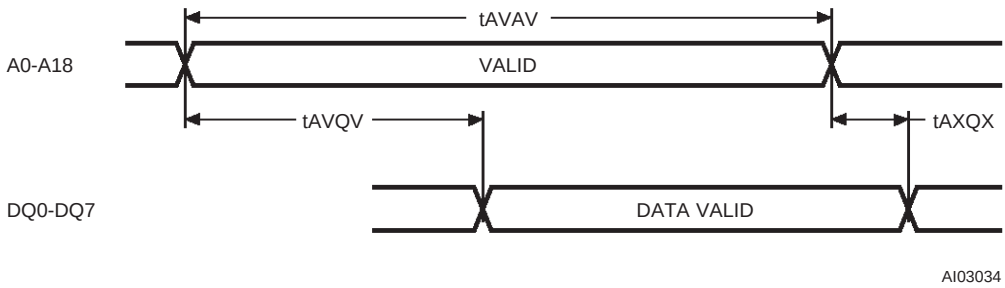
Note: 1. Average AC current, Outputs open, cycling at $t_{AVAV}$ minimum.
2. All other Inputs at $V_{IL} \le 0.8V$ or $V_{IH} \ge 2.2V$.
3. All other Inputs at $V_{IL} \le 0.3V$ or $V_{IH} \ge V_{CC}$ –0.3V.

**Table 7. Read Mode AC Characteristics**
($T_A$ = 0 to 70°C; $V_{CC}$ = 2.7 to 3.6V)

| Symbol | Parameter | M68Z512W | | Unit |
|---|---|---|---|---|
| | | -70 | | |
| | | Min | Max | |
| $t_{AVAV}$ | Read Cycle Time | 70 | | ns |
| $t_{AVQV}$ (1) | Address Valid to Output Valid | | 70 | ns |
| $t_{ELQV}$ (1) | Chip Enable Low to Output Valid | | 70 | ns |
| $t_{GLQV}$ (1) | Output Enable Low to Output Valid | | 35 | ns |
| $t_{ELQX}$ (3) | Chip Enable Low to Output Transition | 10 | | ns |
| $t_{GLQX}$ (3) | Output Enable Low to Output Transition | 5 | | ns |
| $t_{EHQZ}$ (2,3) | Chip Enable High to Output Hi-Z | | 25 | ns |
| $t_{GHQZ}$ (2,3) | Output Enable High to Output Hi-Z | | 25 | ns |
| $t_{AXQX}$ (1) | Address Transition to Output Transition | 10 | | ns |
| $t_{PU}$ | Chip Enable Low to Power Up | 0 | | ns |
| $t_{PD}$ | Chip Enable High to Power Down | | 70 | ns |

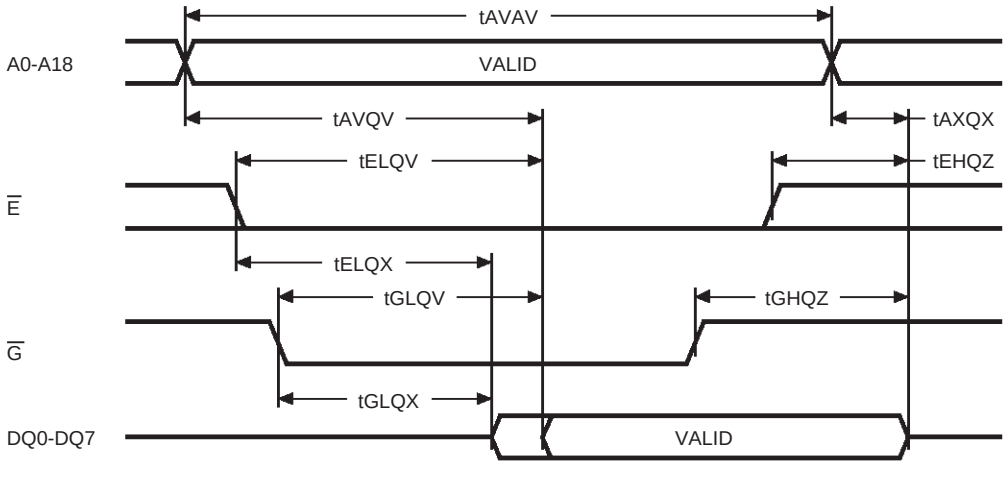
Note: 1. $C_L$ = 100pF.
2. $C_L$ = 5pF.
3. At any given temperature and voltage condition, $t_{EHQZ}$ is less than $t_{ELQX}$ and $t_{GHQZ}$ is less than $t_{GLQX}$ for any given device.

**Figure 5. Address Controlled, Read Mode AC Waveforms**




Note: $\overline{E}$ = Low, E2 = High, $\overline{G}$ = Low, $\overline{W}$ = High.

**Figure 6. Chip Enable or Output Enable Controlled, Read Mode AC Waveforms.**




Note: Write Enable ($\overline{W}$) = High.

**Figure 7. Standby Mode AC Waveforms**

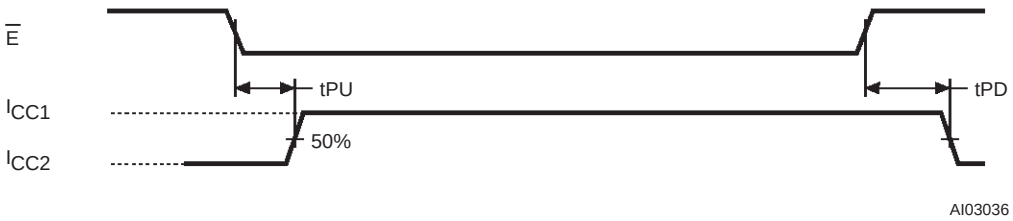
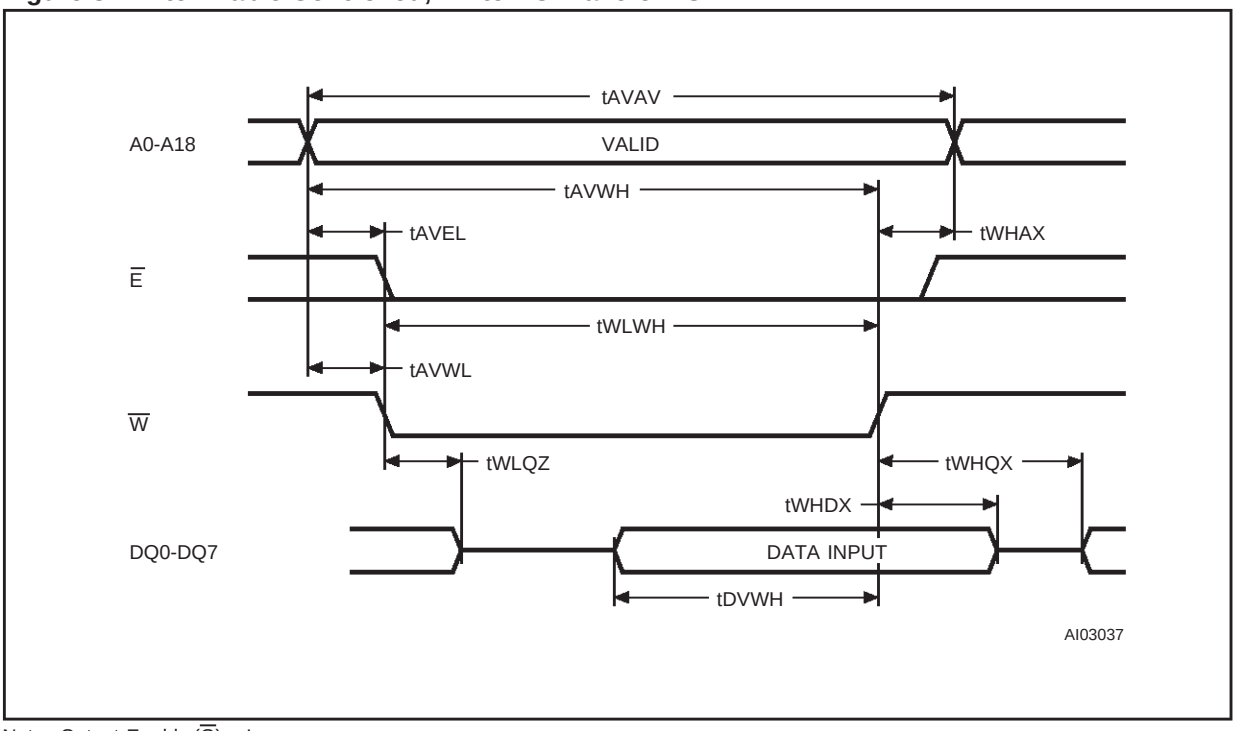


**Table 8. Write Mode AC Characteristics**
($T_A$ = 0 to 70°C; $V_{CC}$ = 2.7 to 3.6V)

| Symbol | Parameter | M68Z512W | | Unit |
|---|---|---|---|---|
| | | -70 | | |
| | | Min | Max | |
| $t_{AVAV}$ | Write Cycle Time | 70 | | ns |
| $t_{AVWL}$ | Address Valid to Write Enable Low | 0 | | ns |
| $t_{AVWH}$ | Address Valid to Write Enable High | 60 | | ns |
| $t_{AVEH}$ | Address Valid to Chip Enable High | 60 | | ns |
| $t_{WLWH}$ | Write Enable Pulse Width | 50 | | ns |
| $t_{WHAX}$ | Write Enable High to Address Transition | 0 | | ns |
| $t_{WHDX}$ | Write Enable High to Input Transition | 0 | | ns |
| $t_{WHQX}$ (2) | Write Enable High to Output Transition | 10 | | ns |
| $t_{WLQZ}$ (1,2) | Write Enable Low to Output Hi-Z | | 25 | ns |
| $t_{AVEL}$ | Address Valid to Chip Enable Low | 0 | | ns |
| $t_{ELEH}$ | Chip Enable Low to Chip Enable High | 60 | | ns |
| $t_{EHAX}$ | Chip Enable High to Address Transition | 0 | | ns |
| $t_{DVWH}$ | Input Valid to Write Enable High | 30 | | ns |
| $t_{DVEH}$ | Input Valid to Chip Enable High | 30 | | ns |

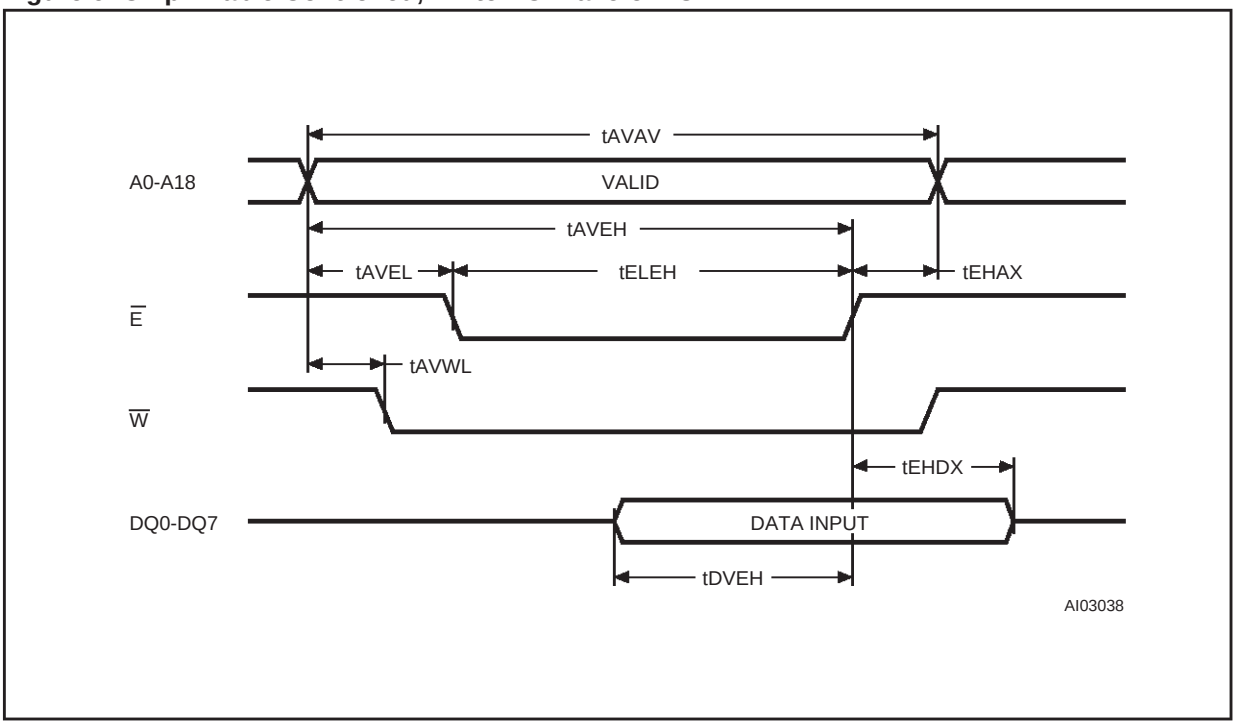
Note: 1. $C_L$ = 5pF.
2. At any given temperature and voltage condition, $t_{WLQZ}$ is less than $t_{WHQX}$ for any given device.

**Figure 8. Write Enable Controlled, Write AC Waveforms**




Note: Output Enable ($\overline{G}$) = Low.

**Figure 9. Chip Enable Controlled, Write AC Waveforms (1,2)**




Note: 1. Output Enable ($\overline{G}$) = High.
2. If $\overline{E}$ goes High with $\overline{W}$ high, the output remains in a high-impedance state.

**Table 9. Low $V_{CC}$ Data Retention Characteristics**
($T_A$ = 0 to 70°C)

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{CCDR}$ (1) | Supply Current (Data Retention) | $V_{CC}$ = 3V, $\overline{E} \geq V_{CC} - 0.3V$ | | 0.4 | 10 | µA |
| $V_{DR}$ | Supply Voltage (Data Retention) | $\overline{E} \geq V_{CC} - 0.3V$ or E2 ≤ 0.3V, f = 0 | 2 | | | V |
| $t_{CDR}$ | Chip Disable to Power Down | $\overline{E} \geq V_{CC} - 0.3V$ or E2 ≤ 0.3V, f = 0 | 0 | | | ns |
| $t_{ER}$ (2) | Operation Recovery Time | | $t_{AVAV}$ | | | ns |

Note: 1. Typical condition: $T_A$ = 25°C.
2. See Figure 10 for measurement points. Guaranteed but not tested. $t_{AVAV}$ is Read cycle time.

**Figure 10. Low $V_{CC}$ Data Retention AC Waveforms**

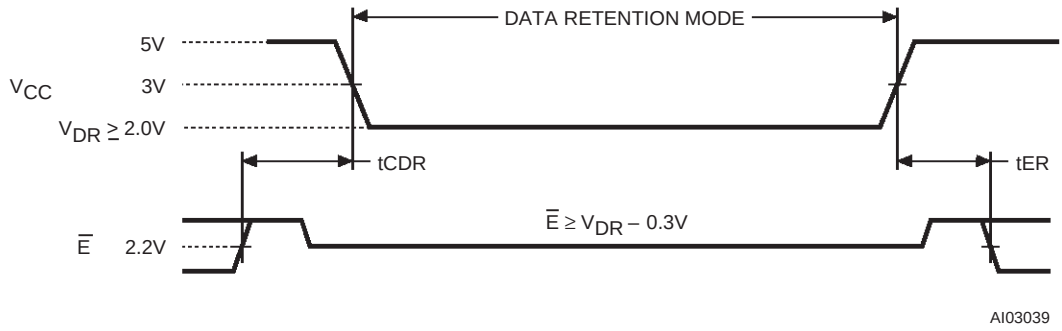
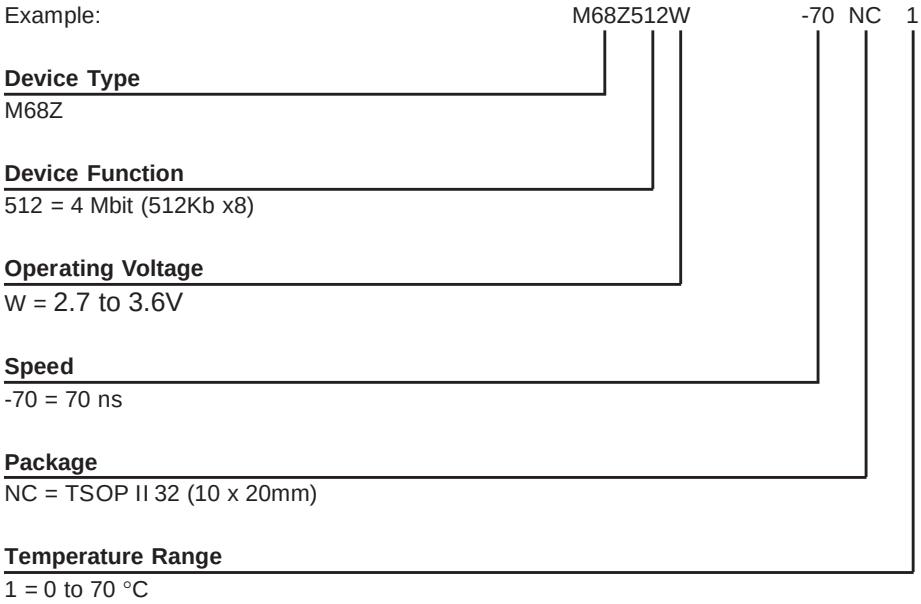


**Table 10. Ordering Information Scheme**




For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

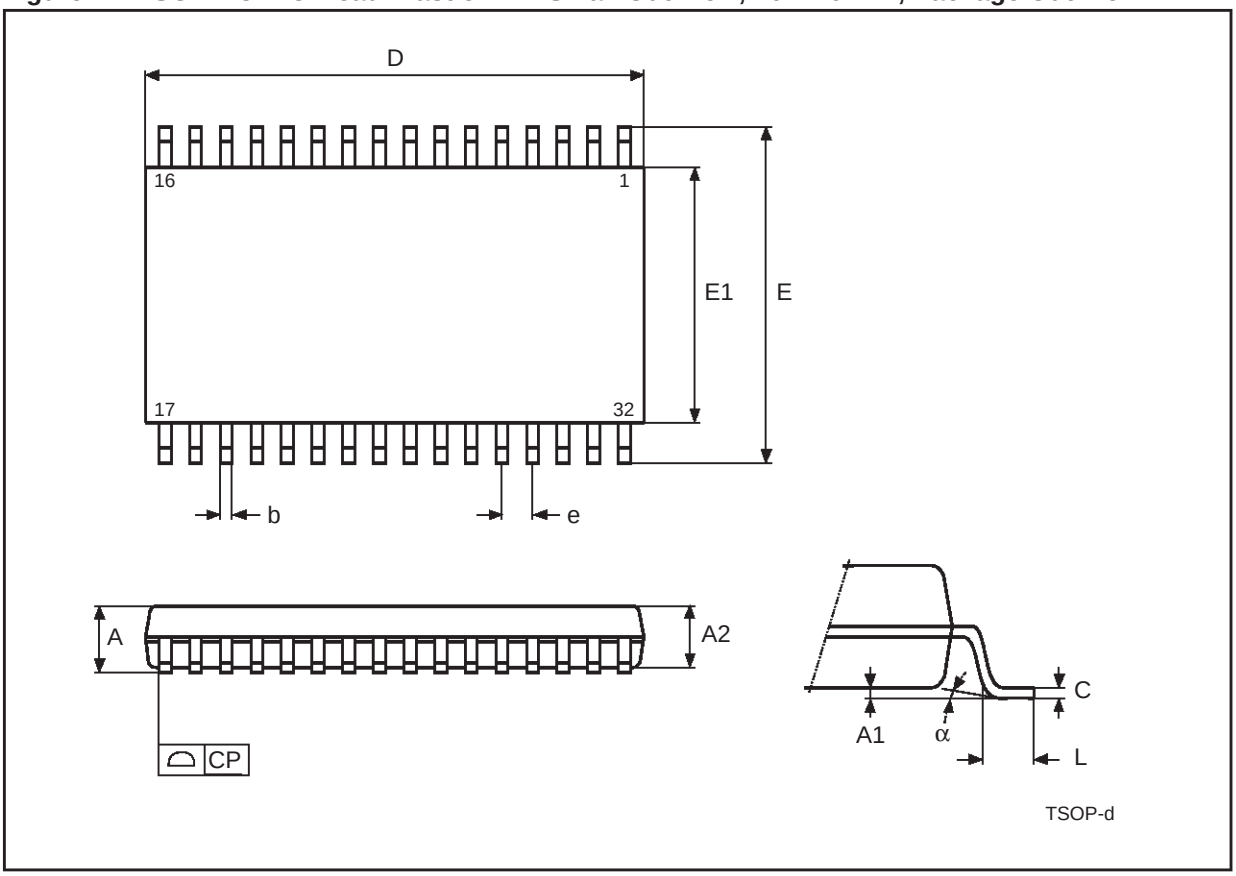
**Table 11. Revision History**

| Date | Revision Details |
|---|---|
| July 1999 | First Issue |
| 06/28/00 | TSOP32 II Package Dimension Changed (Table 12)<br>From Target Specification To Preliminary Data |
| 07/26/00 | Ordering Information Scheme changed (Table 10) |
| 09/21/00 | $I_{CCDR}$ Supply Current changed (Table 9) |

**Table 12. TSOP II 32 - 32 lead Plastic Thin Small Outline II, 10 x 20 mm, Package Mechanical Data**

| Symbol | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | Typ | Min | Max | Typ | Min | Max |
| A | | | 1.20 | | | 0.047 |
| A1 | | 0.05 | 0.15 | | 0.002 | 0.006 |
| A2 | | 0.95 | 1.05 | | 0.037 | 0.041 |
| b | | 0.30 | 0.52 | | 0.012 | 0.020 |
| C | | 0.12 | 0.21 | | 0.005 | 0.008 |
| CP | | | 0.10 | | | 0.004 |
| D | | 20.82 | 21.08 | | 0.820 | 0.830 |
| e | 1.27 | – | – | 0.050 | – | – |
| E | | 11.56 | 11.96 | | 0.455 | 0.471 |
| E1 | | 10.03 | 10.29 | | 0.395 | 0.405 |
| L | | 0.40 | 0.60 | | 0.016 | 0.024 |
| α | | 0° | 5° | | 0° | 5° |
| N | 32 | | | 32 | | |

**Figure 11. TSOP II 32 - 32 lead Plastic Thin Small Outline II, 10 x 20 mm, Package Outline**

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