AN1082
APPLICATION NOTE

DESCRIPTION OF THE ST72141 MOTOR CONTROL PERIPHERAL REGISTERS

by Microcontroller Division Applications

INTRODUCTION

The ST72141 is designed for controlling Brushless Permanent Magnet DC motors with or without sensors.

The motor control is performed by the hardware of the on-chip Motor Control peripheral (MTC). The MTC is functionally divided into four parts.

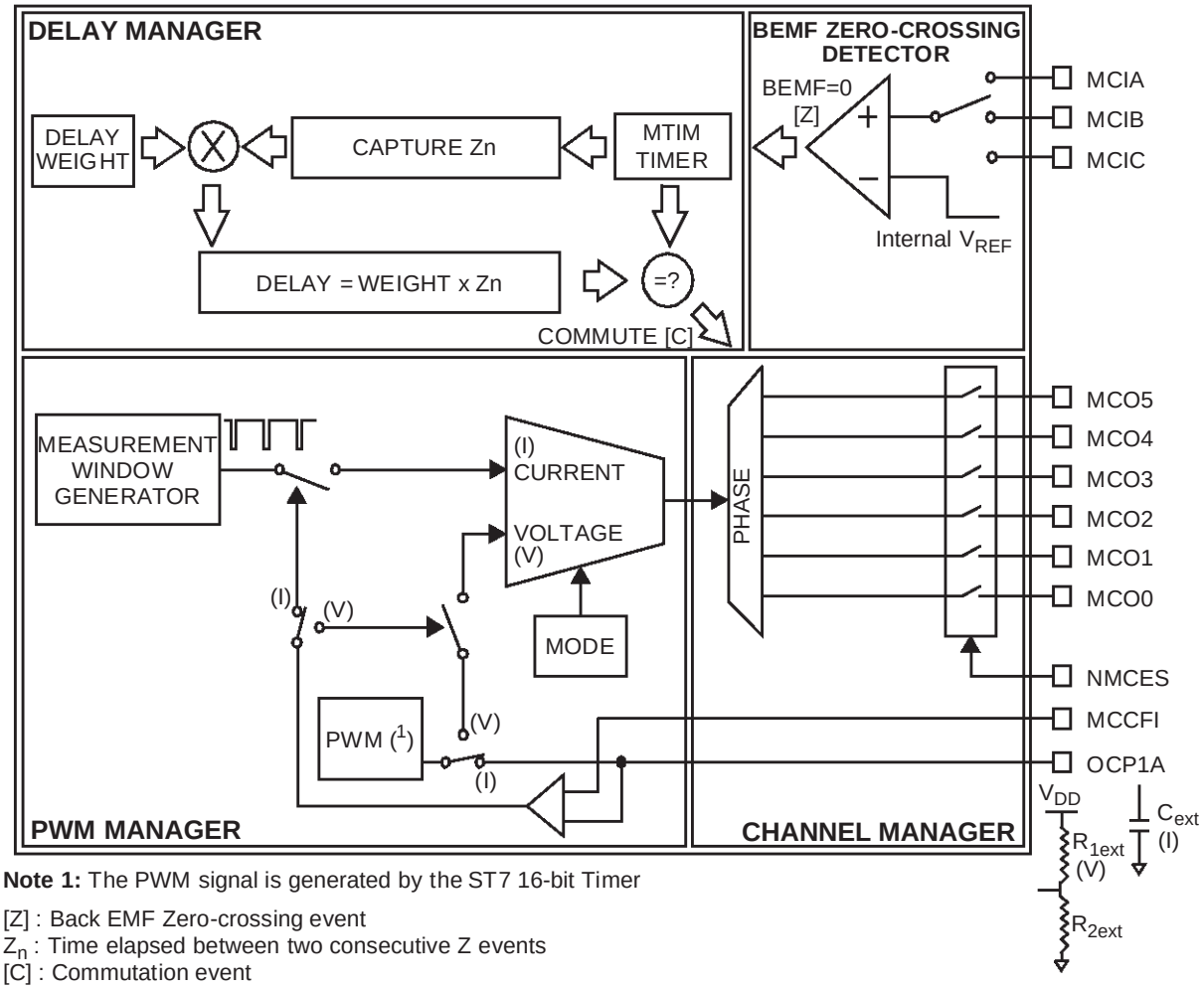
– Zero-crossing and End of Demagnetisation detector

– Delay manager

– PWM manager

– Channel manager

Figure 1. Peripheral general overview



Note 1: The PWM signal is generated by the ST7 16-bit Timer

[Z] : Back EMF Zero-crossing event
Z_n : Time elapsed between two consecutive Z events
[C] : Commutation event
C_n : Time delayed after Z event to generate C event
(I): Current mode
(V): Voltage mode

The procedure for driving the motor with the ST72141 is based on the detection of 3 events:

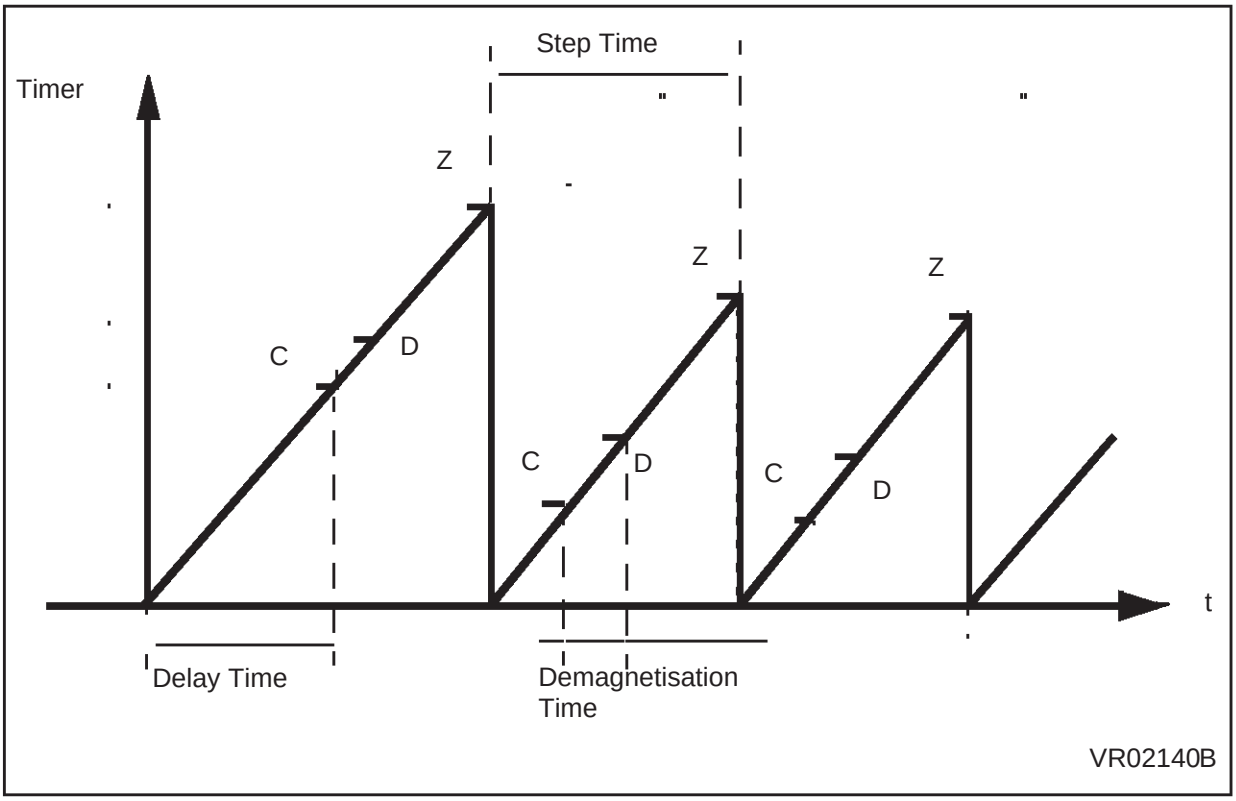
– Commutation event (C event)

– End of Demagnetisation event (D event)

– Zero crossing event (Z event)

The last two of these are physical events which are monitored and read by the ST72141. The first event (commutation) is computed and triggered automatically by the ST72141 in order to keep the motor running at optimum efficiency.

Figure 2. Event Timing Diagram



These events always occur in the same order: first Commutation, then End of Demagnetisation and finally the back-EMF Zero Crossing event.

The Zero-Crossing and Demagnetisation detection part of the peripheral manages the two physical events. In order to detect the Zero-Crossing event, the motor phase signal is sampled at different frequencies depending on the driving mode. To detect the End of demagnetisation event, it is always sampled at a fixed frequency of 800KHz in sensorless mode.

The delay manager is the part of the peripheral where the first event (commutation) is computed: The computed delay is the time between the Zero Crossing event and the next Commutation event.

The PWM manager part of the peripheral is the part which generates the PWM signals that are applied to the switches in current or voltage mode, and are needed to detect the physical events. The reference current of the motor (in current mode) and the reference voltage (in voltage mode) are also generated in this part.

The last part, the channel manager, is where the six microcontroller outputs, connected to the 6 switches, are managed depending on the step configuration.

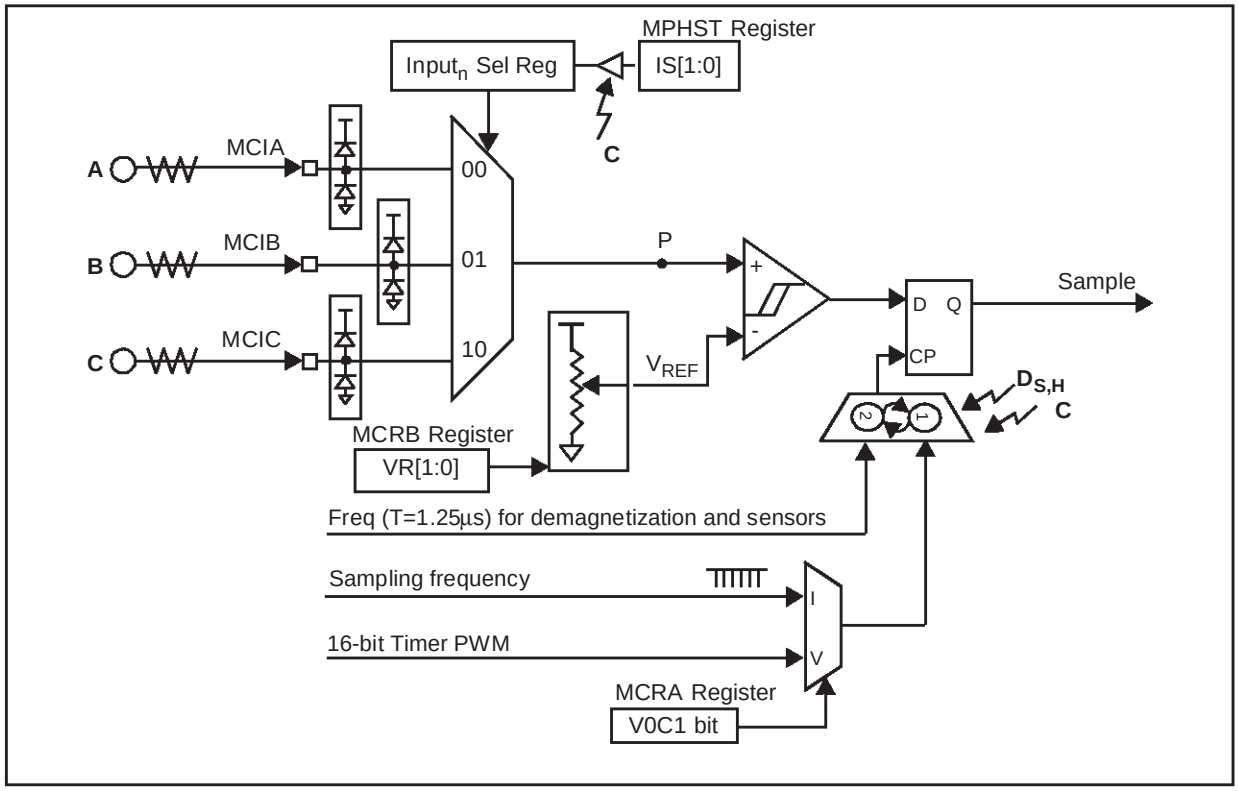
In the ST72141 motor control peripheral, some registers have a preload register, they are indicated in the figures by an asterisk (*). For example, the MPHST register (phase state register) has a preload register meaning that it can be configured in advance, the values are taken into account at the next Commutation event.

The MCRB register (Motor Control register B) has a partial preload register, only some bits can be preloaded for the next commutation event.

The purpose of this application note is to give a precise description of all the registers of the ST72141 motor control peripheral and the functions associated with them.

1 ZERO-CROSSING AND END OF DEMAGNETISATION DETECTOR

Figure 3. Phase input sampling description



MCIA, MCIB and MCIC are the analog voltage inputs where the phase voltage signal is read.

The IS[1:0] bits, bit 7 and bit 6 in the MPHST register, allow you to select the phase where the back-EMF signal will be read. Phase A (from the MCIA input), phase B (from the MCIB input) or phase C (from the MCIC input). For each step, the phase where the signal will be read to detect the End of Demagnetisation event and the zero-crossing event is always the one which is not energised. The signal coming from the phase is one of the inputs of the internal comparator.

The VR[1:0] bits (bit 7 and bit 6 of the MCRB register) set the reference voltage threshold for all analog input signals from the MCIA, MCIB or MCIC microcontroller inputs.

As we can see in Figure 3, the sampling frequency of the phase voltage signal is always 800Khz (4Mhz/5) for the detection of the **end of demagnetisation event in sensorless mode** whichever mode is used to drive the motor (current or voltage mode).

The sampling frequency of the phase voltage for detecting the Zero-crossing event depends on the mode used to drive the motor in **sensorless configuration.**

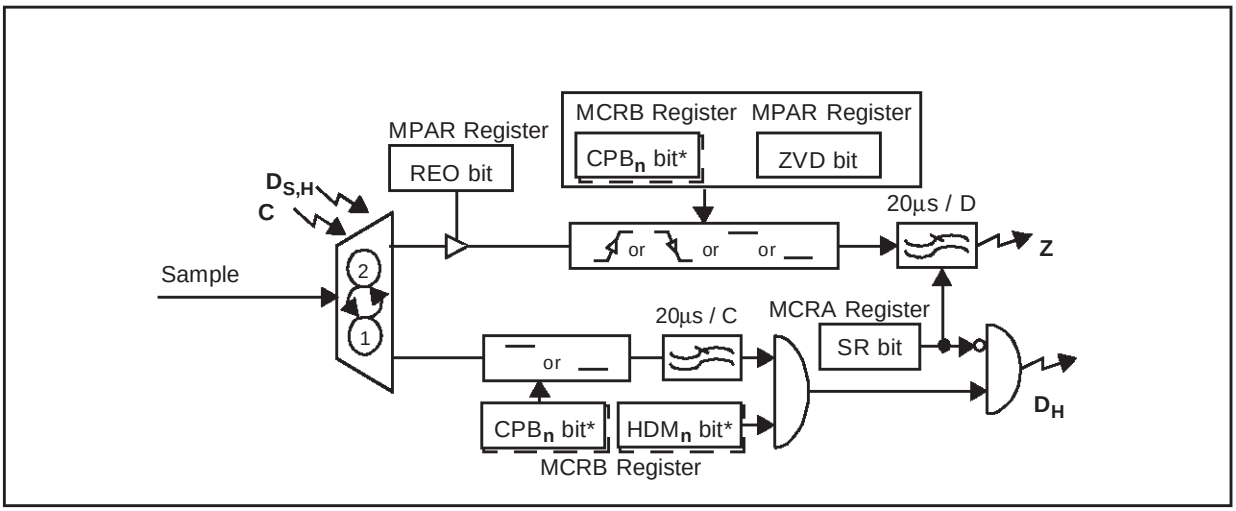
– In current mode, this sampling frequency comes from the internal clock.

– In voltage mode, this sampling frequency comes directly from Timer A. Timer A is an on-chip timer peripheral of the ST72141 that is external to the motor control peripheral.

In sensor configuration, the sampling frequency of the signal from the motor sensor for **zero-crossing event detection** is always 800 kHz.

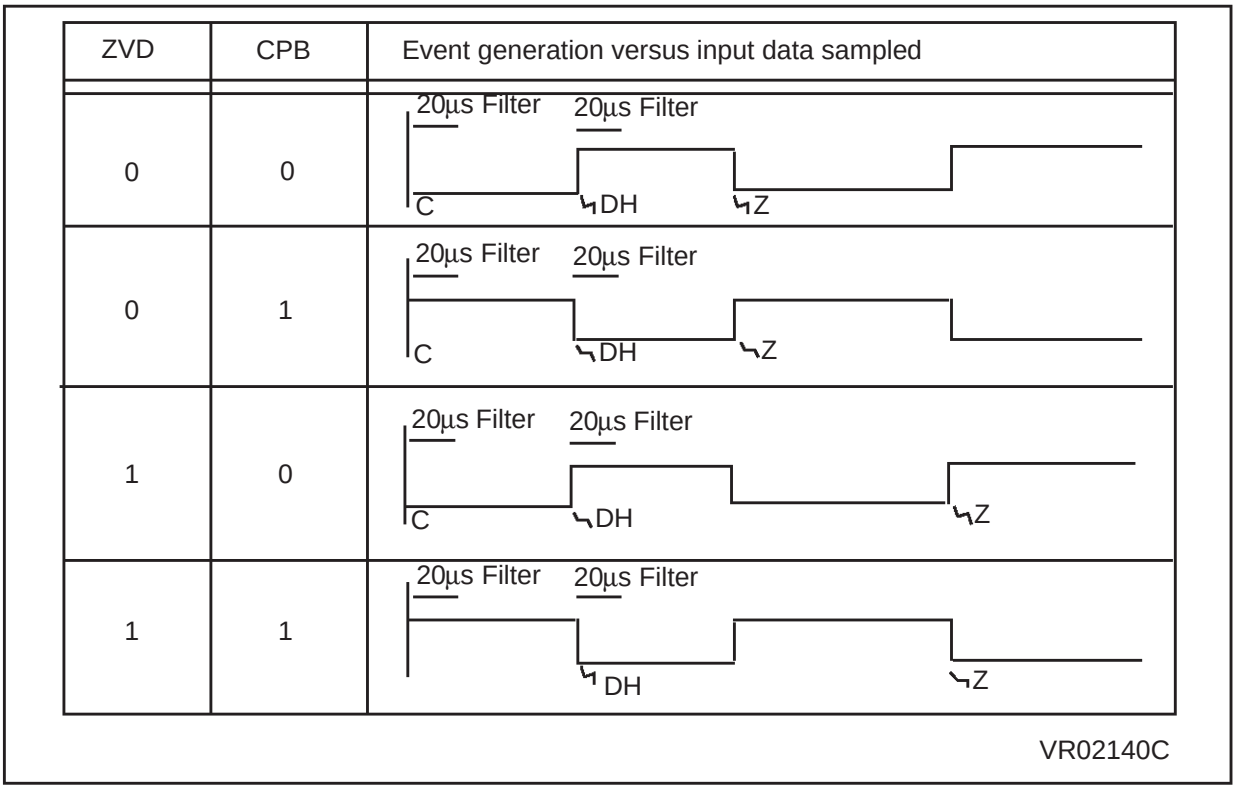
The VOC1 bit (bit 3 of the MCRA register) selects the driving mode (voltage mode or current mode).

Figure 4. Hardware D event and Z event mechanism



The REO bit (bit 6 of the MPAR register) selects the even or odd channel used to read the back-EMF signal at the end of the PWM off-time.

Figure 5. ZVD and CPB level selection



The ZVD bit (bit 7 of the MPAR register) allows you to choose the Z event versus D event edge polarity.

The CPB bit (bit 5 of the MCRB register) allows you to choose the edge polarity for detecting the Zero Crossing event, to be falling edge or rising edge.

With the ZVD and CPB bits, you can select the transition pattern of both End of Demagnetisation and Zero Crossing events, if they have the same level or opposing levels for both high or low levels.

The two first configurations (ZVD=0, CPB=1 or 0) are when Z and D events have opposing-edge transition.

The two last configurations (ZVD=1, CPB=1 or 0) are when Z and D events have same-edge transition.

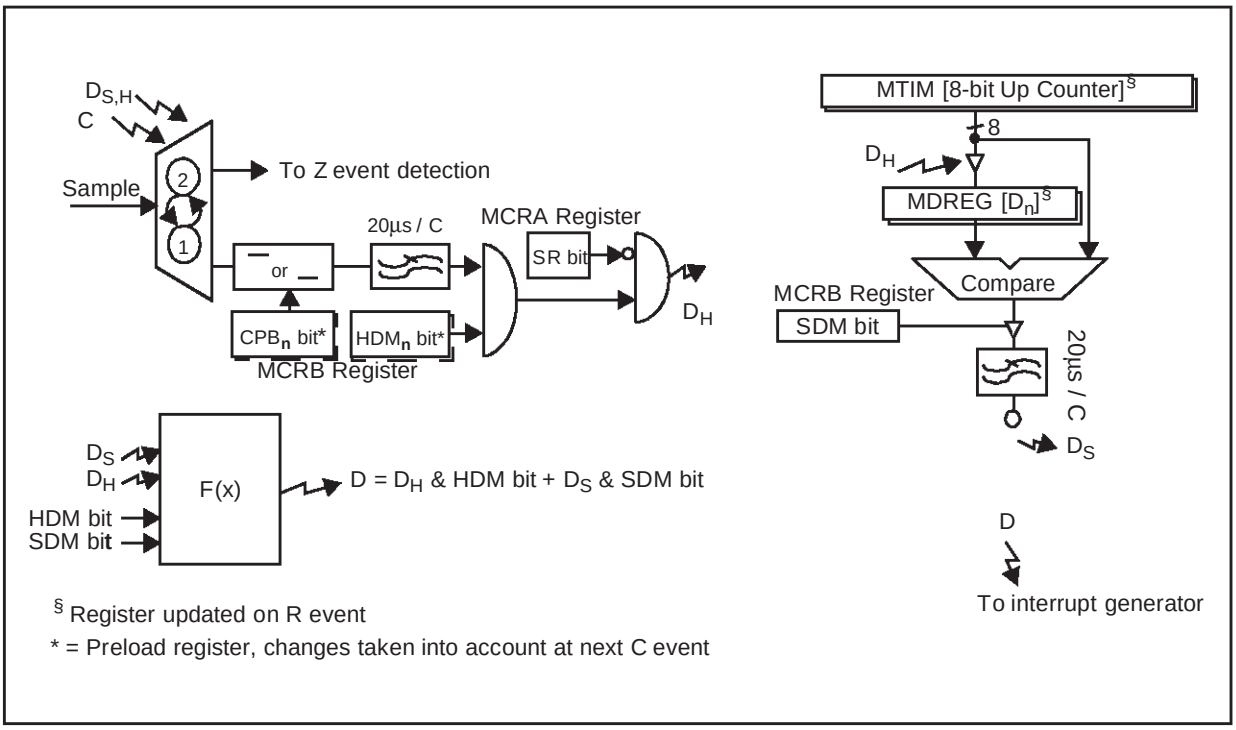
In practice, in a Brushless Permanent Magnet DC motor, Z and D events always have opposing-edge transition.

The SR bit (bit 5 of the MCRA register) indicates if we are in sensor mode or in sensorless mode, this bit is configured at the initialisation of the peripheral.

The ST72141 motor control peripheral allows you to simulate the End of Demagnetisation event. This is called software demagnetisation. The HDM and SDM bits (bit 3 and bit 4 of the MCRB register) indicate if you are using a hardware demagnetisation (HDM bit is set) or software demagnetisation (SDM bit is set). This is useful in certain cases (depending on the edge of the detection of this event) when it is difficult to detect the hardware demagnetisation. The HDM, SDM and CPB bits are accessed by preload register, this means that we can change the configuration step by step. In Figure 4 we see the hardware demagnetisation and the Z event mechanism. Figure 6 adds the software demagnetisation mechanism to the previous figure (Figure 4).

The threshold voltage set by the VR[1:0] bits (Figure 3) is the same for the detection of the end of demagnetisation and the zero crossing events. The threshold voltage can be selected from four different values (0.2, 0.6, 1.2, 2.5V).

Figure 6. Software D event mechanism



In our case, on the falling edge of the demagnetisation, we make a software end of demagnetisation event and on the rising edge of the demagnetisation, we have a hardware end of demagnetisation. When a step requiring hardware demagnetisation occurs, the time of this hardware demagnetisation is captured in the MDREG register. This time will be used to compute a software demagnetisation time for the next step.

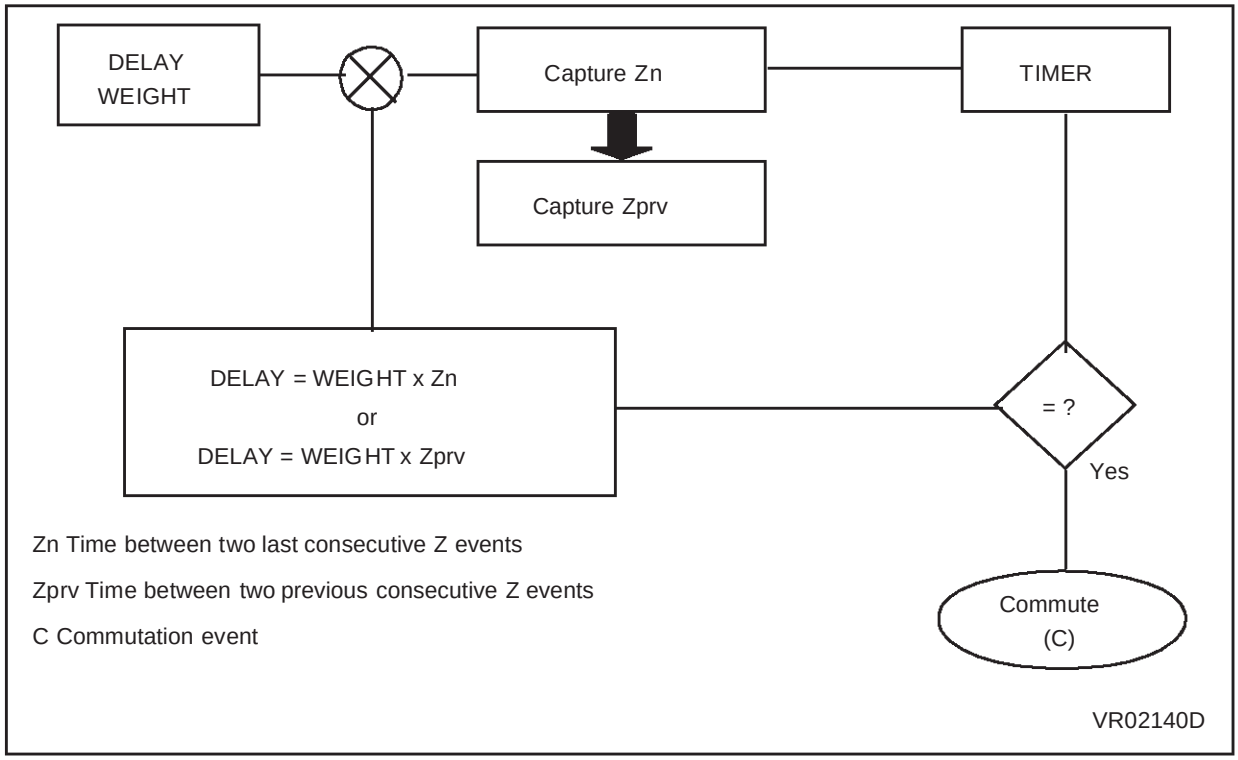
The value captured in the MDREG register when the hardware demagnetisation occurs is computed with a corrector coefficient and then reloaded in the MDREG register in order to respect 2 conditions:

– The software demagnetisation time computed must be always greater than the MTIM value at the time the register MDREG is refreshed (if the MTIM value is greater than the software demagnetisation value, no end of demagnetisation event will be detected and therefore the window for monitoring the zero crossing event will not be opened).

– The software demagnetisation value must be always greater than the MCOMP register value for the same step because MCOMP register contains the delay before the commutation, and the end of demagnetisation event must always occur after the commutation event.

2 DELAY MANAGER

Figure 7. Delay manager general overview

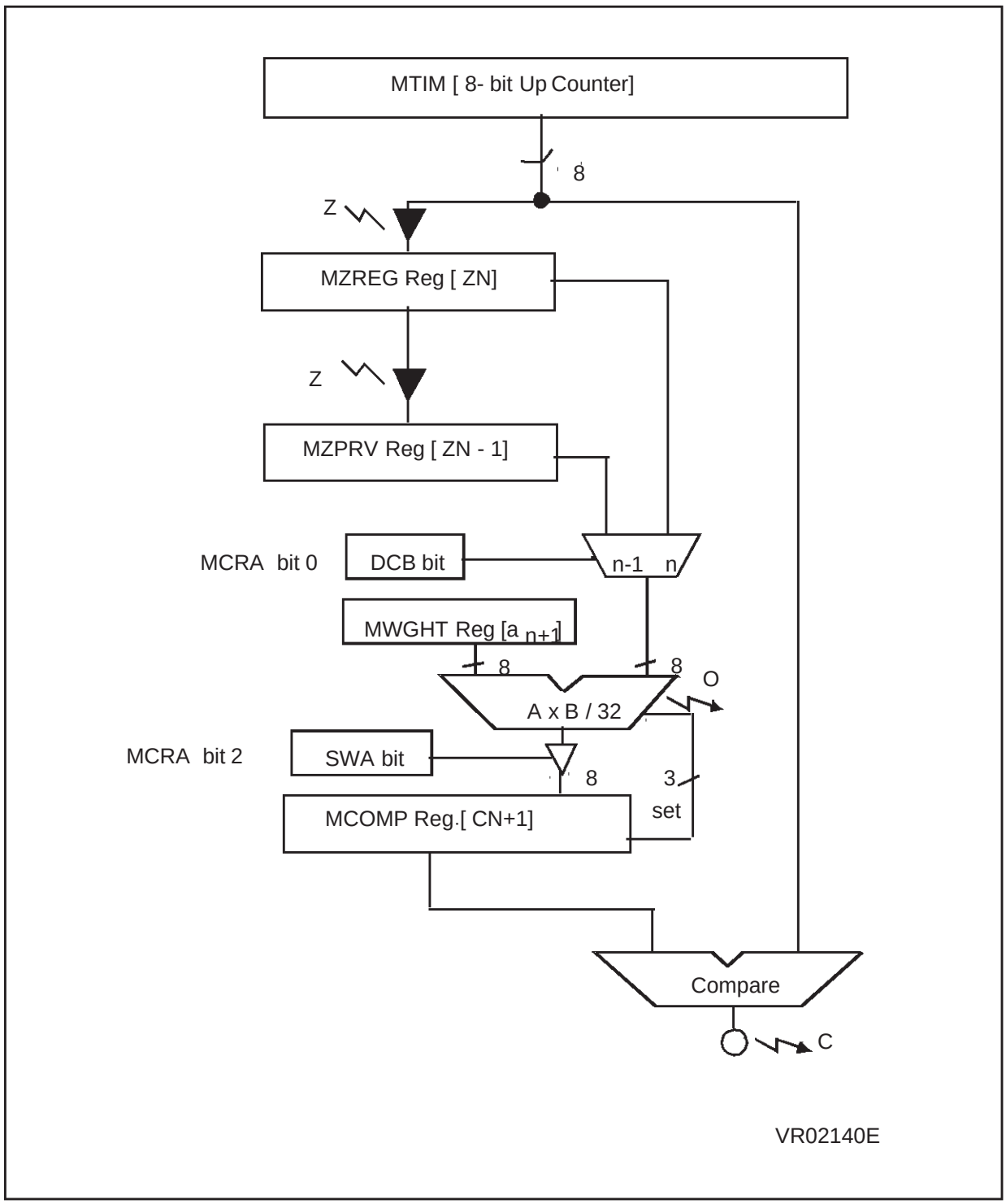


When a Z event is detected in the Zero crossing detector part of the peripheral, the value of the internal 8 bit timer of the peripheral (MTIM) is captured and then MTIM is reset (in auto commutated mode). This value will be used with the delay coefficient (DELAY WEIGHT in MWGHT register) to calculate the computed delay (time between the Z event and the next commutation event).

We can calculate the computed delay on the actual Z event (Zn) or on the previous one (Z previous). It depends on the motor type. Z previous is useful for dissymmetrical motors.

In fact, when a Z event occurs, the value of MTIM is captured and put in the MZREG register (Z actual) before the MTIM is reset and the value which was already in the MZREG register resulting from the previous Z event is put in the MZPRV previous register).

Figure 8. Commutation event generation



MCOMP, MZPREV, MZREG and MTIM are updated on R event (MTIM ratio change).

All the data in the preload registers are transferred to the active registers at the C event.

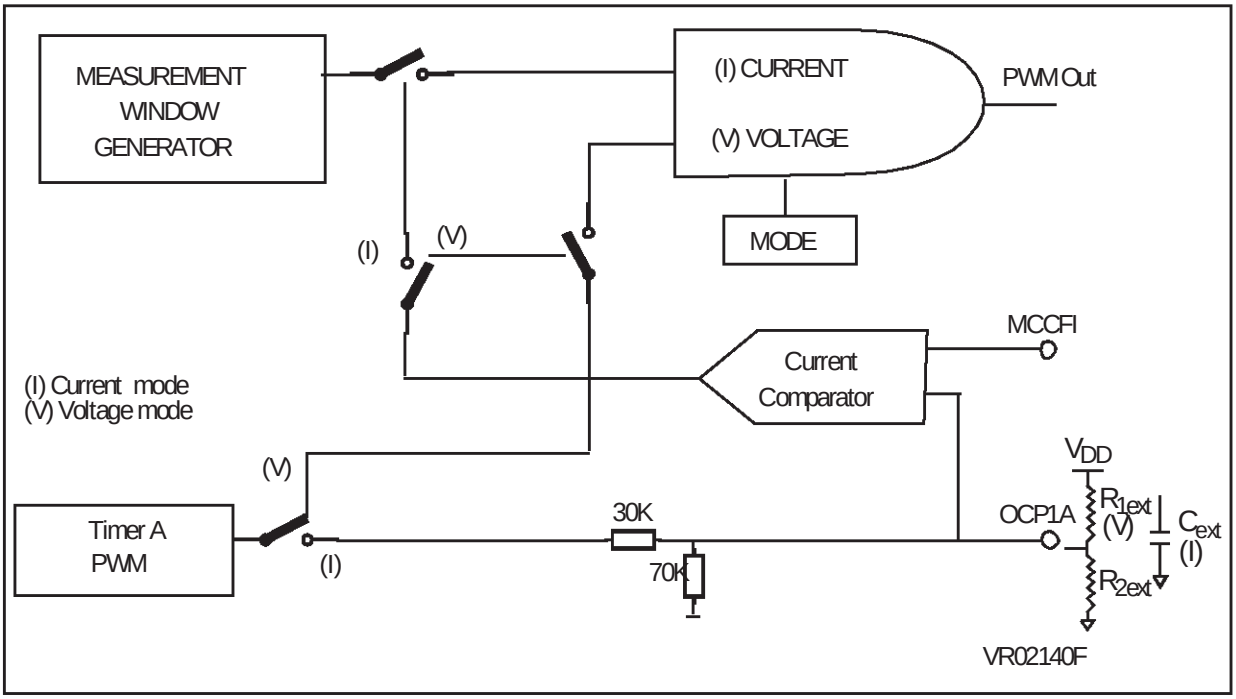
The DCB bit in the MCRA register selects if the calculation of the computed delay is done with Z actual or Z previous time. The step time (time between two Z events in auto-commutated mode) is multiplied by the delay coefficient in the MWGHT register and then divided by 32. The result of this operation gives the computed delay (time between the actual Z event and the next commutation). This is done automatically by the microcontroller and keeps the motor running at optimum efficiency.

The result of the operation is put in the MCOMP register, when the MTIM value (reset on Z event in auto-commutated mode) reaches the value in the MCOMP register, the commutation will happen (C event).

The SWA bit (bit 2 of the MCRA register) indicates if we are in switched (starting sequence) or auto-commutated mode. Effectively, in synchronous (switched) mode the MCOMP register contains the imposed step time and not the computed delay.

3 PWM MANAGER

Figure 9. PWM Manager General overview



In current mode, Timer A sets the motor reference current (depending on the required torque). This current reference is input to the internal comparator with the current feedback from the motor. The internal clock sets the PWM frequency which will be applied to the switches. The frequency of this PWM is also the sampling frequency of the phase voltage signal for detecting the Z event **in sensorless mode**.

Each time (in current mode) the current feedback from the motor reaches the current reference set by Timer A, the PWM signal previously set by the internal clock goes off. The duty cycle of this PWM is variable and has a minimum off-time to allow stabilization of the system before reading.

In voltage mode, Timer A sets the voltage to be applied to the motor and this PWM signal is also applied to the switches (in voltage mode, the internal clock is no longer used to set the PWM signal applied to the switches, it is only used to sample at 800KHz the signal from the motor phases). So, in voltage mode, the PWM frequency of Timer A is also the sampling frequency of the phase voltage signal for detecting the zero crossing event **in sensorless mode**. In voltage mode, the entry of the internal comparator compared to the current feedback from the motor is not the current reference but the current limitation. As we can see in Figure 9, this current limitation can be set by an external divider or directly on the OCP1A pin.

Figure 10. Sampling clock generation

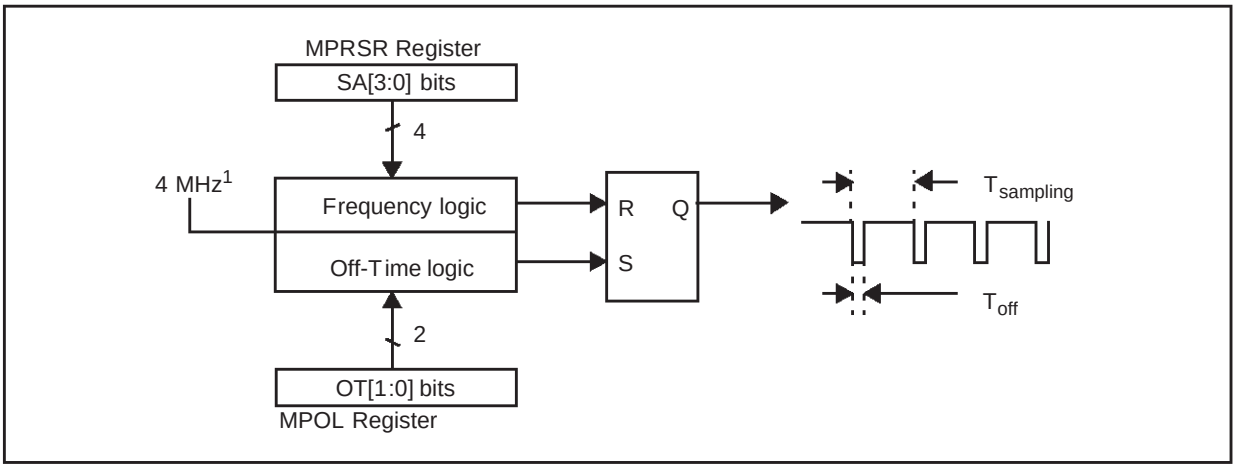


Table 1. Sampling Frequency Selection Bits

SA3	SA2	SA1	SA0	Sampling Frequency
0	0	0	0	25.0 KHz
0	0	0	1	20.0 KHz
0	0	1	0	18.1 KHz
0	0	1	1	15.4 KHz
0	1	0	0	12.5 KHz
0	1	0	1	10.0 KHz
0	1	1	0	6.25 KHz
0	1	1	1	3.13 KHz
1	0	0	0	1.56 KHz
1	0	0	1	1.25 KHz
1	0	1	0	1.14 KHz
1	0	1	1	961 Hz
1	1	0	0	781 Hz
1	1	0	1	625 Hz
1	1	1	0	390 Hz
1	1	1	1	195 Hz

Table 2. Off-Time Selection bits

OT1 bit	OT0 bit	Off-Time Sensorless Mode (SR bit=0)	Off-Time Sensor Mode (SR bit =1)
0	0	5 µs	1.25 µs
0	1	10 µs	
1	0	15 µs	
1	1	30 µs	

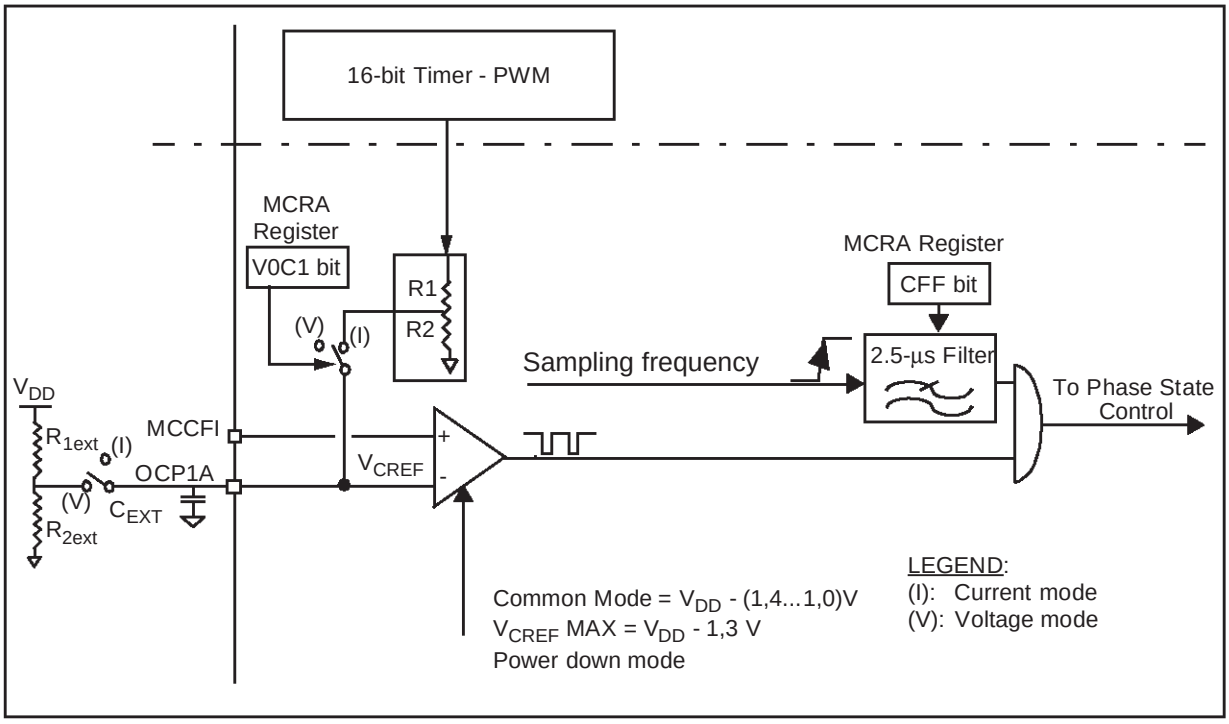
Figure 10 shows the sampling clock generation **in current mode** with the internal clock Motor Control peripheral (4 MHz in this case).

The internal clock PWM signal must have a minimum off time of 5 µs to allow the stabilization of the system before reading, this off time is chosen between 4 values in sensorless mode (5, 10, 15, 30 µs). In sensor mode, the off-time is fixed at 1.25 µs.

The SA[3:0] bits in the MPRSR register allow the user to change the internal clock frequency. Increasing the frequency of the internal clock PWM signal increases the resolution (in current mode) but there are more losses in the transistors.

Note: In either driving mode is (current or voltage mode) the sampling frequency of the phase voltage for detecting the end of demagnetisation event is 800kHz (4MHz/5). If the MTC peripheral input frequency is different, this will change the sampling frequency.

Figure 11. Current feedback description



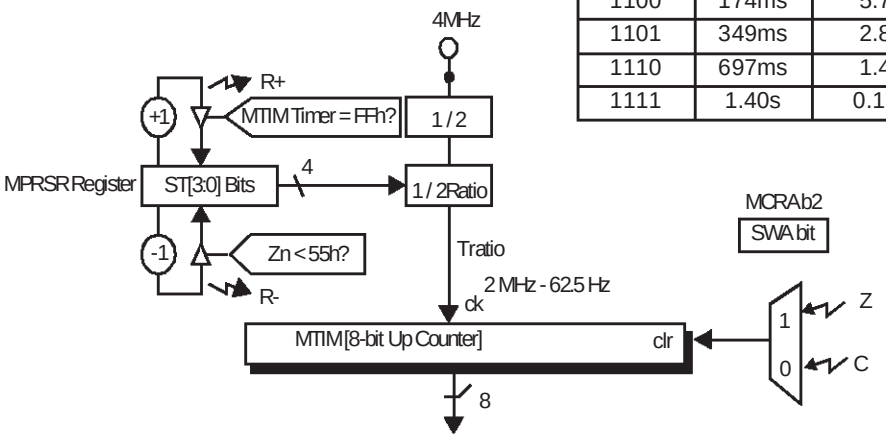
In current mode, the current reference is provided to the comparator by the PWM output of the Timer A, filtered through a RC filter.

The sensed current is input on the MCCFI pin. By setting the CFF bit, (bit 1 of the MCRB register), a 2.5 µs filter at each switching on of the PWM can be applied on the comparator output, to mask possible spikes due to the diode recovery current.

In voltage mode, the current comparator is used as a current limitation for safety purposes. The current limit value is set by an external resistor divider (The resistor values are set by the user depending on the application needs). This current limitation can be set also directly throught the OCP1A pin.

Figure 12. MTIM overview

Step Ratio Register ST[3:0]	Minimum Step period	Maximum Step Frequency (Hz)	Maximum Step period	minimum Step Frequency (Hz)
0000	42.5µs	23.5k	127.5µs	7.85k
0001	85µs	11.7k	255µs	3.93k
0010	170µs	5.88k	510µs	1.96k
0011	340µs	2.94k	1.02ms	980
0100	680µs	1.47k	2.04ms	490
0101	1.36ms	735	4.08ms	245
0110	2.72ms	367	8.16ms	123
0111	5.44ms	183	16.32ms	81.3
1000	10.9ms	91.9	32.6ms	30.7
1001	21.8ms	45.9	65.2ms	15.4
1010	43.6ms	22.9	130ms	7.66
1011	87ms	11.4	261ms	3.83
1100	174ms	5.74	522ms	1.92
1101	349ms	2.87	1.04s	0.958
1110	697ms	1.43	2.08s	0.479
1111	1.40s	0.178	4.17s	0.240



All MTIM registers are in Read-Write mode until the internal clock is enabled (with MOE and DAC bits). This is useful for initializing the timer, prescaler register and compare for start-up.

In sensorless and in synchronous (switched) mode, the prescaler is loaded with an initial value and then it can be incremented or decremented by software.

In the MPRSR register (prescaler register), the ST [3:0] bits allow you to select the ratio of the MTIM. Each ratio (from 0 to 15) corresponds to a minimum and maximum step time.

To start directly in auto-commutated mode, for example with sensors, write an appropriate value in the MZREG register and MZPRV register to perform a step calculation as soon as the clock is enabled.

The MTIM 8-bit internal timer is designed to capture the Z event between 55h (85 decimal) and FFh, this gives an accuracy of 1.17% (1/85) in the worst case. If there is an overflow (R+ event) or an underflow (R- event) of the timer, it is reset to its middle value =7Fh.

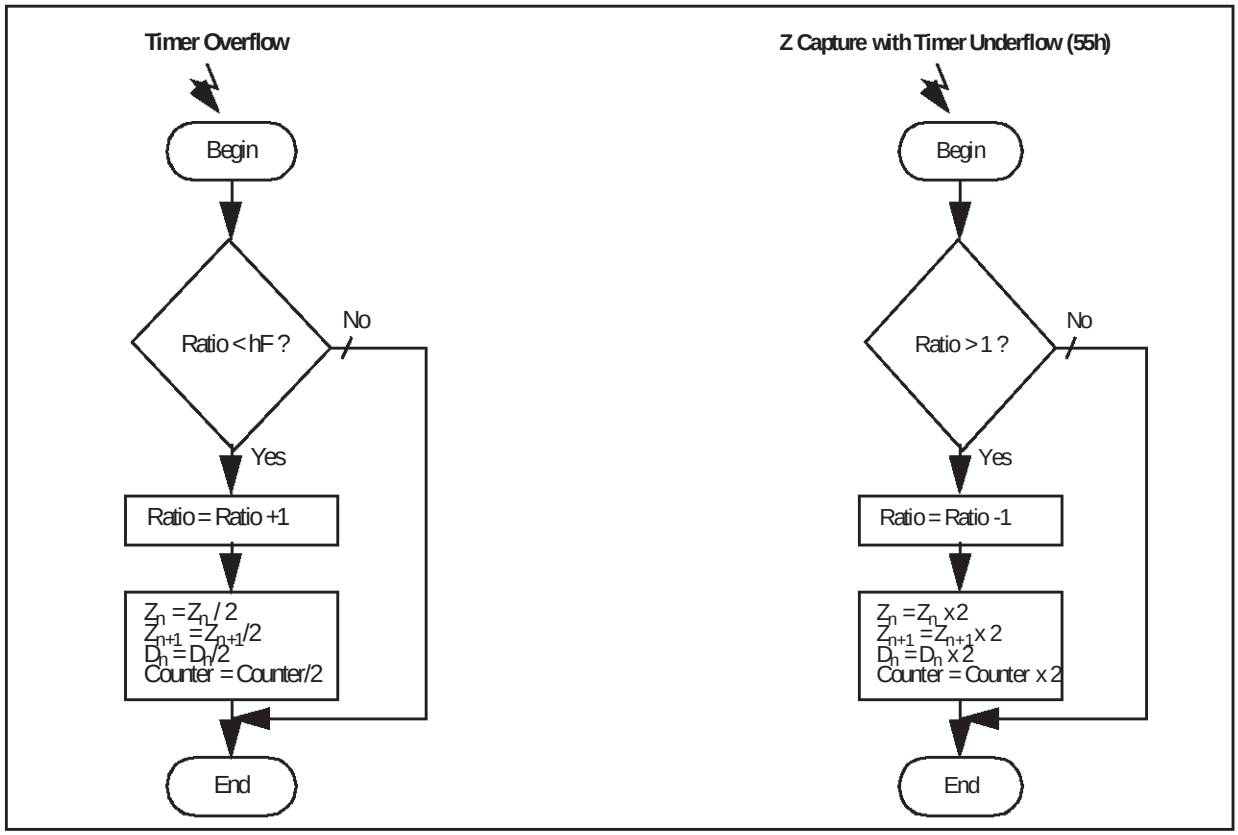
The R+ event means that MTIM reaches FFh before the Z event or the D event occurs.

The R- event means that MTIM value is under 55h when the Z event occurs.

R+ and R- events constitute the R event where some registers are updated.

When there is an R event (R+ or R-) on MTIM, the prescaler of MTIM is automatically incrmented or decremented order to keep the capture of the Z event between 55h and FFh.

Figure 13. R+ and R- events



For example: If the ratio of MTIM is 0101:

If there is an R+ event, we need to slow down the clock so the ratio is increased from 0101 to 0110.

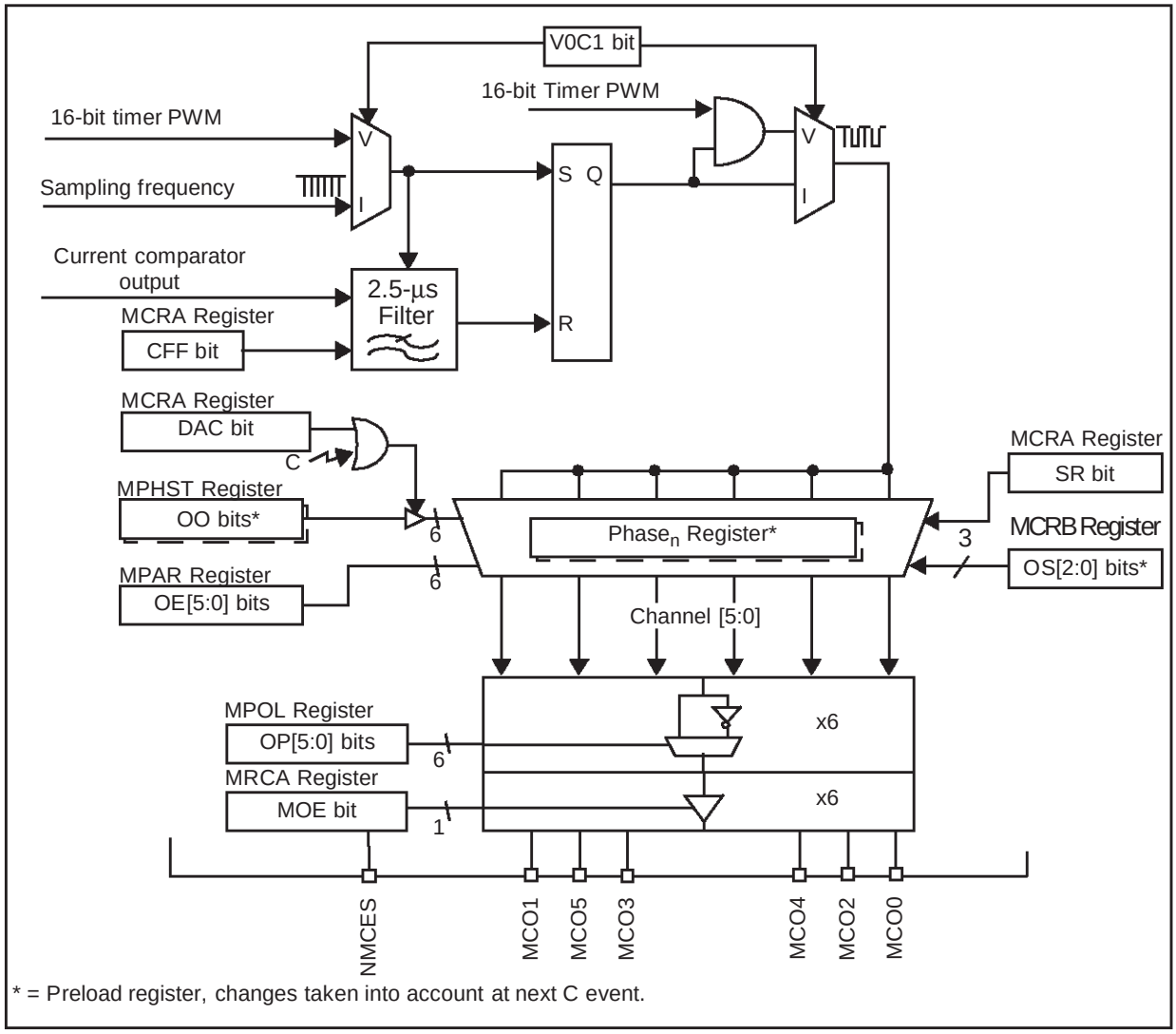
If there is an R- event, we need to accelerate the clock, so the ratio is decreased from 0101 to 0100.

In both case, this is automatically done by hardware.

We have to get the R event in the speed software regulation.

4 CHANNEL MANAGER

Figure 14. Channel manager part of the peripheral



* = Preload register, changes taken into account at next C event.

The MPHST register has a preload register and an active register.

The six channels can be divided into 2 groups in the MPAR register: Even channels and Odd channels. This is to be able to apply the PWM to different groups for detecting events.

The MPAR register allows you to choose the parity of the outputs. For example T1, T3, T5 are Odd and T2,T4,T6 are Even switches. This means that, depending on the event we are waiting for, the PWM signal can be applied on the Odd or Even switches (this is determined by the OS bits in the MCRB register). During the demagnetisation, the PWM signal is applied on the high side switch or on the low side switch depending on the step configuration. For the zero crossing event detection, PWM is always applied on the high side switch.

The MPOL register can be used to select the polarity of each of the outputs: 0 means that the output is active at low level, 1 means that the output is active at high level.

Table 3. Step behaviour summary

Mode		OS2 bit	PWM after C and before D	OS [1:0] bits	PWM after D and before C
Voltage mode(V0C1=0)	Sensorless (SR=0)	0	Not Alternate	00	On even channels
				01	On odd channels
				10	Alternate odd/even
				11	All active channels
		1	Alternate	00	On even channels
				01	On odd channels
				10	Alternate odd/even
				11	All active channels
	Sensor (SR=1)	x	Unused	00	On even channels
				01	On odd channels
				10	Alternate odd/even
				11	All active channels
Current mode (V0C1=1)	Sensorless (SR=0)	0	On even Channels	00	On even channels
				01	On odd channels
				10	Alternate odd/even
				11	All active channels
		1	On odd channels	00	On even channels
				01	On odd channels
				10	Alternate odd/even
				11	All active channels
	Sensor (SR=1)	x	Unused	00	On even channels
				01	On odd channels
				10	Alternate odd/even
				11	All active channels

Table 3 shows how the PWM signal can be applied to the switches depending on the event that has to be detected. For example in sensorless current mode, before the detection of the end of demagnetisation event, the PWM signal can be applied to the odd channels or the even channels to accelerate the demagnetisation (see application note AN1129). This depends on the edge of the end of demagnetisation event. For the zero crossing event detection, the PWM signal is applied to the even or odd channels, bearing in mind that the PWM signal is always applied to the high side switch to detect the zero crossing event.

APPENDIX 1: REGISTER DESCRIPTION

TIMER COUNTER REGISTER (MTIM)

Read Only
Reset Value: 0000 0000 (00h)

7							0
T7	T6	T5	T4	T3	T2	T1	T0

Bit 7:0 = **T[7:0]**: *MTIM Counter Value.*
These bits contain the current value of the 8-bit up counter.

CAPTURE Z_{n-1} REGISTER (MZPRV)

Read Only
Reset Value: 0000 0000 (00h)

7							0
ZP7	ZP6	ZP5	ZP4	ZP3	ZP2	ZP1	ZP0

Bit 7:0 = **ZP[7:0]**: *Previous Z Value.*
These bits contain the previous captured BEMF value (Z_{N-1}).

CAPTURE Z_n REGISTER (MZREG)

Read Only
Reset Value: 0000 0000 (00h)

7							0
ZC7	ZC6	ZC5	ZC4	ZC3	ZC2	ZC1	ZC0

Bit 7:0 = **ZC[7:0]**: *Current Z Value.*
These bits contain the current captured BEMF value (Z_N).

COMPARE C_{n+1} REGISTER (MCOMP)

Read/Write
Reset Value: 0000 0000 (00h)

7							0
DC7	DC6	DC5	DC4	DC3	DC2	DC1	DC0

Bit 7:0 = **DC[7:0]**: *Next Compare Value.*
These bits contain the compare value for the next commutation (C_{N+1}).

DEMAGNETIZATION REGISTER (MDREG)

Read/Write

Reset Value: 0000 0000 (00h)

7							0
DN7	DN6	DN5	DN4	DN3	DN2	DN1	DN0

Bit 7:0 = **DN[7:0]**: *D Value.*

These bits contain the compare value for software demagnetization (D_N) and the captured value for hardware demagnetization (D_H).

A_N WEIGHT REGISTER (MWGHT)

Read/Write

Reset Value: 0000 0000 (00h)

7							0
AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0

Bit 7:0 = **AN[7:0]**: *A Weight Value.*

These bits contain the A_N weight value for the multiplier. In auto-commutated mode the MCOMP register is automatically loaded with:

$$\frac{Z_n \times MWGHT}{32(d)} \quad \text{or} \quad \frac{Z_{N-1} \times MWGHT}{32(d)} \quad (*)$$

when a Z event occurs.

(*) depending on the DCB bit in the MCRA register.

PRESCALER & SAMPLING REGISTER (MPRSR)

Read/Write

Reset Value: 0000 0000 (00h)

7							0
SA3	SA2	SA1	SA0	ST3	ST2	ST1	ST0

Bit 7:4 = **SA[3:0]**: *Sampling Ratio.*

These bits contain the sampling ratio value for current mode.

Bit 3:0 = **ST[3:0]**: *Step Ratio.*

These bits contain the step ratio value. It acts as a prescaler for the MTIM timer and is auto incremented/decremented with each R+ or R- event.

INTERRUPT MASK REGISTER (MIMR)

Read/Write (except bits 7:6)

Reset Value: 0000 0000 (00h)

7							0
HST	CL	RIM	OIM	EIM	ZIM	DIM	CIM

Bit 7 = **HST**: *Hysteresis Comparator Value.*

This read only bit contains the hysteresis comparator output.

0: Demagnetisation/BEMF comparator is under V_{REF}

1: Demagnetisation/BEMF comparator is above V_{REF}

Bit 6 = **CL**: *Current Loop Comparator Value.*

This read only bit contains the current loop comparator output value.

0: Current sense voltage is under V_{CREF}

1: Current sense voltage is above V_{CREF}

Bit 5 = **RIM**: *Ratio update Interrupt Mask bit.*

0: Ratio update interrupts (R+ and R-) disabled

1: Ratio update interrupts (R+ and R-) enabled

Bit 4 = **OIM**: *Multiplier Overflow Interrupt Mask bit.*

0: Multiplier Overflow interrupt disabled

1: Multiplier Overflow interrupt enabled

Bit 3 = **EIM**: *Emergency stop Interrupt Mask bit.*

0: Emergency stop interrupt disabled

1: Emergency stop interrupt enabled

Bit 2 = **ZIM**: *Back EMF Zero-crossing Interrupt Mask bit.*

0: BEMF Zero-crossing Interrupt disabled

1: BEMF Zero-crossing Interrupt enabled

Bit 1 = **DIM**: *End of Demagnetization Interrupt Mask bit.*

0: End of Demagnetization interrupt disabled

1: End of Demagnetization interrupt enabled if the HDM or SDM bit in the MCRB register is set

Bit 0 = **CIM**: *Commutation Interrupt Mask bit*

0: Commutation Interrupt disabled

1: Commutation Interrupt enabled

INTERRUPT STATUS REGISTER (MISR)

Read/Write

Reset Value: 0000 0000 (00h)

7							0
0	RPI	RMI	OI	EI	ZI	DI	CI

Bit 7 = Reserved. Forced by hardware to 0.

Bit 6 = **RPI**: *Ratio Increment interrupt flag.*

Autoswitched mode (SWA bit =0)**:**

0: No R+ interrupt pending

1: R+ Interrupt pending

Switched mode (SWA bit =1)**:**

0: No R+ action

1: The hardware will increment the ST[3:0] bits when the next commutation occurs and shift all timer registers right.

Bit 5 = **RMI**: *Ratio Decrement interrupt flag.*

Autoswitched mode (SWA bit =0)**:**

0: No R- interrupt pending

1: R- Interrupt pending

Switched mode (SWA bit =1)**:**

0: No R- action

1: The hardware will decrement the ST[3:0] bits when the next commutation occurs and shift all timer registers left.

Bit 4 = **OI**: *Multiplier Overflow interrupt flag.*

0: No Multiplier Overflow interrupt pending

1: Multiplier Overflow interrupt pending

Bit 3 = **EI**: *Emergency stop Interrupt flag.*

0: No Emergency stop interrupt pending

1: Emergency stop interrupt pending

Bit 2 = **ZI**: *BEMF Zero-crossing interrupt flag.*

0: No BEMF Zero-crossing Interrupt pending

1: BEMF Zero-crossing Interrupt pending

Bit 1 = **DI**: *End of Demagnetization interrupt flag.*

0: No End of Demagnetization interrupt pending

1: End of Demagnetization interrupt pending

Bit 0 = **CI**: *Commutation interrupt flag*

0: No Commutation Interrupt pending

1: Commutation Interrupt pending

Table 4. Step Ratio Update

MOE bit	SWA bit	Clock State	Read	Ratio Increment (Slow Down)	Ratio Decrement (Speed-Up)
0	x	Disabled	Always possible	Write the ST[3:0] value directly in the MPRSR register	
1	0	Enabled		Set RPI bit in the MISR register **till** next commutation	Set RMI bit in the MISR register **till** next commutation
1	1	Enabled		Updated automatically according to MZREG value	

CONTROL REGISTER A (MCRA)

Read/Write

Reset Value: 0000 0000 (00h)

7							0
MOE	RST	SR	DAC	V0C1	SWA	CFF	DCB

Bit 7 = **MOE:** *Output Enable bit.*

0: Outputs and Clocks disabled

1: Outputs and Clocks enabled

MOE bit	MCO[5:0] Output pin State
0	Tristate
1	Output enabled

Bit 6 = **RST**: *Reset MTC registers.*

Software can set this bit to reset all MTC registers without resetting the ST7.

0: No MTC register reset

1: Reset all MTC registers

Bit 5 = **SR**: *Sensor ON/OFF.*

0: Sensorless mode

1: Sensor mode

Table 5. Sensor mode selection

SR bit	Mode	OS2 bit enable	Behaviour of the output PWM
0	Sensors not used	OS2 enabled	“Before D” behaviour & “after D” behaviour
1	Sensors used	OS2 disabled	Only “after D” behaviour

Bit 4 = **DAC**: *Direct Access to phase state register.*

0: No Direct Access (reset value). In this mode all the registers with a preload register are taken into account at the C event.

1: Direct Access enabled. In this mode, write a value in the MPHST register to access the outputs directly. All other registers with a preload register are taken into account at the same time.

Table 6. DAC bit meaning

MOE bit	DAC bit	Effect on Output	Effect on MTIM Timer
0	x	High Z	Clock disabled
1	0	Standard running mode	Standard running mode
1	1	MPHST register value (depending on MPOL register value)	Clock disabled

Bit 3 = **V0C1**: *Voltage/Current Mode*

0: Voltage Mode

1: Current Mode

Bit 2 = **SWA**: *Switched/Autoswitched Mode*

0: Switched Mode

1: Autoswitched Mode

Table 7. Switched and autoswitched modes

SWA bit	Commutation Type	MCOMP Register access
0	Switched mode	Read/Write
1	Autoswitched mode	Read only

Bit 1 = **CFF**: *Current Feedback Filter*

0: Current Feedback Filter disabled

1: Current Feedback Filter enabled

Bit 0 = **DCB**: *Data Capture bit*

0: Use MZPRV (Z_N-1) for multiplication

1: Use MZREG (Z_N) for multiplication

Table 8. Multiplier result

DCB bit	Commutation Delay
0	MCOMP = MWGHT x MZPRV / 32
1	MCOMP = MWGHT x MZREG / 32

CONTROL REGISTER B (MCRB)

Read/Write

Reset Value: 0000 0000 (00h)

7							0
VR1	VR0	CPB*	HDM*	SDM*	OS2*	OS1	OS0

Bit 7:6 = **VR[1:0]**: *BEMF/demagnetization Reference threshold*

These bits select the V_{REF} value as shown in the following table.

VR1	VR0	V_{REF} Voltage threshold
0	0	0.2V
0	1	0.6V
1	0	1.2V
1	1	2.5V

Bit 5 = **CPB***: *Compare Bit for Zero-crossing detection.*

0: Zero crossing detection on falling edge

1: Zero crossing detection on rising edge

Bit 4 = **HDM***: *Hardware Demagnetization event Mask bit*

0: Hardware Demagnetization disabled

1: Hardware Demagnetization enabled

Bit 3 = **SDM***: *Software Demagnetization event Mask bit*

0: Software Demagnetization disabled

1: Software Demagnetization enabled

Bit 2:0 = **OS2*,OS[1:0]**: *Operating output mode Selection bits*

These bits are used to configure the various PWM output configurations.

Note: The OS2 bit is the only one with a preload register.

Table 9. Step behaviour summary

Mode		OS2 bit	PWM after C and before D	OS [1:0] bits	PWM after D and before C
Voltage mode(V0C1=0)	Sensorless (SR=0)	0	Not Alternate	00	On even channels
				01	On odd channels
				10	Alternate odd/even
				11	All activechannels
		1	Alternate	00	On even channels
				01	On odd channels
				10	Alternate odd/even
				11	All active channels
	Sensor (SR=1)	x	Unused	00	On even channels
				01	On odd channels
				10	Alternate odd/even
				11	All active channels
Current mode (V0C1=1)	Sensorless (SR=0)	0	On even Channels	00	On even channels
				01	On odd channels
				10	Alternate odd/even
				11	All active channels
		1	On odd channels	00	On even channels
				01	On odd channels
				10	Alternate odd/even
				11	All active channels
	Sensor (SR=1)	x	Unused	00	On even channels
				01	On odd channels
				10	Alternate odd/even
				11	All active channels

* Preload bits, new value taken into account at next C event.

PHASE STATE REGISTER (MPHST)

Read/Write

Reset Value: 0000 0000 (00h)

7							0
IS1*	IS0*	OO5*	OO4*	OO3*	OO2*	OO1*	OO0*

Bit 7:6 = **IS[1:0]***: *Input Selection bits*

These bits select the input to connect to the comparator as shown in the following table:

Table 10. Input channel selection

IS1	IS0	Channel selected
0	0	MCIA
0	1	MCIB
1	0	MCIC
1	1	Not Used

Bit 5:0 =**OO[5:0]***: Channel On/Off bits

These bits are used to switch channels on/off at the next C event if the DAC bit =0 or directly if DAC=1

0: Channel Off, the relevant switch is OFF, no PWM possible

1: Channel On the relevant switch is ON, PWM is possible.

Table 11. OO[5:0] bit meaning

OO[5:0]	Output Channel State
0	Inactive
1	Active

* Preload bits, new value taken into account at next C event.

PARITY REGISTER (MPAR)

Read/Write

Reset Value: 0000 0000 (00h)

7							0
ZVD	REO	OE5	OE4	OE3	OE2	OE1	OE0

Bit 7 = **ZVD**: *Z vs D edge polarity.*

0: Zero-crossing and End of Demagnetisation have opposite edges

1: Zero-crossing and End of Demagnetisation have same edge

Bit 6 = **REO**: *Read on Even or Odd channel bit*

0: Read the BEMF signal during the off time on even channels

1: Read on odd channels

Bit 5:0 = **OE[5:0]**: *Output Parity Mode.*

0: Output channel is Even

1: Output channel Odd

POLARITY REGISTER (MPOL)

Read/Write

Reset Value: 0000 0000 (00h)

7							0
OT1	OT0	OP5	OP4	OP3	OP2	OP1	OP0

Bit 7:6 = **OT[1:0]**: *Off Time selection.*

These bits are used to select the off time in sensorless mode as shown in the following table.

Table 12. Off-Time bit Meaning

OT1	OT0	Off-Time Sensorless Mode (SR=0)	Off-Time Sensor Mode (SR=1)
0	0	5 µs	1.25 µs
0	1	10 µs	
1	0	15 µs	
1	1	30 µs	

Bit 5:0 = **OP[5:0]**: *Output channel polarity.*

These bits are used together with the OO[5:0] bits in the MPHST register to control the output channels.

0: Output channel is Active Low

1: Output channel is Active High

Table 13. Output Channel state control

OP[5:0] bit	OO[5:0] bit	MCO[5:0] pin
0	0	1 (Off)
0	1	0 (PWM possible)
1	0	0 (Off)
1	1	1 (PWM possible)

Note: The CPB, HDM, SDM, OS2 bits in the MCRB and the bits OE[5:0] are marked with *. This means that these bits are taken into account at the following commutation event (in normal mode) or when a value is written in the MPHST register when in direct access mode. For more details, refer to the description of the DAC bit in the MCRA register. The use of a Preload register allows all the registers to be updated at the same time.

Warning: Access to Preload registers

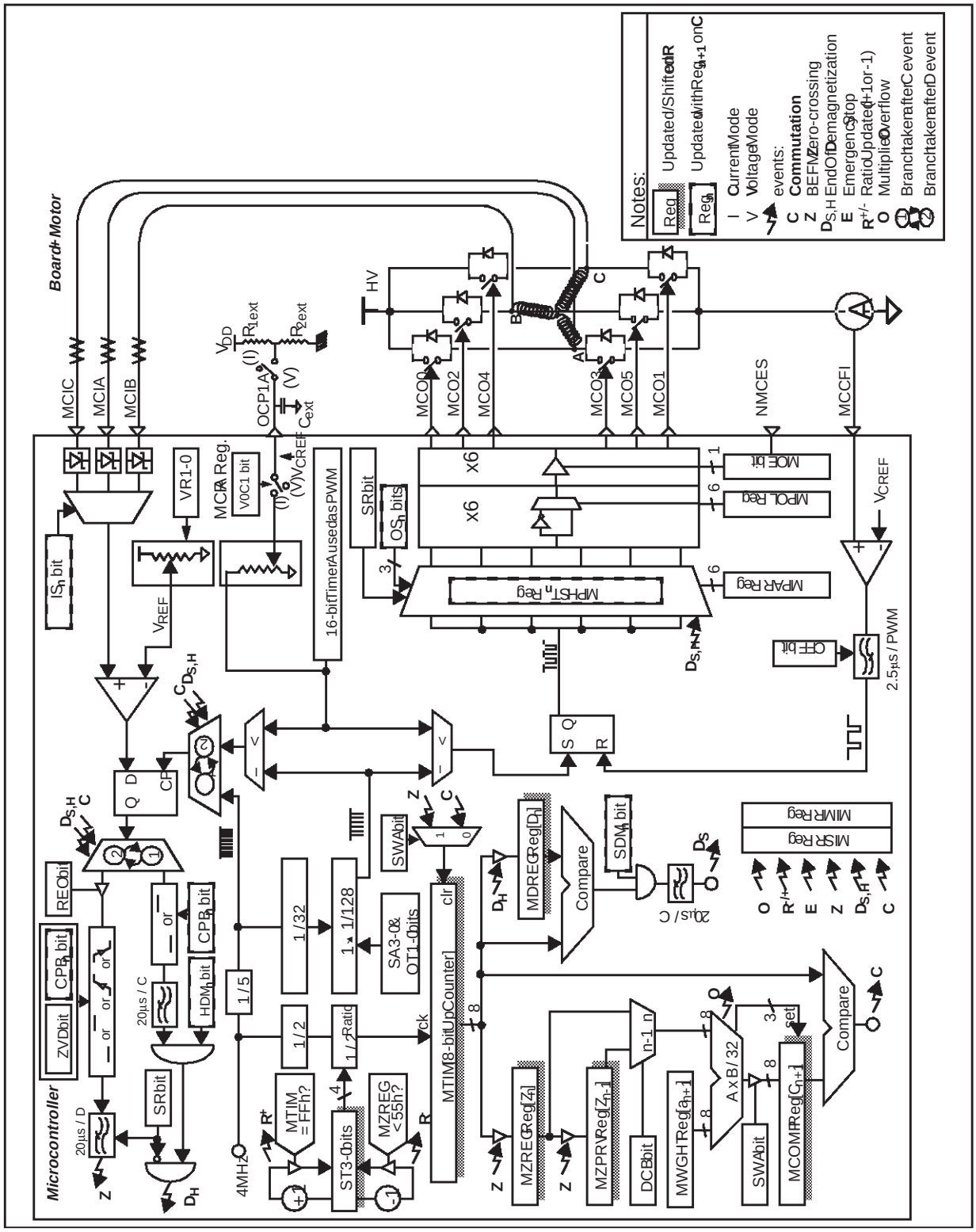
Special care has to be taken with Preload registers, especially when using the ST7 BSET and BRES instructions on MTC registers.

For instance, while writing to the MPHST register, you will write the value in the preload register. However, while reading at the same address, you will get the current value in the register and not the value of the preload register.

All preload registers are loaded in the real registers at the same time. In normal mode this is done automatically when a C event occurs, however in direct access mode (DAC bit=1) the preload registers are loaded as soon as a value is written in the MPHST register.

APPENDIX 2:

Figure 15. Detailed view of the MTC



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