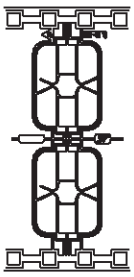
ST1305D

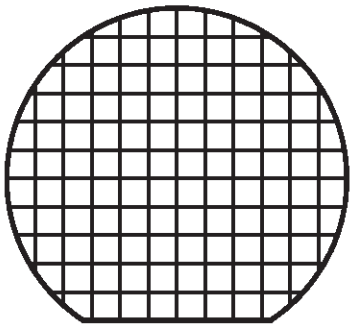
Memory Card IC 192 bit High Endurance EEPROM With Secure Logic Access Control and Inlock System

DATA BRIEFING

- 5 V Single Supply Voltage
- Memory Divided Into:
  - 16 bits of Circuit Identification
  - 48 bits of Card Identification
  - 48 bits of Count Data
  - 16 bits of Certificate
  - 24 bits of Transport Code
  - 64 bits of Issuer Data
- Counting Capability up to 262,144
- Circuit Protected by Transport Code for Delivery from ST to the Customer
- 5 External Contacts Only (ISO 7816 Compatible)
- Answer to Reset (Fully Compatible with ISO 7816-3)
- E.S.D. Protection Greater Than 4000 V
- Power-On and Low V_{CC} Reset
- Inlock system on RST input pin
- More than 300,000 Erase/Write Cycles
- More than 10 Years Data Retention
- 3.5 ms Programming Time (typical)



Micromodule (D15)



Wafer

DESCRIPTION

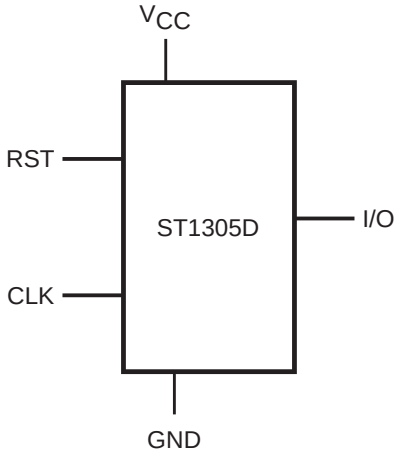
The ST1305D is a 192-bit EEPROM device with associated security logic to control memory access. The circuit includes counting capabilities and thus is very well adapted to prepaid card applications.

The ST1305D is protected by hard-wired security logic and special fuses. The memory is arranged

Table 1. Signal Names

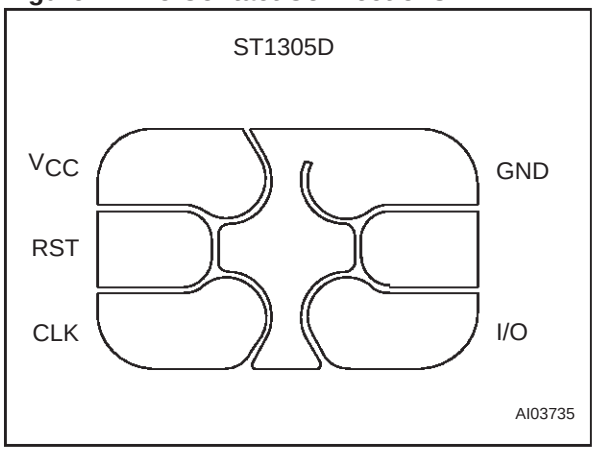
CLK	Clock
RST	Reset
I/O	Serial Data Input/Output
V_{CC}	Supply Voltage
GND	Ground

Figure 1. Logic Diagram



Complete data available under NDA.

Figure 2. D15 Contact Connections



as a matrix of 24x8 cells, accessed in a serial bit-wise fashion for reading and programming, and in a byte-wise fashion for internal erasing.

MODES

The device works in two distinct modes of operation:

– Issuer Mode: for the card manufacturer. allowing custom data to be written to the device, to initialize it before release to the end user.

– User Mode: for the end user of the card, with restricted, and controlled access to the device.

EXTERNAL COMMANDS

Four distinct commands can be composed using the external contacts:

– RESET: to reset the internal address counter to zero and to output the data on Serial Data Input/ Output (I/O)

– READ: to increment the internal address counter and, if authorised, to output the data bit on Serial Data Input/Output (I/O)

– COMPARE: to allow the presented code, on Serial Data Input/Output (I/O) in the Issuer Mode, to be compared against the internal transport code

– PROGRAM: to program the bit at the current address.

ADDRESS SPACE

The internal address space of the ST1305D is divided into several zones, as shown in Figure 3.

The Transport Code area is available in the Issuer Mode. In the User Mode, it becomes the Counter area.

Figure 3. Memory Map

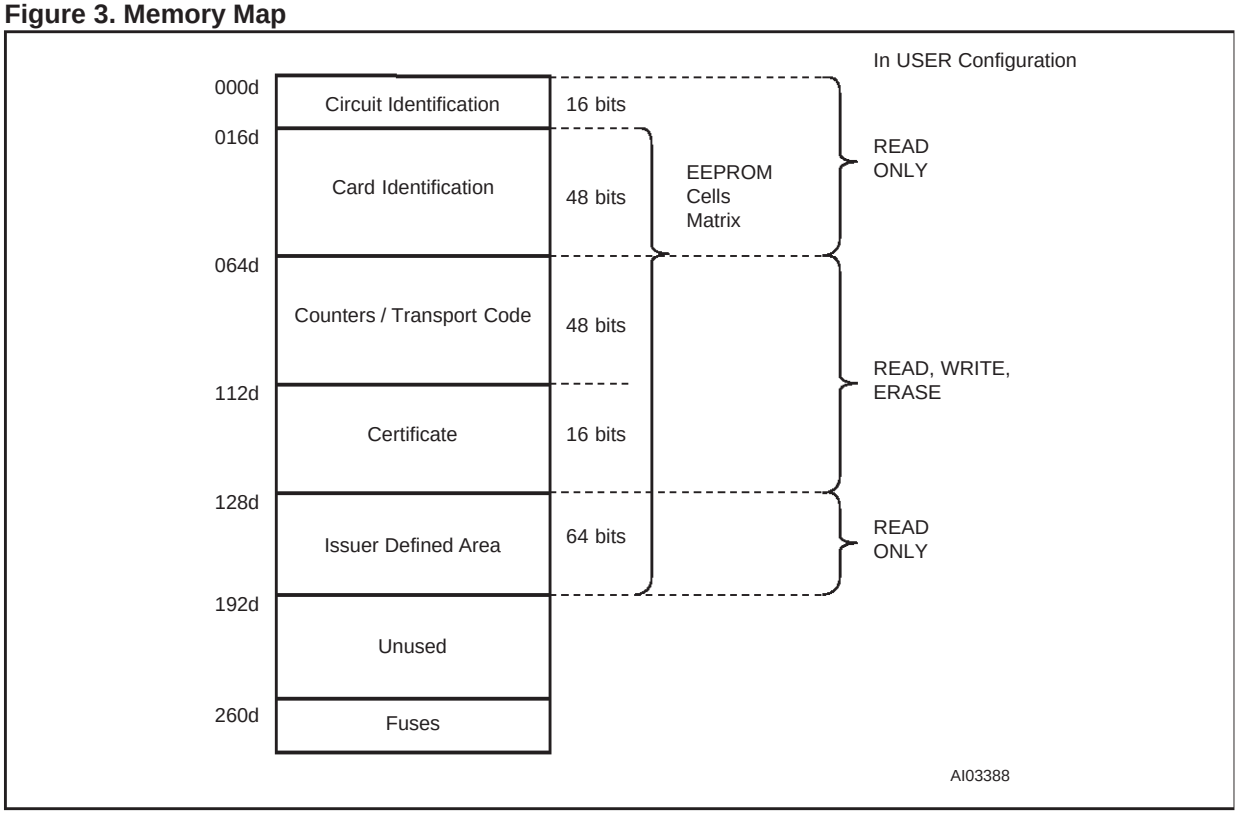
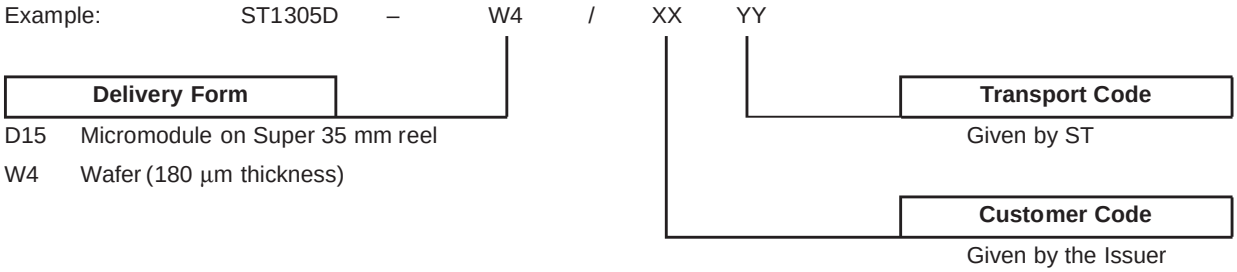


Table 2. Ordering Information Scheme



ORDERING INFORMATION

The notation used for the device number is as shown in Table 2. For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST Sales Office.