

**BU808DFP**

HIGH VOLTAGE FAST-SWITCHING NPN POWER DARLINGTON

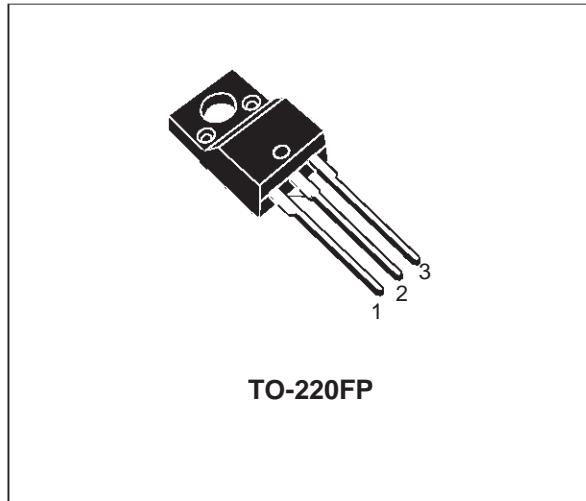
- STMicroelectronics PREFERRED SALES TYPE
- NPN MONOLITHIC DARLINGTON WITH INTEGRATED FREE-WHEELING DIODE
- HIGH VOLTAGE CAPABILITY (> 1400 V)
- HIGH DC CURRENT GAIN (TYP. 150)
- FULLY MOLDED ISOLATED PACKAGE 2KV DC ISOLATION (U.L. COMPLIANT)
- LOW BASE-DRIVE REQUIREMENTS
- DEDICATED APPLICATION NOTE AN1184

APPLICATIONS

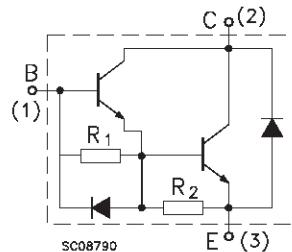
- COST EFFECTIVE SOLUTION FOR HORIZONTAL DEFLECTION IN LOW END TV UP TO 21 INCHES.

DESCRIPTION

The BU808DFP is a NPN transistor in monolithic Darlington configuration. It is manufactured using Multiepitaxial Mesa technology for cost-effective high performance.



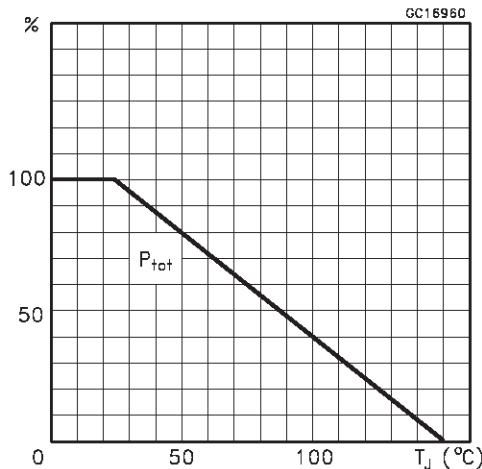
INTERNAL SCHEMATIC DIAGRAM



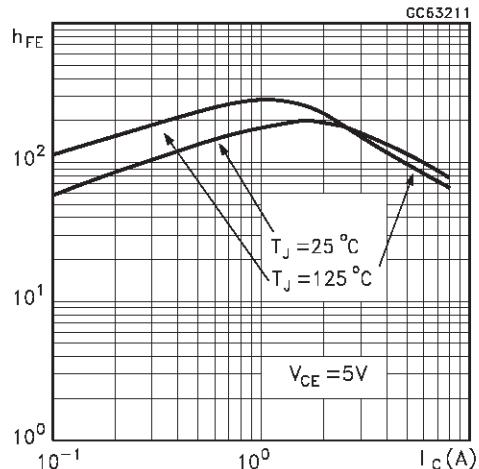
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CBO}	Collector-Base Voltage ($I_E = 0$)	1400	V
V_{CEO}	Collector-Emitter Voltage ($I_B = 0$)	700	V
V_{EBO}	Emitter-Base Voltage ($I_C = 0$)	5	V
I_C	Collector Current	8	A
I_{CM}	Collector Peak Current ($t_p < 5$ ms)	10	A
I_B	Base Current	3	A
I_{BM}	Base Peak Current ($t_p < 5$ ms)	6	A
P_{tot}	Total Dissipation at $T_c = 25$ °C	42	W
T_{stg}	Storage Temperature	-65 to 150	°C
T_j	Max. Operating Junction Temperature	150	°C

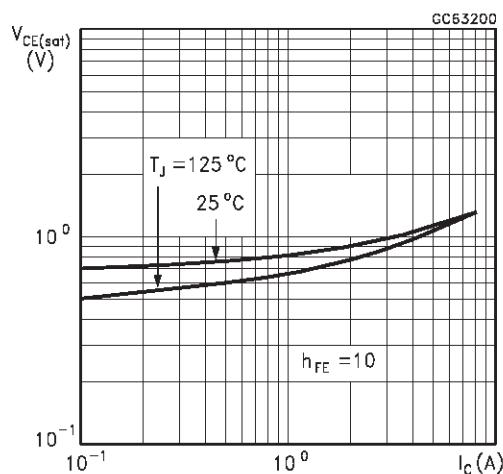
Derating Curve



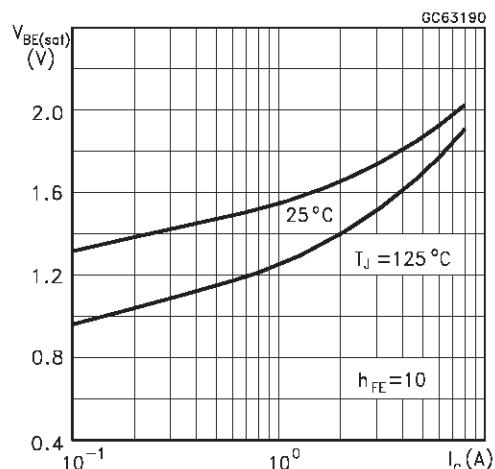
DC Current Gain



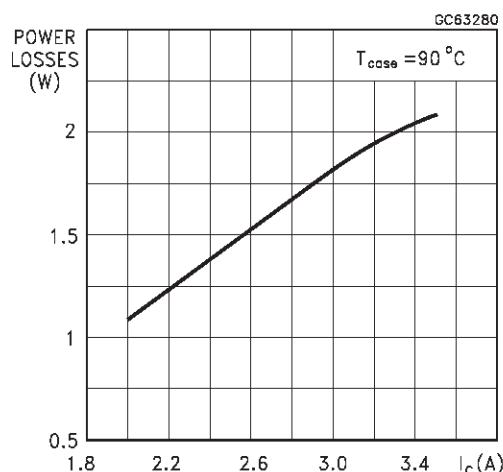
Collector Emitter Saturation Voltage



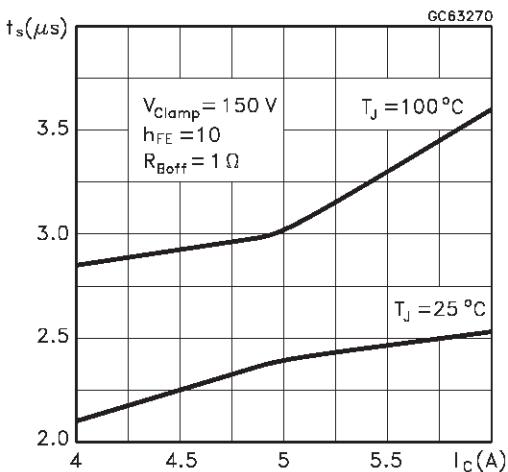
Base Emitter Saturation Voltage



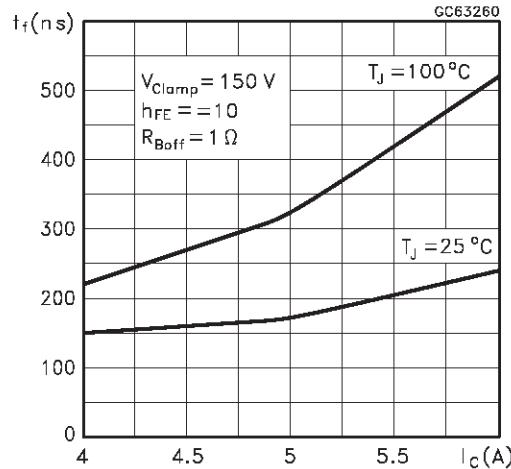
Power Losses at 16 KHz



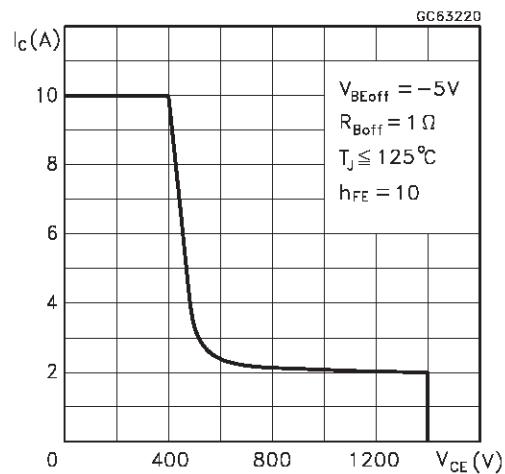
Switching Time Inductive Load at 16KHz



Switching Time Inductive Load at 16KHZ



Reverse Biased SOA



BASE DRIVE INFORMATION

In order to saturate the power switch and reduce conduction losses, adequate direct base current I_{B1} has to be provided for the lowest gain h_{FE} at 100°C (line scan phase). On the other hand, negative base current I_{B2} must be provided to turn off the power transistor (retrace phase).

Most of the dissipation, in the deflection application, occurs at switch-off. Therefore it is essential to determine the value of I_{B2} which minimizes power losses, fall time t_f and, consequently, T_j . A new set of curves have been defined to give total power losses, t_s and t_f as a function of I_{B2} at both 16 KHz scanning frequencies for choosing the optimum negative

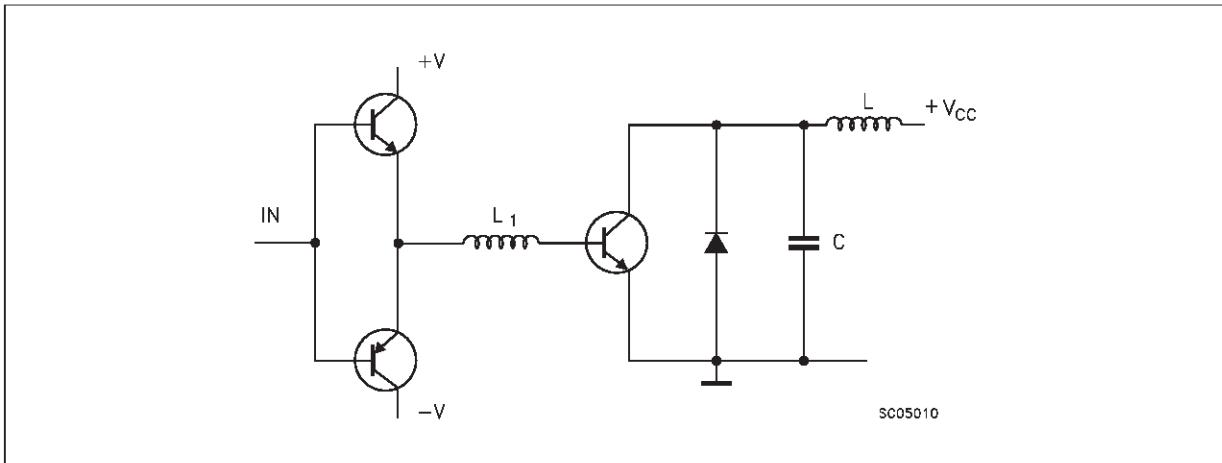
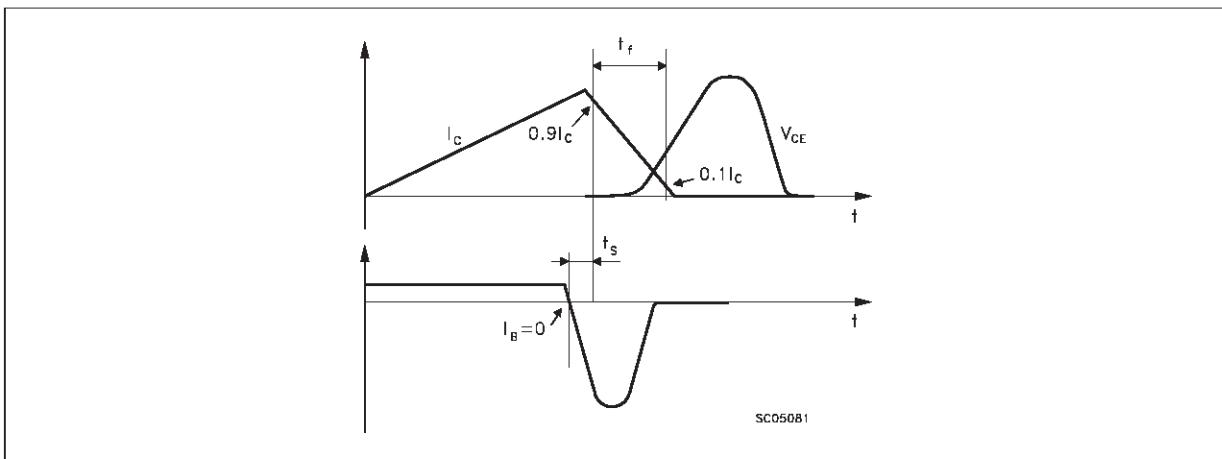
drive. The test circuit is illustrated in figure 1.

Inductance L_1 serves to control the slope of the negative base current I_{B2} to recombine the excess carrier in the collector when base current is still present, this would avoid any tailing phenomenon in the collector current.

The values of L and C are calculated from the following equations:

$$\frac{1}{2} L (I_c)^2 = \frac{1}{2} C (V_{CEfly})^2 \quad \omega = 2 \pi f = \frac{1}{\sqrt{LC}}$$

Where I_c = operating collector current, V_{CEfly} = flyback voltage, f = frequency of oscillation during retrace.

Figure 1: Inductive Load Switching Test Circuits.**Figure 2:** Switching Waveforms in a Deflection Circuit

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specification mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a trademark of STMicroelectronics

©2000 STMicroelectronics – Printed in Italy – All Rights Reserved
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco -
Singapore - Spain - Sweden - Switzerland - United Kingdom - U.S.A.

<http://www.st.com>

