



PD55015 - PD55015S

RF POWER TRANSISTORS

The LdmoST FAMILY

PRELIMINARY DATA

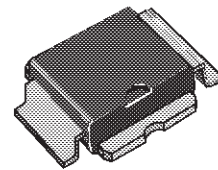
N-CHANNEL ENHANCEMENT-MODE LATERAL MOSFETs

- EXCELLENT THERMAL STABILITY
- COMMON SOURCE CONFIGURATION
- $P_{OUT} = 15\text{ W}$ with 14 dB gain @ 500 MHz / 12.5 V
- NEW RF PLASTIC PACKAGE

DESCRIPTION

The PD55015 is a common source N-Channel, enhancement-mode lateral Field-Effect RF power transistor. It is designed for high gain, broad band commercial and industrial applications. It operates at 12 V in common source mode at frequencies of up to 1 GHz. PD55015 boasts the excellent gain, linearity and reliability of ST's latest LDMOS technology mounted in the first true SMD plastic RF power package, PowerSO-10RF. PD55015's superior linearity performance makes it an ideal solution for car mobile radio.

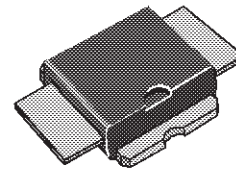
The PowerSO-10 plastic package, designed to offer high reliability, is the first ST JEDEC approved, high power SMD package. It has been specially optimized for RF needs and offers excellent RF performances and ease of assembly.



**PowerSO-10RF
(formed lead)**

ORDER CODE
PD55015

BRANDING
XPD55015



**PowerSO-10RF
(Straight lead)**

ORDER CODE
PD55015S

BRANDING
XPD55015S

ABSOLUTE MAXIMUM RATINGS ($T_{CASE} = 25^{\circ}\text{C}$)

Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$	Drain-Source Voltage	40	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Drain Current	5	A
P_{DISS}	Power Dissipation (@ $T_c = 70^{\circ}\text{C}$)	73	W
T_J	Max. Operating Junction Temperature	165	$^{\circ}\text{C}$
T_{STG}	Storage Temperature	-65 to +165	$^{\circ}\text{C}$

THERMAL DATA

$R_{th(j-c)}$	Junction -Case Thermal Resistance	1.3	$^{\circ}\text{C/W}$
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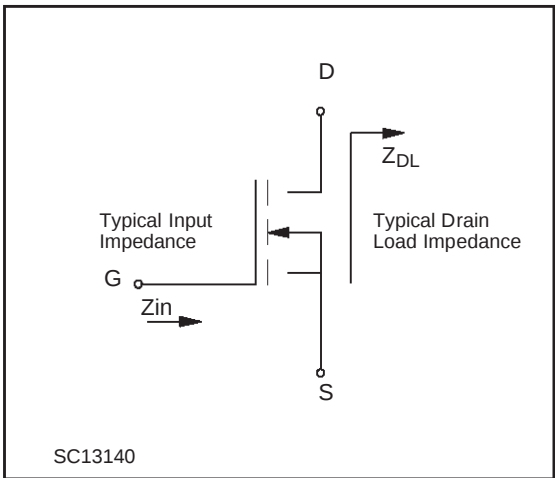
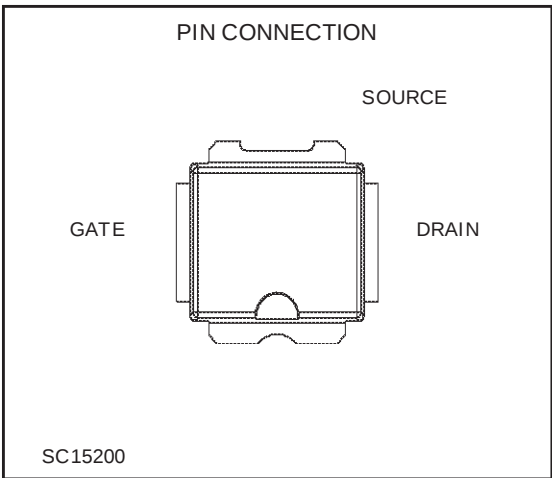
ELECTRICAL SPECIFICATION (T_{CASE} = 25°C)

STATIC

Symbol	Test Conditions		Min.	Typ.	Max.	Unit
I _{DSS}	V _{GS} = 0 V	V _{DS} = 28 V			1	μA
I _{GSS}	V _{GS} = 20 V	V _{DS} = 0 V			1	μA
V _{GS(Q)}	V _{DS} = 10 V	I _D = 150 mA	2.0		5.0	V
V _{DS(ON)}	V _{GS} = 10 V	I _D = 2.5 A			0.8	V
g _{FS}	V _{DS} = 10 V	I _D = 2.5 A	2.0	2.5		mho
C _{ISS}	V _{GS} = 0 V	V _{DS} = 12.5 V		89		pF
C _{OSS}	V _{GS} = 0 V	V _{DS} = 12.5 V		60		pF
C _{RSS}	V _{GS} = 0 V	V _{DS} = 12.5 V		6.5		pF

DYNAMIC

Symbol	Test Conditions		Min.	Typ.	Max.	Unit
P _{1dB}	V _{DD} = 12.5 V	I _{DQ} = 150 mA f = 500 MHz	15			W
G _P	V _{DD} = 12.5 V	I _{DQ} = 150 mA P _{OUT} = 15 W f = 500 MHz		14		dB
η _D	V _{DD} = 12.5 V	I _{DQ} = 150 mA P _{OUT} = 15 W f = 500 MHz		55		%
Load mismatch	V _{DD} = 15.5 V	I _{DQ} = 150 mA P _{OUT} = 15 W f = 500 MHz ALL PHASE ANGLES	20:1			VSWR



IMPEDANCE DATA

PD55015

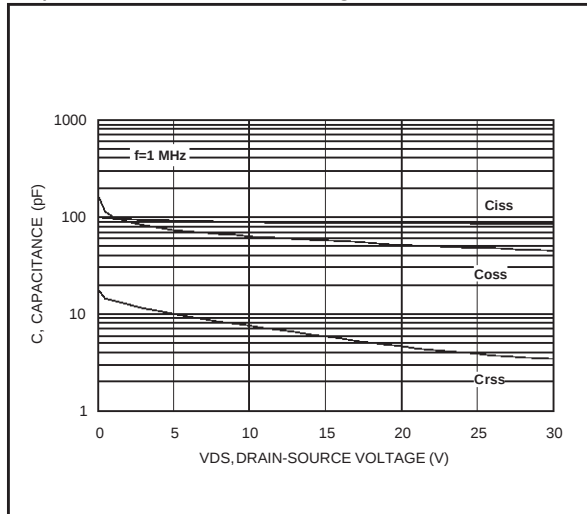
FREQ. MHz	Z _{IN} (Ω)	Z _{DL} (Ω)
480	1.58 + j .56	1.27 - j 1.36
500	1.53 + j .77	1.51 - j 1.81
520	1.70 + j 1.17	1.44 - j 2.13

PD55015S

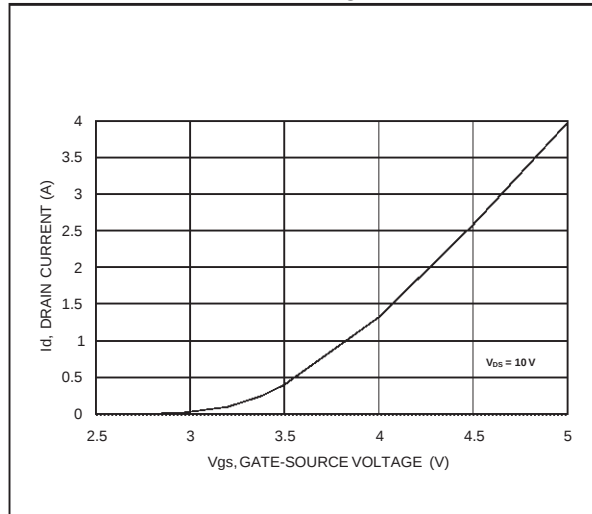
FREQ. MHz	Z _{IN} (Ω)	Z _{DL} (Ω)
480	1.30 - j .54	1.18 + j .04
500	1.26 - j .30	1.32 - j .22
520	1.34 - j .11	1.46 - j .22

TYPICAL PERFORMANCE

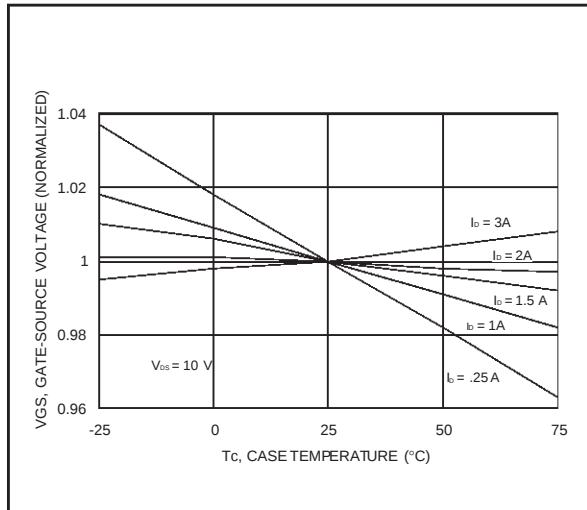
Capacitance vs. Drain Voltage



Drain Current vs. Gate Voltage



Gate-Source Voltage vs. Case Temperature

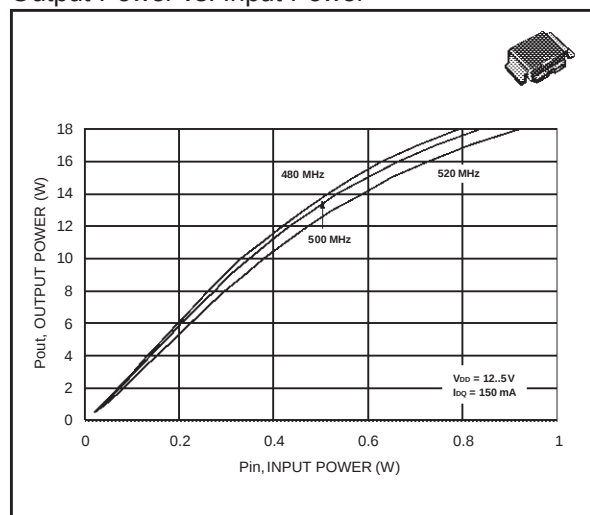


PD55015 - PD55015S

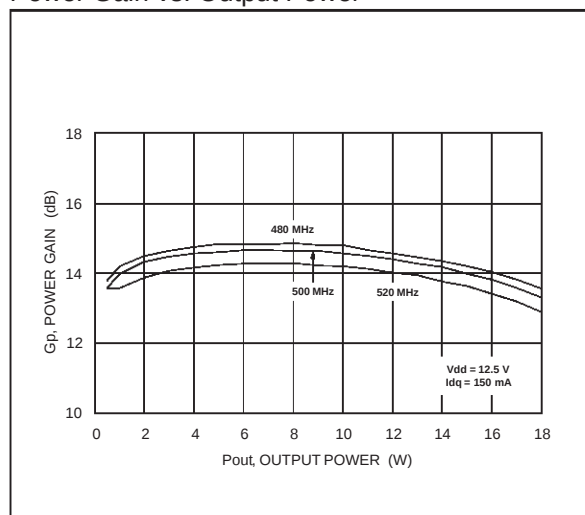
TYPICAL PERFORMANCE

Output Power vs. Input Power

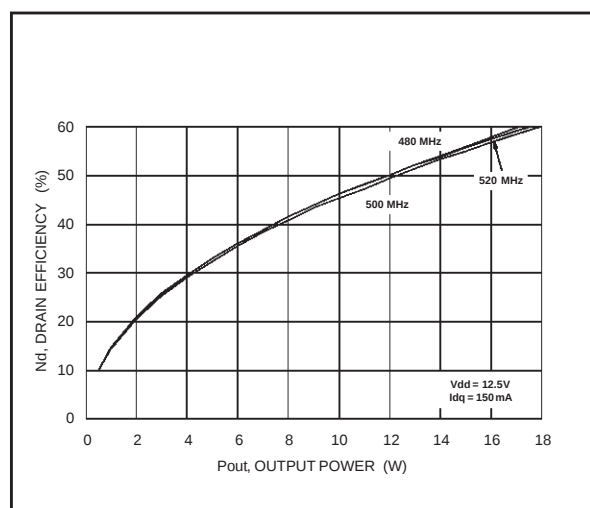
PD55015



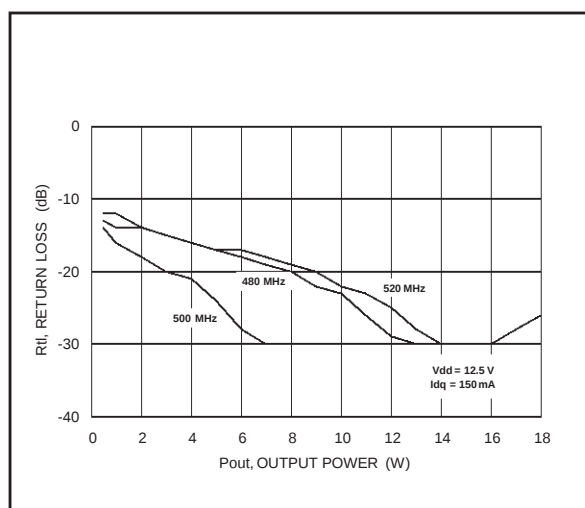
Power Gain vs. Output Power



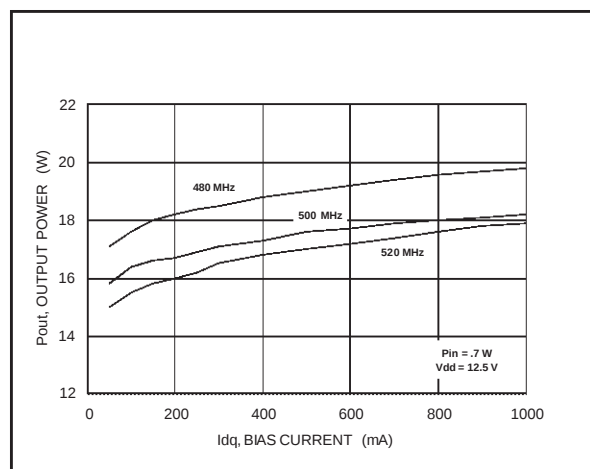
Drain Efficiency vs. Output Power



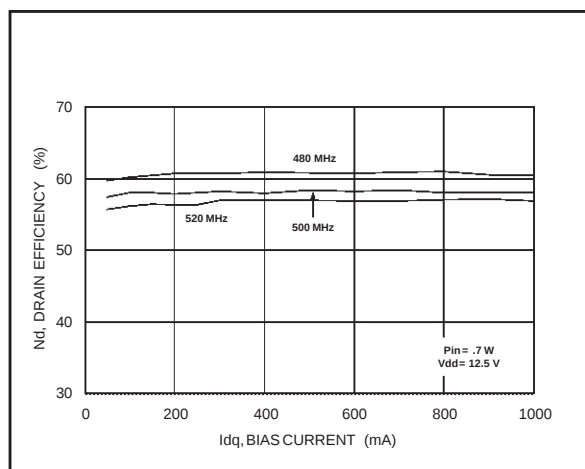
Return Loss vs. Output Power



Output Power vs. Bias Current

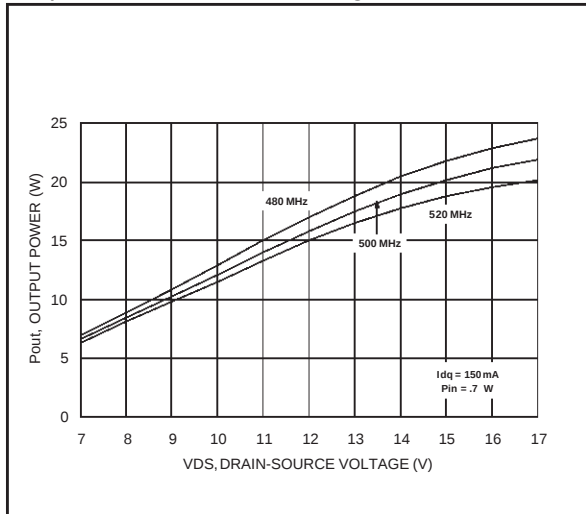


Drain Efficiency vs. Bias Current

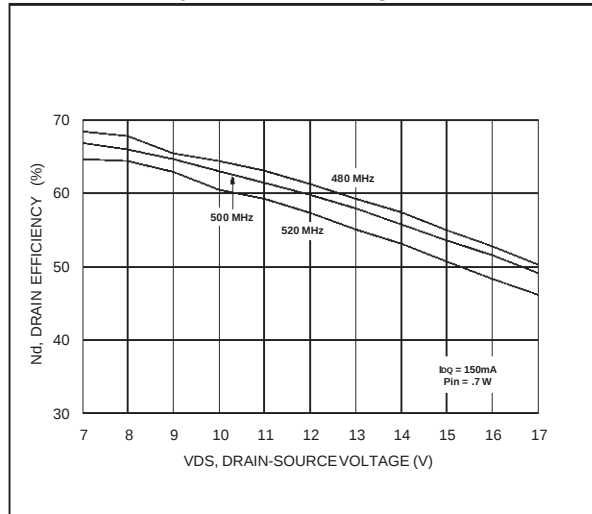


TYPICAL PERFORMANCE

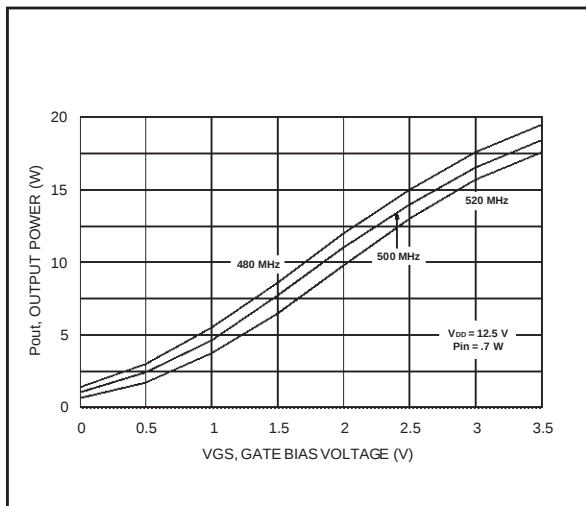
Output Power vs. Drain Voltage



Drain Efficiency vs. Drain Voltage

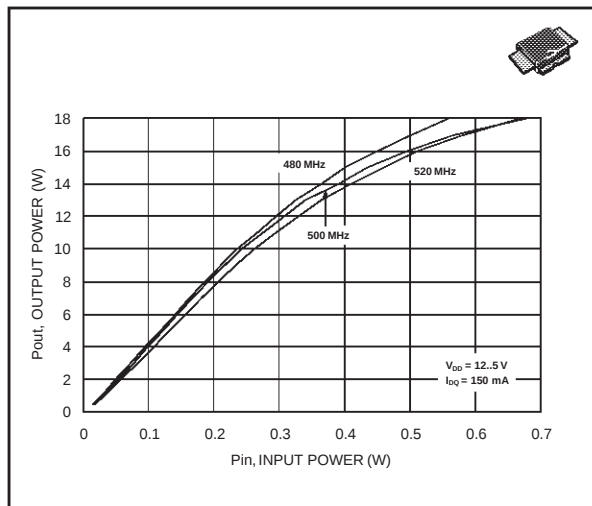


Output Power vs. Gate Bias Voltage

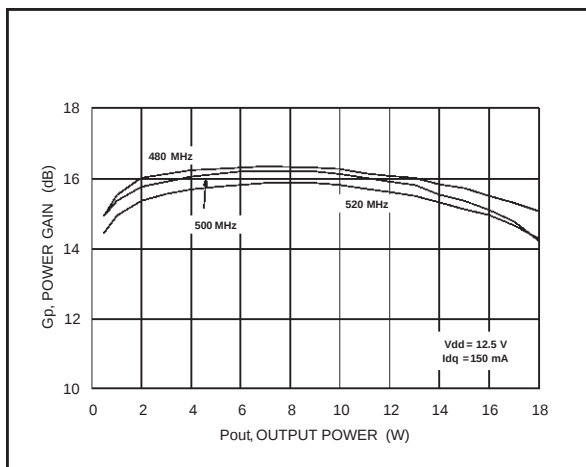


Output Power vs. Input Power

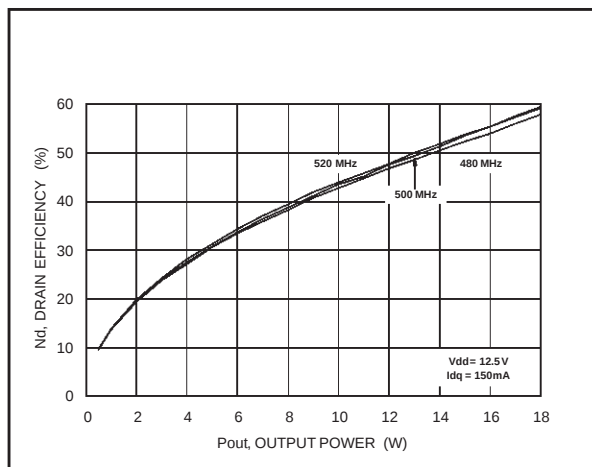
PD55015S



Power Gain vs. Output Power



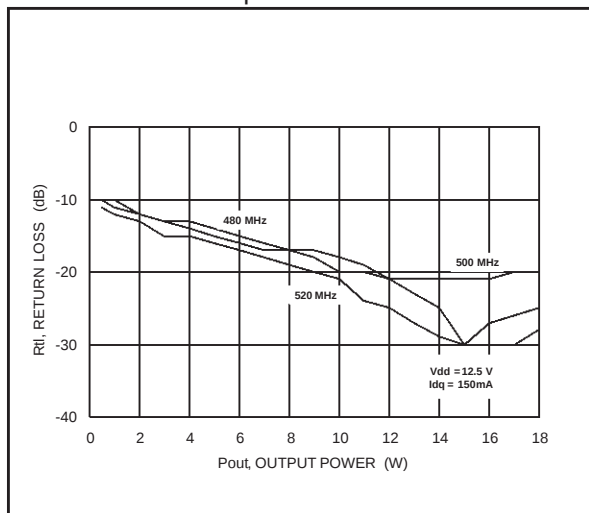
Drain Efficiency vs. Output Power



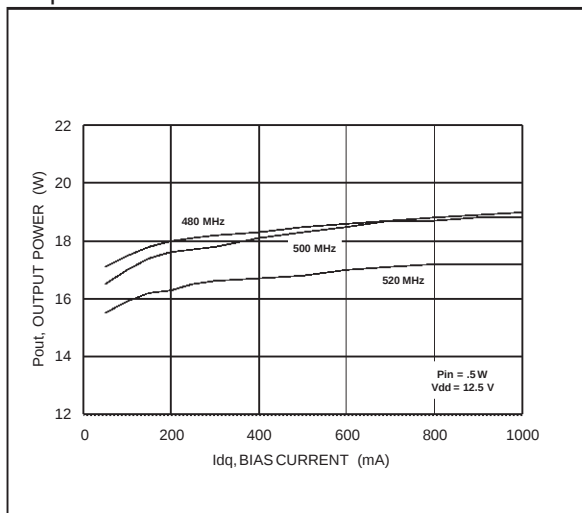
PD55015 - PD55015S

TYPICAL PERFORMANCE

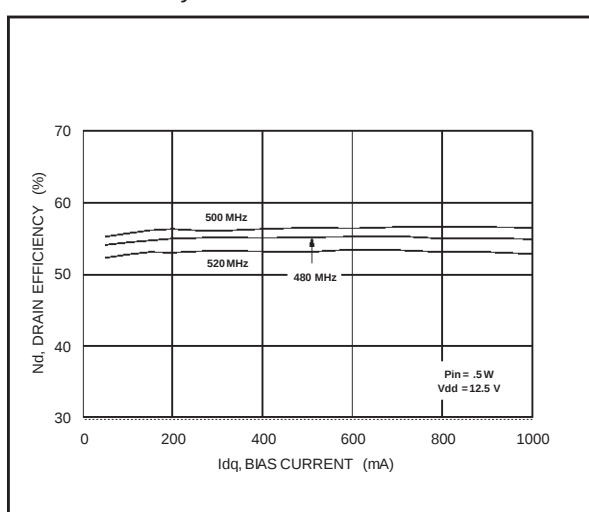
Return Loss vs. Output Power



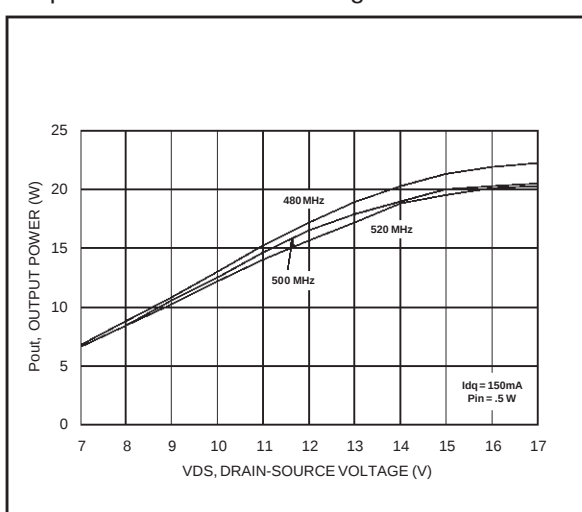
Output Power vs. Bias Current



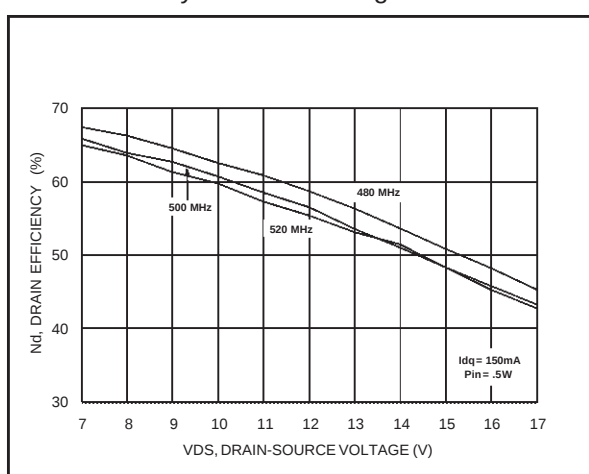
Drain Efficiency vs. Bias Current



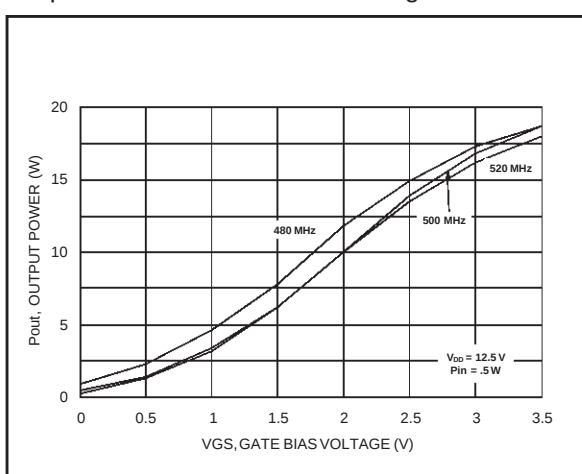
Output Power vs. Drain Voltage



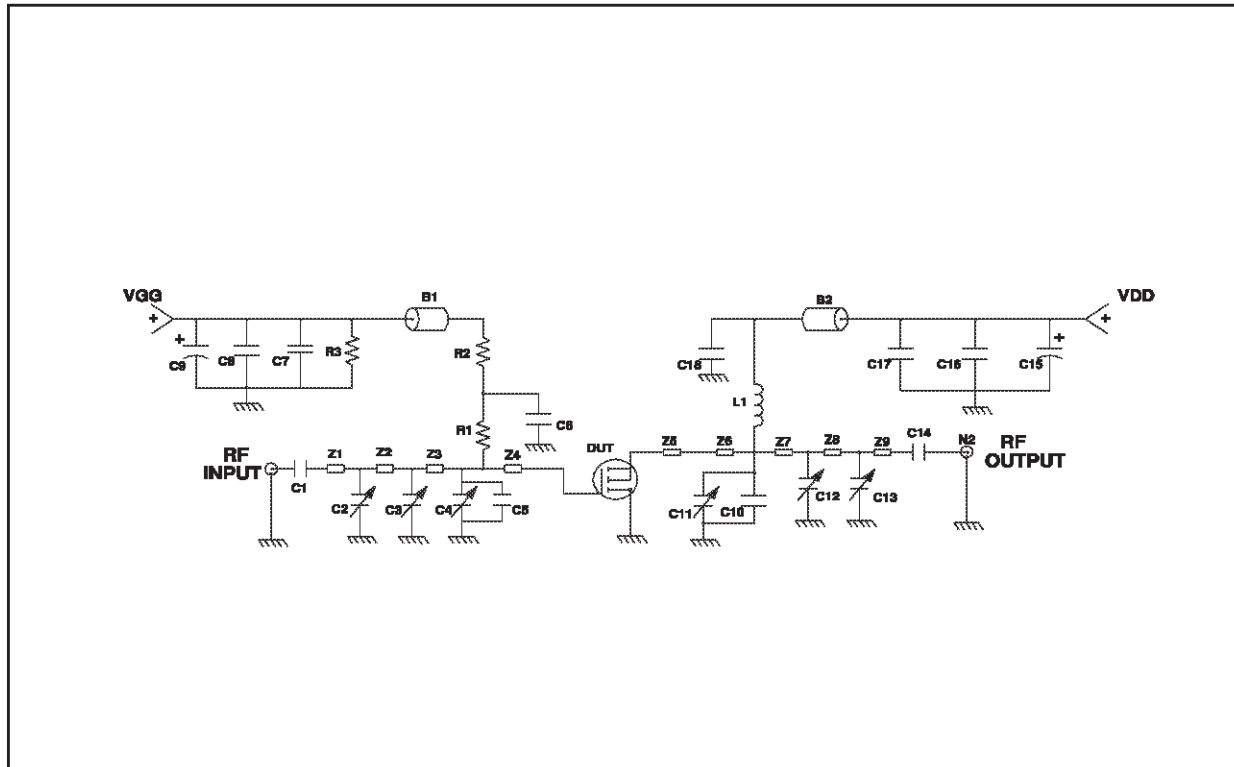
Drain Efficiency vs. Drain Voltage



Output Power vs. Gate Bias Voltage



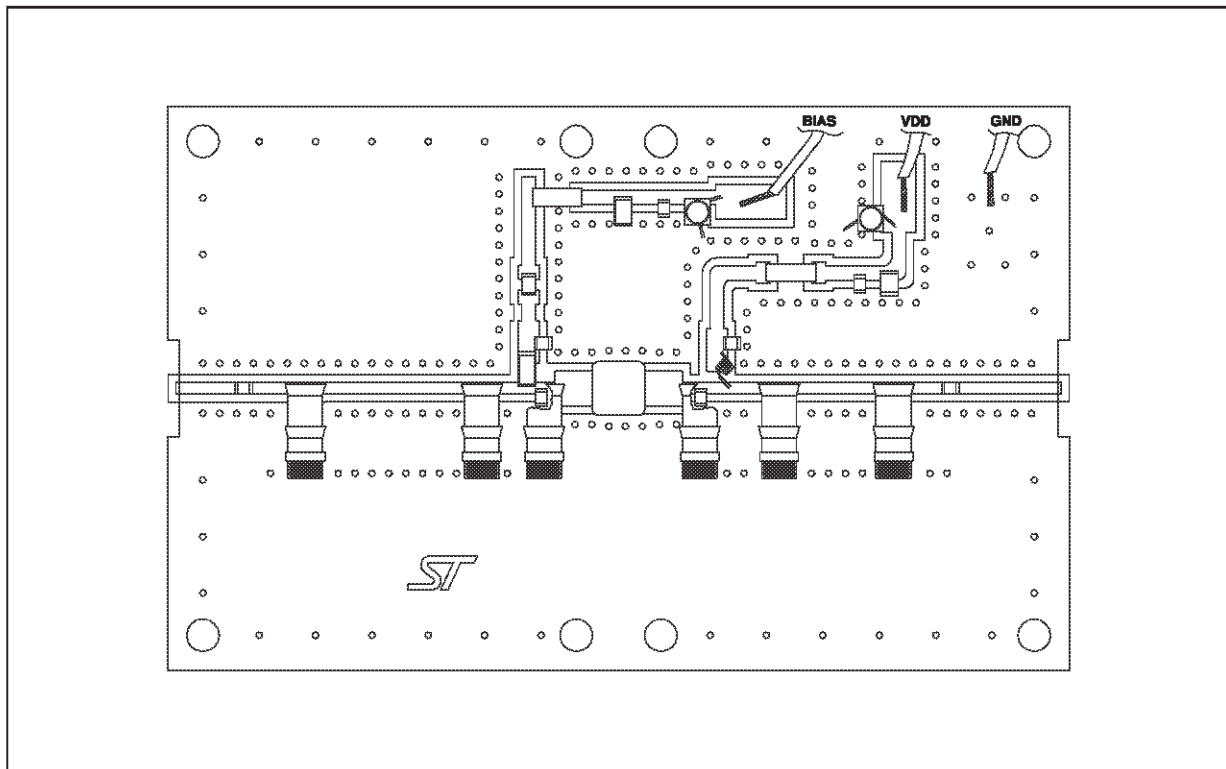
TEST CIRCUIT SCHEMATIC



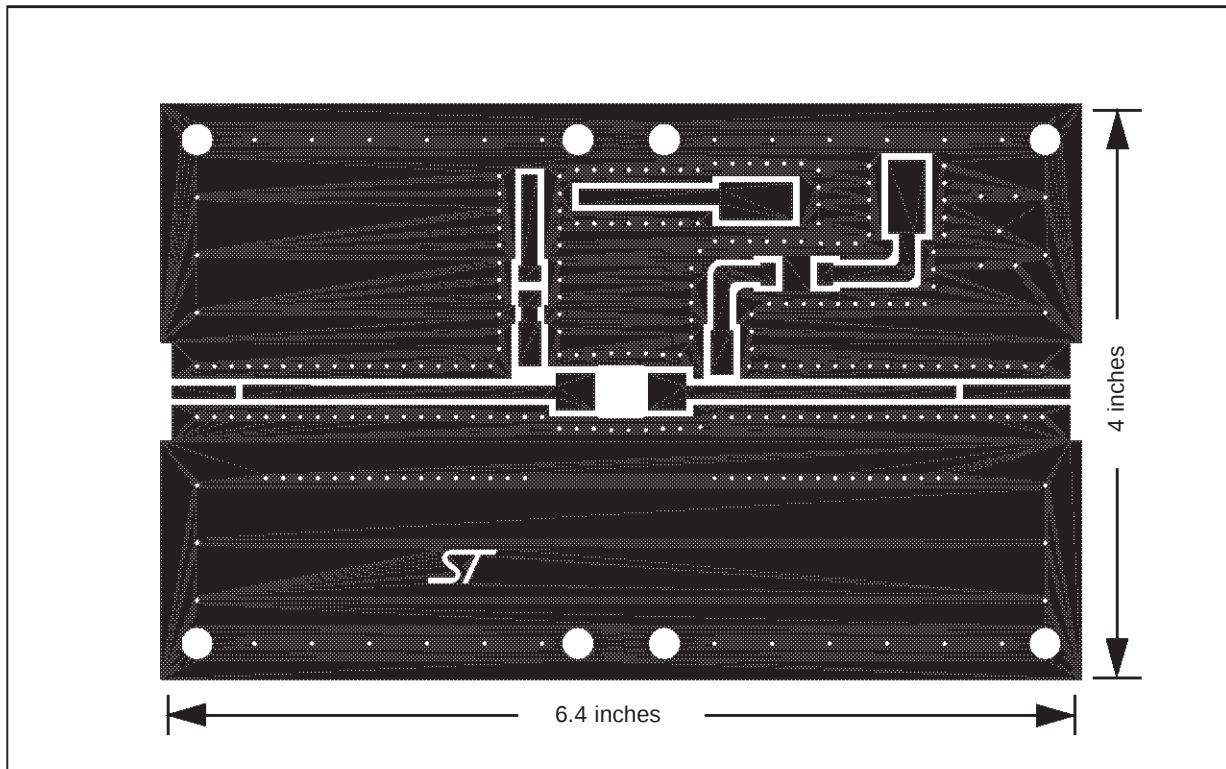
TEST CIRCUIT COMPONENT PART LIST

COMPONENT	DESCRIPTION
B1,B2	FERRITE BEAD
C1,C12	300 pF, 100 mil CHIP CAPACITOR
C2,C3,C4,C11,C12,C13	1 to 20 pF TRIMMER CAPACITOR
C6, C18	120 pF 100 mil CHIP CAPACITOR
C9, C15	10 μ F, 50 V ELECTROLYTIC CAPACITOR
C8, C16	0.1 mF, 100 mil CHIP CAP
C7, C17	1.000 pF 100 mil CHIP CAP
C5, C10	33 pF, 100 mil CHIP CAP
L1	56 nH, 7 TURN, COILCRAFT
N1, N2	TYPE N FLANGE MOUNT
R1	15 Ω , 1 W CHIP RESISTOR
R2	1 K Ω , 1 W CHIP RESISTOR
R3	33 K Ω , 1 W CHIP RESISTOR
Z1	0.471" X 0.080" MICROSTRIP
Z2	1.082" X 0.080" MICROSTRIP
Z3	0.372" X 0.080" MICROSTRIP
Z4,Z5	0.260" X 0.223" MICROSTRIP
Z6	0.050" X 0.080" MICROSTRIP
Z7	0.551" X 0.080" MICROSTRIP
Z8	0.825" X 0.080" MICROSTRIP
Z9	0.489" X 0.080" MICROSTRIP
BOARD	ROGER, ULTRA LAM 2000 THK 0.030", $\epsilon_r = 2.55$ 2oz. ED cu 2 SIDES.

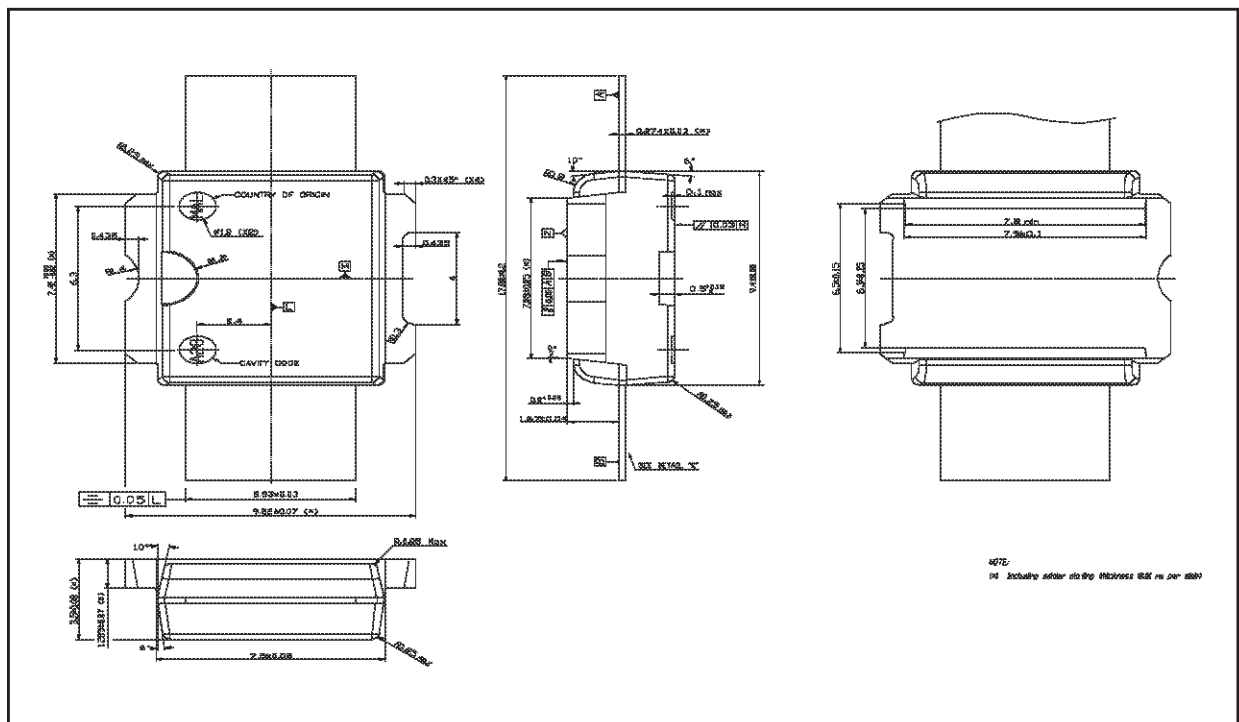
TEST CIRCUIT



TEST CIRCUIT PHOTOMASTER



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