APPLICATION NOTE

ST10F168 ST EMBEDDED ALGORITHM KERNEL (STEAK) FOR FLASH PROGRAMMING / ERASING

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1 - INTRODUCTION

This application note describes the ST EMBEDDED ALGORITHMS KERNEL (STEAK™), which eases the way to program and erase the on-chip Flash memory of the ST10F168 device.

In order to secure flash programming and erasing operations, and also to simplify the software development for programming and erasing the Flash, the ST10F168 Flash is programmed or erased by executing a specific sequence of instructions (called 'Unlock Sequence') with command and parameters loaded into GPRs.

The Unlock Sequence' invokes embedded kernel routines that checks the validity of the parameters provided by the user, and decodes the command (programming or erasing) and executes it.

When performing a programming command, the Embedded Algorithm Kernel automatically times the program pulse widths (taking in account the CPU period provided as a parameter by the user) and verifies proper cell programming.

When performing an erasing command, the Embedded Algorithm Kernel automatically preprograms the bank to be erased if it is not already programmed.

During erase, the Embedded Algorithm Kernel automatically times the erase pulse widths (taking in account the CPU period provided as a parameter by the user) and verifies proper cell erasing.

2 - CALLING STEAK ROUTINES

To start a program/erase operation, the user's application must call a STEAK routine.

As these routines are non-visible portion of code (written in a portion of Flash called Testflash, which is not mapped in the flash address area in normal operation mode of the device), the way to call these routines is performed by executing a specific instruction sequence, called 'Unlock Sequence'.

The 'Unlock Sequence' consists in two consecutive writes, the first with the direct addressing mode (MOV mem, Rwn) and the second with the indirect addressing mode (MOV [Rwm], Rwn), to an even address in the active address space of the Flash memory, and Rwn can be any unused word GPR (R6 to R15) loaded with a value resulting in the same even address than 'mem'.

Prior to invoke the STEAK, proper parameters must be assigned through R0-R4 registers.

The R0 register is the command register. Following registers handle the address and data to be programmed or sector to be erased.

A definition for these command sequences is given below:

Table 1 : Command - Parameters Definition

COMMAND	R0	R1	R2	R3	R4
Single Word programming	55Ash	AddOff	W	nu	2TCL
Double Word programming	DD4sh	AddOff	DWL	DWH	2TCL
Multiple (block) programming	AA5sh	BegAddOff	EndAddOff	SourceAddr	2TCL
Sector Erasing	EEEEh	5555h	Bnk	Bnk	2TCL
Set Flash Protection UPROG bit	CCCCh	5555h	3333h	AAAAh	2TCL
Read Status	7777h	nu	nu	nu	2TCL

Where:

s = Segment of the Target Flash Memory cell,

AddOff = Segment Offset of the Target Flash Memory cell. Must be even value (word-aligned),

W = Data (word) to be written in Flash,

DWL,DWH = Data (double word), DHL = low word, DWH = high word to be written in Flash,

BegAddOff = Segment Offset of the FIRST Target Flash Memory word to be written in a Multiple Word programming command. Must be even value (word-aligned),

EndAddOff = Segment Offset of the LAST Target Flash Memory word to be written in a Multiple Word programming command. Must be even value (word-aligned),
The value D = (EndAddOff - BegAddOff) must be:
2 <= D < 16384 (ie. up to one page (16K Bytes) can be written with one Multiple Word programming command).

SourceAdd = Start address for the source data (block) to be programmed. This address is using implicitly the data paging mechanism of the CPU. SourceAdd value must respect the following rules:
SourceAdd + (EndAddOff - BegAddOff) < 16384,
Page 0 and 1 can NOT be used for source data if bit ROMS1 = '1' (in SYSCON register),
Note that source data can be located in flash (In pages 0, 1, 6 to 19 if bit ROMS1 = '0',
or in pages 4, 5, 6 to 19 if bit ROMS1 = '1').

Bnk = Number of the Bank to be erased. Note that for security, R2 and R3 must hold the same value,

2TCL = CPU clock period in nseconds (eg. R4 = 50d means CPU frequency is 20MHz).

Note That big difference (1,5 time) between this value and the real CPU period may affect the flash reliability.

When the embedded programming/erasing algorithm returns to trigger point, information can be collected through register R0 so the user can take specific actions.

Table 2 : Error Code Definition (R0 content after STEAK execution)

ERROR CODE	MEANING
00h	Operation was successful
01h	Flash Protection is active
02h	Vpp voltage not present
03h	Programming operation failed
04h	Address value (R1) incorrect: not in Flash address area or odd
05h	CPU period out of range (must be between 30ns to 200ns)
06h	Not enough free space on system stack for proper operation
07h	Incorrect bank number (R2,R3) specified
08h	Erase operation failed (phase 1)
09h	Bad source address for Multiple Word programming command
0Ah	Bad number of words to be copied in Multiple Word programming command: one destination will be out of flash.
0Bh	PLL Unlocked or Oscillator watchdog overflow occured during programming or erasing the flash.
0Ch	Erase operation failed (phase 2)
FFh	Unknown or bad command

Return Values:

After a **Single or Double Word programming command**, R0 contains error code, R1 remains unchanged, R2 will contain the data in Flash for location Segment+Segment Offset (R0[3:0] with R1), R3 will contain the data in Flash for location Segment+Segment Offset +2 (R0[3:0] with R1+2), R4 to R15 remain unchanged.

After a **Multiple Word programming command**, R0 contains error code, R1 will contains the last segment offset address of the last written word in flash (failing flash address if R0 is not equal to zero), R2 and R3 are undefined, R4 to R15 remain unchanged..

After **erasing command**, only R4 to R15 remain unchanged, R0 will contain error code, R1 to R3 are undefined.

After **status read command**, R0 contains error code, R1 contains flash embedded revision (0100h for the revision 1.0 of STEAK - MSByte = major release, LSByte = minor revision), R2 and R3 contains circuit identifiers (R2 = #0787h and R3 = #0101h for this device), R4 to R15 remain unchanged.

Notes 1/ The Flash Embedded Algorithms require at least 50 words on the Internal System Stack for proper operation. The program verifies itself that there is enough free space on the System Stack before performing a programming or erasing operation. The MDH, MDL and MDC register content are modified.

2/ Once started, a programming or erasing sequence shall no be interrupted by voltage shutdown or reset. In such a case, the entire sequence (programming or erasing) shall be rerun.

3 - PROGRAMMING COMMANDS

There are 3 commands that allows to program the flash:

– Single word (16 bits) per STEAK call,
– Double word (32 bits) per STEAK call,
– Up to one page (16Kbytes) per STEAK call using implicit double word programming.

3.1 - Single Word Programming Routine

This routine is run when the Single Word Programming Command value (055Ash) is loaded in R0 register before executing the 'Unlock Sequence'.

The CPU execution will be derouted to the Embedded Kernel routine, and will perform the following actions:

– Return to user's application with R0 = 01 if the flash protection is enabled,
– Return to user's application with R0 = 05 if CPUPER parameter (value of R4 register) is > 200ns (F_{CPU} < 5MHz) or < 30ns (F_{CPU} > 33MHz),
– Return to user's application with R0 = 06 if there is NOT enough free words on System Stack for proper STEAK execution, i.e. if (SP - STKOV < 100 bytes),
– Save internally used registers on System Stack,
– Wait (~ 10µs) for internal stabilizing of Vpp voltage,
– Return to User's application with R0 = 02h if Vpp voltage is internally sensed < ~11 Volts,
– Return to User's application with R0 = 04 if address formed by R0 (segment address in the 4 least significant bits) and R1 (segment offset address) is NOT a word address (i.e. even value), or is NOT inside the address area of the flash (taking in account the current mapping of the Flash, for example if bit ROMS1 of SYSCON is set),
– Call of PRESTO programming algorithm.
– Return to User's application, with error code of PRESTO algorithm returned in register R0.

3.2 - Double Word Programming Routine

This routine is run when the Double Word Programming Command value (0DD4sh) value is loaded inside R0 register before executing the 'Unlock Sequence'.

The CPU execution will be derouted to the Embedded Kernel routine, and will perform the following actions:

– Return to user's application with R0 = 01 if the flash protection is enabled,
– Return to user's application with R0 = 05 if CPUPER parameter (value of R4 register) is > 200ns (F_{CPU} < 5MHz) or < 30ns (F_{CPU} > 33MHz),
– Return to user's application with R0 = 06 if there is NOT enough free words on System Stack for proper STEAK execution, i.e. if (SP - STKOV < 100 bytes),
– Save internally used registers on System Stack,
– Wait (~10µs) for internal stabilization of Vpp voltage,
– Return to User's application with R0 = 02h if Vpp voltage is internally sensed < ~11 Volts,
– Return to User's application with R0 = 04 if address formed by R0 (segment address in the 4 least significant bits) and R1 (segment offset address) is NOT a double word address (i.e. multiple of 4 value), or is NOT inside the address area of the flash (taking in account the current mapping of the Flash, for example of bit ROMS1 of SYSCON is set),
– Call of PRESTO programming algorithm.
– Return to User's application with error code of PRESTO algorithm returned in register R0.

3.3 - Multiple Word Programming Routine

This routine is run when the Multiple Word Programming Command value (0AA5sh) value is loaded inside R0 register before executing the 'Unlock Sequence'.

The CPU execution will be derouted to the Embedded Kernel routine, and will perform the following actions:

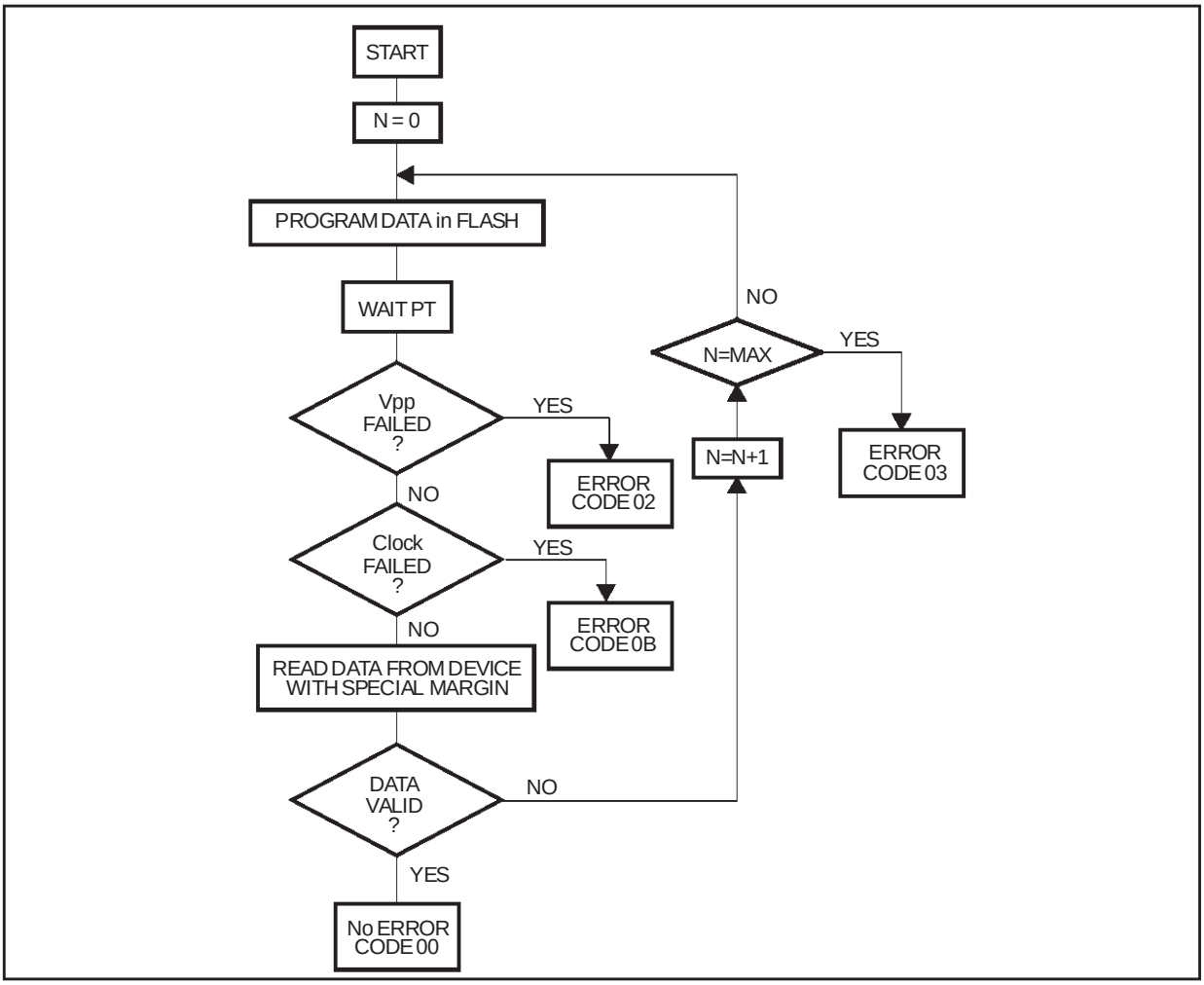
– Return to user's application with R0 = 01 if the flash protection is enabled,
– Return to user's application with R0 = 05 if CPUPER parameter (value of R4 register) is > 200ns (F_{CPU} < 5MHz) or < 30ns (F_{CPU} > 33MHz),
– Return to user's application with R0 = 06 if there is NOT enough free words on System Stack for proper STEAK execution, i.e. if (SP - STKOV < 100 bytes),
– Save internally used registers on System Stack,
– Wait (~10µs) for internal stabilization of Vpp voltage,
– Return to User's application with R0 = 02h if Vpp voltage is internally sensed < ~11 Volts,
– Return to User's application with R0 = 04 if first flash address to be programmed formed by R0 (segment address in the 4 least significant bits) and R1 (segment offset address) is NOT a word address (i.e. even value), or is NOT inside the address area of the flash (taking in account the current mapping of the Flash, for example if bit ROMS1 of SYSCON is set),

– Return to User's application with R0 = 04 if last flash address to be programmed formed by R0 (segment address in the 4 least significant bits) and R2 (segment offset address) is NOT a word address (i.e. even value), or is NOT inside the address area of the flash (taking in account the current mapping of the Flash, for example if bit ROMS1 of SYSCON is set),
– Return to User's application with R0 = 04 if last flash address to be programmed (in R2 register) is less than first address (in R1 register),
– Return to User's application with R0 = 0Ah if number of words to be programmed exceed a page size (8048 words, i.e. 16K Bytes),
– Return to User's application with R0 = 09h if source page offset (in R3 register) + 2* number of words to be programmed exceed the source page boundary,
– Return to User's application with R0 = 09h if source address is inside page 0 and 1 while the flash is mapped in segment 1,
– For the number of words to be programmed, call of PRESTO programming algorithm with data read at source address (in R3), destination is address defined by R0/R1 register then increment source address (R3) by 2, and destination address by 2 (R0/R1),
– If PRESTO programming algoritm returns an error, return to User's application, with error code of PRESTO algorithm returned in register R0, else program next word.

3.4 - PRESTO Programming Algorithm

All these 3 Kernel routines are using the same PRESTO programming algorithm to write and verify the flash in an efficient and reliable manner. The following flow-chart describes this PRESTO programming algorithm used by all 3 STEAK programming routines. This PRESTO programming algorithm can program a single word (16-bit value) or double word (32-bit value) data.

Figure 1 : PROGRAMMING Presto Algorithm



3.5 - Management of errors returned by STEAK Programming Commands

STEAK Programming Command routines are performing many checks and retries to try to program the data in flash. Thus, in many situations, when an error is repported by STEAK, it clearly means that the programming of the Flash can NOT be done. Here are a guide of what should be done when STEAK Programming commands return an error:

Error code 01 (flash protection is active):

– *Signification:* the Flash Protection is acitivated.

– *What can be done:* the flash can be 'temporary' unprotected by writing a zero at any even address in the active space of the Flash memory. This write must be done by an instruction executed from the internal Flash memory itself. For example:

```
MOV  FLASHM, ZEROS; Temporary unprotects the Flash.
                  ; FLASHM is any even address in Flash memory
                  ; space. This intruction MUST be executed from
                  ; Flash memory itself.
```

Error code 02 (Vpp failed):

– *Signification:* the internal Vpp voltage in the flash is not within the specifications. This fail can be due a glitch on Vpp (Vpp decoupling) a voltage drop (Vpp generator current capability) or static erroneous Vpp (generator out of specifications).

– *What can be done:* check Vpp and restart the sequence.

– *Note:* the on chip hardware is not suitable for detecting marginal variations outside the specifications. Vpp compliance to the ST10 specifications shall be guaranted by the Vpp generator characteristics.

Error code 03 (Programming failed):

– *Signification:* the PRESTO programming algorithm did not succeed in reading the correct data in flash after maximum number of programming retries. This error code covers two cases of programming failure:
- one bit (or more) must be programmed to "1" and the corresponding location(s) of the flash memory is "0",
- one bit (or more) must be programmed to "0" and the corresponding location(s) of the flash memory does not record any "0", it is locked to "1".

– *What can be done:* check the Vpp compliance to the specifications. Check the CPU period value entered en R4. User may then read the data (word, double word) at the address(es) that failed and compare it (them) with the data to be programmed.
- if the flash memory location(s) is(are) read as "0" while target data is "1", the default may be recovered. The flash memory must be erased again, at least the current bank, before to be programmed once more.
- if the flash memory location(s) is(are) read as "1" while target data is "0", the corresponding cell(s) may be damaged. A complete erasing/programming cycle may be tried.

Error code 04 (Address value incorrect: not in Flash address area or odd):

– *Signification:* the destination address, formed by the 4 low bits of R0 register (segment number) and R1 (16-bit offset address in segment) does not correspond to an address in Flash. This can come from a given address not consistant with flash memory mapping, i.e. trying to program a data in flash at the begining of segment 1 while the first 32 KByte of flash is mapped in segment 0.

– *What can be done:* the user's software can check the current memory mapping of the flash (test the setting of bit ROMS1 in SYSCON register), specially when trying to program address range 00'0000h to 00'7FFEh or 01'0000h to 01'7FFEh.Check the linker/locator setting of the tools chain to compare with the flash memory area.

Error code 05 (CPU period out of range: must be between 30ns and 200ns):

– *Signification:* the CPU period given in R4 is out of valid range. This parameter is requested by STEAK programming commands to set the duration of waiting loops inside the STEAK routines.

– *What can be done:* provide a valid value in R4 before calling STEAK command.

– *Note:* big difference between the value entered in R4 and the real CPU period overstresses the cells during programming and can lower the flash life.

Error code 06 (Not enough free space on system stack for proper operation):

– *Signification:* the STEAK programming routine needs at least 50 words on System Stack. Steak routine performs the following check:
if (SP - STKOV) < 100 then return error 06.

– *What can be done:* change the initialisation setting of SYSCON (bitfield STKSZ) to provide a bigger stack size, or flush the System Stack to external memory before calling STEAK programming command, and then restore it after STEAK return.

Error code 09 (Bad source address for Multiple Word programming command):

– *Signification:* the address of source data for a Multiple Word programming command (value in R3 register) is an odd address, or this address plus the number of bytes to be programmed exceed a page boundary, or this source address is inside page 0 or 1 while the flash is mapped in segment 1.

– *What can be done:* be sure that the following condition is true before calling STEAK Multiple Word programming command:
(R3 AND #03FFFh) + R2 -R1 < 04000h

Error code 0A (Bad number of words for Multiple Word programming command):

– *Signification:* the number of bytes to be programmed in a Multiple Word programming command exceed a page size (R2 - R1 >= #04000h).

– *What can be done:* be sure that the following condition is true before calling STEAK Multiple Word programming command:
R2 - R1 < 04000h

Error code 0B (PLL Unlock or Oscillator Watchdog Overflow occurred):

– *Signification:* PLL frequency is no more locked, or Oscillator Watchdog detected a missing input clock signal during a flash erasing or programming operation. This error is returned if XP3IR Interrupt flag is set.

– *What can be done:* reset the device (hardware reset or software bi-directional reset) for re-locking the PLL, erase the device (at least the current bank), and retry the programming.

Error code FF (Bad STEAK command):

– *Signification:* R0 content is not a valid command number.

– *What can be done:* be sure that R0 = #055Ash or #0DD4sh or #0AA5sh before calling STEAK programming routine.

3.6 - Single Word Programming using STEAK: code example

The following code is provided as an example to program a single word, check and react to error code returned by STEAK:

```
; code hereafter assumes that flash is mapped in segment 1
; ie. bit ROMS1 = ‘1’ in SYSCON register
; Flash must also be enabled, ie. bit ROMEN = ‘1’ in SYSCON.

PrgSgl:

MOV       R0, #055A0h     ; 55Axh : Single word programming command
OR        R0, #01h        ; Selects segment 1 in flash memory
MOV       R1, #00224h     ; Address to be programmed is 01’0224h
MOV       R2, #03456h     ; Data to be programmed at 01’0224h
MOV       R4, #050d       ; 50ns is 20MHz CPU clock frequency
MOV       R7, #08000h     ; R7 used for Flash trigger sequence
```

```
#define FCR 08000h
; Flash Unlock Sequence: consists in two consecutive writes, with the
direct addressing mode and then the indirect addressing mode. FCR must
represent an even address in the active address space of the Flash
memory, and Rwn can be any unused word GPR (R6 to R15)loaded with a
value resulting in the same even address than FCR
EXTS      #1, #2          ; flash can be mapped in segment 0 or 1
MOV       FCR, R7         ; first part
MOV       [R7], R7        ; second part
NOP                       ; WARNING: place 2 NOP operations after
NOP                       ; the Unlock sequence to avoid all possible
                          ; pipeline conflict in STEAK programs
CMP       R0, #0          ; Check error code returned by STEAK

JMP       cc_EQ, PrgDone  ; Programming OK!
CMP       R0, #1          ; Error Code = 01?
JMP       cc_NE, CkR02    ; No: next R0 check
; Flash is protected: to temporary unprotected it,
; a MOV FLASH_location, ZEROS instruction must be executed from
; the internal flash memory itself: refer to section 5 - Flash
; protection for more details.

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ChkR02:
CMP     R0, #2            ; Vpp failed.
JMP     cc_NE, CkR03
JMP     cc_UC, ErrorVpp   ; say that Vpp is failling.

ChkR03:
CMP     R0, #3            ; Error Code = 03?
JMP     cc_NE, ChkR04     ; No: next R0 check

                          ; Yes: Programming failed: we must check
                          ; the data versus flash content.
EXTS    #1, #1            ; read flash content using EXTended
MOV     R0, 0224h         ; instruction.
AND     R0, #03456h       ; Flash content is ANDed with data to be
                          ; programmed in flash.
CMP     R0, #03456h       ; If (Flash cont. AND Data) is NOT equal
                          ; to Data, then at least one bit of the
                          ; flash is at ‘0’ while it is at ‘1’ in the
JMP     cc_NE, EraseBnk   ; Data: Flash bank must be erased prior
JMP     cc_UC, FlashERL   ; else: the flash failed to be be
                          ; programmed (i.e. at least one bit in
                          ; Flash was not able to be programmed to
                          ; ‘0’): the flash part reached
                          ;  end of reliable lifetime
ChkR04:
```

```
CMP     R0, #4              ; Error Code = 04?
JMP     cc_NE, ChkR05       ; No: next R0 check
JMP     cc_UC, ErrorAd      ; Yes: say that address was not correct
ChkR05:
CMP     R0, #5              ; Error Code = 05?
JMP     cc_NE, ChkR06       ; No: next R0 check
JMP     cc_UC, ErrorCPUPER  ; Yes: say that CPU period was not
                            ; correct
ChkR06:
CMP     R0, #6              ; Error Code = 06?
JMP     cc_NE, ChkR0B       ; No: next R0 check
JMP     cc_UC, ErrorSysStk  ; Yes: say that not enough free
                            ; words on System Stack.
ChkR0B:
CMP     R0, #0B             ; Error Code = 0Bh?
JMP     cc_NE, ChkR0B       ; No: next R0 check
JMP     cc_UC, ErrorClock   ; Yes: say that a clock problem (PLL
                            ; unlocked or OWD overflow) occurred.
```

3.7 - Multiple Word Programming using STEAK: code example

The following code is provided as an example to program a block of data. Flash to be programmed is from address 01'9000h to 01'9FFEh (included). Source data (data to be copied into flash) is located in external RAM from address 05'1000h (to 05'1FFEh, implicitly):

```
; code hereafter assumes that flash is mapped in segment 1
; i.e. bit ROMS1 = '1' in SYSCON register
; Flash must also be enabled, i.e. bit ROMEN = '1' in SYSCON.
MOV     R0, #0AA50h     ; AA5xh: Multiple Word programming command
OR      R0, #01h        ; Selects segment 1 in flash memory
MOV     R1, #09000h     ; First Flash Segment Offset Address
MOV     R2, #09FFEh     ; Last Flash Segment Offset Address
MOV     R3, #09000h     ; Source data address: use DPP2 as
                        ; data page pointer
SCXT    DPP2,#014h      ; Source is in page 21 (014h): save previous
                        ; DPP2 value and load it with source page
                        ; number
MOV     R4, #050d       ; 50ns is 20MHz CPU clock frequency
MOV     R7, #08000h     ; R7 used for Flash trigger sequence
#define FCR 08000h
EXTS    #1, #2          ; flash can be mapped in segment 0 or 1
MOV     FCR, R7         ; first part
MOV     [R7], R7        ; second part
NOP                     ; WARNING: place 2 NOP operations after
NOP                     ; the Unlock sequence to avoid all possible
                        ; pipeline conflict in STEAK programs
POP     DPP2            ; restore DPP2
; Check R0 return value
(see previous example)
```

4 - ERASING COMMAND

The STEAK Erasing command allows to erase one sector (or bank) at a time, by executing the following automatically:

– First, program the whole bank with 0000h values for each words of the bank, using the same PRESTO programming algorithm than for STEAK programming commands,

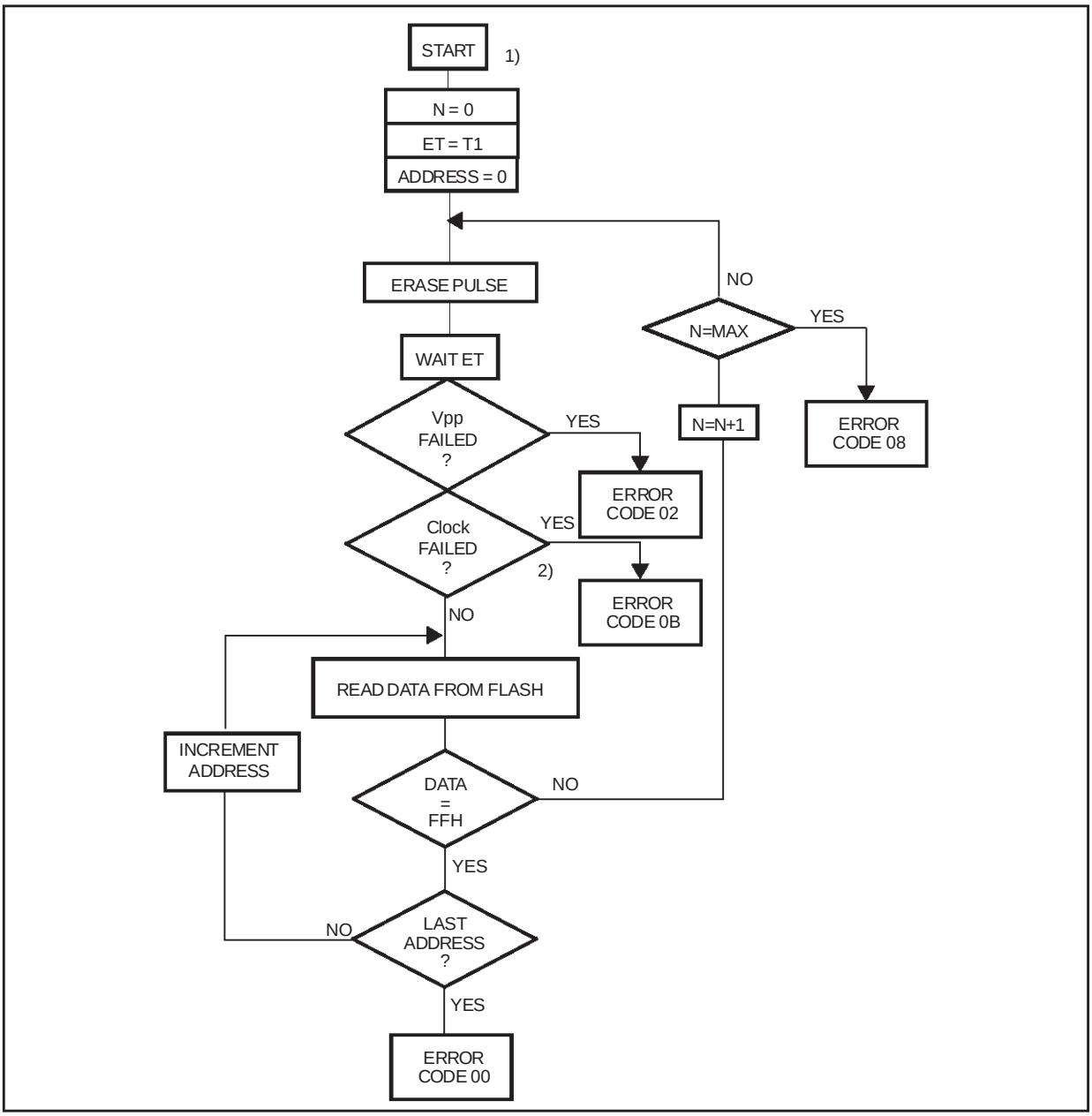
– Then, erase the bank by using the PRESTO Erase Algorithm.

4.1 - PRESTO Erasing Algorithm

The following flow-chart describes the PRESTO Erasing algorithm used by the STEAK erasing routine.

The whole bank must be previously programmed (i.e. all words in the bank must contains 0000h data): this is automatically done by the Steak erasing routine.

Figure 2 : ERASE Presto Algorithm



Notes 1. All words of the bank have been programmed (to 0000H) before starting PRESTO erase algorithm.

2. Clock failed if bit XP3IR is set.

4.2 - Management of error returned by STEAK Erasing Command

STEAK Erasing Command routine is performing many checks and retries write and then erase a bank of the flash memory. Thus, in many situations, when an error is returned by STEAK, it clearly means that the erasing of the Flash can NOT be done. Here is a guide of what should be done when STEAK Erasing command returns an error:

Error code 01 (flash protection is active):

– *Signification:* the Flash Protection is active.

– *What can be done:* the flash can be 'temporary' unprotected by writing a zero at any even address in the active space of the Flash memory. This write must be done by an instruction executed from the internal Flash memory itself. For example:

```
MOV   FLASHM, ZEROS   ; Temporary unprotect the Flash.
                      ; FLASHM is any even address in Flash memory
                      ; space. This instruction MUST be executed from
                      ; Flash memory itself.
```

Error code 02 (Vpp failed):

– *Signification:* the internal Vpp voltage in the flash is not within the specifications. This fail can be due a glitch on Vpp (Vpp decoupling) a voltage drop (Vpp generator current capability) or static erroneous Vpp (generator out of specifications).

– *What can be done:* check Vpp and restart the sequence.

– *Note:* the on chip hardware is not suitable for detecting marginal variations outside the specifications. Vpp compliance to the ST10 specifications shall be guaranted by the Vpp generator characteristics.

Error code 03 (Programming failed):

– *Signification:* the PRESTO programming algorithm did not succeed in programming the whole bank with zeros data after maximum number of programming retries.

– *What can be done:* check the Vpp static and dynamic values compliance with the specifications. Check the CPU period entered in R4. The user may then restart the erasing sequence.

Error code 05 (CPU period out of range : must be between 30ns and 200ns):

– *Signification:* the CPU period given in R4 is out of valid range. This parameter is requested by STEAK programming commands to to set the duration of waiting loops inside the STEAK routines.

– *What can be done:* provide a valid value in R4 before calling STEAK command.

– *Note:* big difference between the value entered in R4 and the real CPU period overstresses the cells during programming and can lower the flash life.

Error code 06 (Not enough free space on system stack for proper operation):

– *Signification:* the STEAK erasing routine needs at least 50 words on System Stack. STEAK routine performs the following check: if (SP - STKOV) < 100 then return error 06.

– *What can be done:* change the initialisation setting of SYSCON (bitfield STKSZ) to provide a bigger stack size, or flush the System Stack to external memory before calling STEAK erasing command, and then restore it after STEAK return.

Error code 07 (Incorrect Bank number specified):

– *Signification:* the content bank number specified in R2 and R3 register is not equal to 0,1,2 or 3.

– *What can be done:* be sure that R2=R3=0,1,2 or 3 before calling STEAK erasing routine.

Error code 08 or 0C (Erasing failed):

– *Signification:* the PRESTO erasing algorithm did not succeed in erasing the whole bank after maximum number of erasing retries.

– *What can be done:* check the Vpp static and dynamic values compliance with the specifications. Check the CPU period entered in R4. Restart then the sequence. If the error remains the flash part may have reached end of reliable lifetime: change the device.

Error code 0B (PLL Unlock or Oscillator Watchdog Overflow occurred):

– *Signification:* PLL frequency is no more locked, or Oscillator Watchdog detected a missing input clock signal during a flash erasing or programming operation. This error is returned if XP3IR Interrupt flag is set.

– *What can be done:* reset the device (hardware reset or software bi-directional reset) for re-locking the PLL, and retry the erasing command.

Error code FF (Bad STEAK command):

– *Signification:* the content of R2 register is not equal to the content of R3 register, or the content of R1 register is not equal to #05555h, or R0 content is not a valid command number.

– *What can be done:* be sure that R2=R3, R1 = #05555h and R0 = #0EEEEh before calling STEAK erasing routine.

4.3 - Bank Erasing using STEAK: code example

The following code is provided as an example to erase a bank of the flash. Flash content can be undefined before calling the STEAK Erasing Command:

```
; code hereafter assumes that flash is mapped in segment 1
; i.e. bit ROMS1 = ‘1’ in SYSCON register
; Flash must also be enabled, i.e. bit ROMEN = ‘1’ in SYSCON.

EraseBnk:

MOV   R0, #0EEEEh     ; EEEEh: Bank Erasing command
MOV   R1, #05555h     ; Security data
MOV   R2, #01h        ; Bank 1 to be erased
MOV   R3, #01h        ; Security: R3 must be equal to R2
MOV   R4, #050d       ; 50ns is 20MHz CPU clock frequency
MOV   R7, #08000h     ; R7 used for Flash trigger sequence

#define FCR 08000h
EXTS  #1, #2          ; flash can be mapped in segment 0 or 1
MOV   FCR, R7         ; first part
MOV   [R7], R7        ; second part
NOP                   ; WARNING: place 2 NOP operations after
NOP                   ; the Unlock sequence to avoid all possible
                      ; pipeline conflict in STEAK programs
; Check R0 return value

(see programming example)

CMP   R0, #0          ; Check error code returned by STEAK
JMP   cc_EQ, EraseDone; Erasing OK!


CMP   R0, #2          ; Vpp failed.
JMP   cc_NE, EraseError
JMP   cc_UC, ErrorVpp ; say that Vpp is failing.

EraseDone: (next instructions)
```

5 - FLASH PROTECTION ACTIVATION COMMAND

The STEAK Flash Protection Activation command allows to activate the Flash Protection mechanism.

5.1 - Flash Protection Mechanism

If the Flash Protection is active, data operands in the on-chip Flash Memory area can only be read by a program executed from the Flash Memory itself. Program branches from or into the on-chip Flash memory are possible in the Flash protection mode. **Erasing and programming of the Flash memory is not possible as long as protection is active.**

Flash protection is controlled by the Protection UPROM Programming Bit (UPROG). UPROG is a 'hidden' one-time programmable bit. If UPROG is set to "1", Flash protection is active after reset. All parts delivered by STMicroelectronics have the Flash Protection disabled (UPROG=0). The STEAK Flash Protection Activation command allows to program the UPROG bit.

When flash protection is active (default after reset if UPROG bit is set), then any read access in the flash by a code executed from external or internal RAM (IRAM or XRAM) will return the value 0B88Bh. Any call of STEAK will return the error code '01' (Protected flash).

5.2 - Flash Protection Temporary de-Activation

Flash protection can be 'temporary' de-activated, for example because the Flash memory has to be reprogrammed with updated program/variables. To 'temporary' de-activated the flash protection, a zero value has to be written at any even address in the active address space of the Flash memory.

This write MUST be done only by an instruction executed from the internal Flash Memory itself. For example:

```
MOV   FLASH,ZEROS   ; Deactivate Flash Protection. FLASH is any even
                    ; address in Flash memory space. This
                    ; instruction MUST be executed from Flash
                    ; memory itself.
```

After this instruction, the flash is temporary de-protected, thus any read access of the flash from code executed from external memory or internal RAMs will be correctly executed, and calls of STEAK can be correctly performed (programming, erasing or status reading).

Note that all STEAK commands will re-activate the flash protection if bit UPROG is set when completed.

5.3 - Management of error returned by STEAK Protection Activation Command

STEAK Flash Protection Activation Command routine is performing many internal checks and returns an error when the Flash Protection UPROM Programming Bit (UPROG) can NOT be programmed. Here are a guide of what should be done when STEAK Erasing command returns an error:

Error code 01 (flash protection is active):

– *Signification:* the Flash Protection is already active.

– *What can be done:* nothing, as the UPROG bit is already programmed.

Error code 02 (Vpp failed):

– *Signification:* the internal Vpp voltage in the flash is not within the specifications. This fail can be due a glitch on Vpp (Vpp decoupling) a voltage drop (Vpp generator current capability) or static erroneous Vpp (generator out of specifications).

– *What can be done:* check Vpp and restart the sequence.

– *Note:* the on chip hardware is not suitable for detecting marginal variations outside the specifications. Vpp compliance to the ST10 specifications shall be guaranted by the Vpp generator characteristics.

Error code 05 (CPU period out of range : must be between 30ns and 200ns):

– *Signification:* the CPU period given in R4 is out of valid range. This parameter is requested by STEAK programming commands to correctly time some waiting loops inside the STEAK routines.

– *What can be done:* provide a valid value in R4 before calling STEAK command.

– *Note:* big difference between the value entered in R4 and the real CPU period overstresses the cells during programming and can lower the flash life.

Error code 06 (Not enough free space on system stack for proper operation):

– *Signification:* the STEAK erasing routine needs at least 50 words on System Stack. STEAK routine performs the following check:
if (SP - STKOV) < 100 then return error 06.

– *What can be done:* change the initialisation setting of SYSCON (bitfield STKSZ) to provide a bigger stack size, or flush the System Stack to external memory before calling STEAK erasing command, and then restore it after STEAK return.

Error code 0B (PLL Unlock or Oscillator Watchdog Overflow occurred):

– *Signification:* PLL frequency is no more locked, or Oscillator Watchdog detected a missing input clock signal during UPROG programming operation. This error is returned if XP3IR Interrupt flag is set.

– *What can be done:* reset the device (hardware reset or software bi-directional reset) for re-locking the PLL, and retry the erasing command.

Error code FF (Bad STEAK command):

– *Signification:* the content of R1 register is not equal to #05555h, or the content of R2 register is not equal to #03333h, or the content of R3 register is not equal to #0AAAAh,or R0 content is not a valid command number.

– *What can be done:* be sure that R1 = #05555h, R2 = #03333h, R3 = #0AAAAh and R0 = #0CCCCh before calling STEAK Flash Protection Activation command.

5.4 - Flash Protection Activation using STEAK: code example

The following code is provided as an example for Flash Protection activation:

```
; code hereafter assumes that flash is mapped in segment 0
; i.e. bit ROMS1 = ‘0’ in SYSCON register
; Flash must also be enabled, i.e. bit ROMEN = ‘1’ in SYSCON.
SetProt:
MOV  R0, #0CCCCh     ; 0CCCCh: set flash protection command
MOV  R1, #05555h     ; Security data #1
MOV  R2, #03333h     ; Security data #2
MOV  R3, #0AAAAh     ; Security data #3
MOV  R4, #050d       ; 50ns is 20MHz CPU clock frequency
MOV  R7, #00000h     ; R7 used for Flash trigger sequence
#define FCR 00000h
EXTS #0, #2          ; flash is mapped in segment 0
MOV  FCR, R7         ; first part
MOV  [R7], R7        ; second part
NOP                  ; WARNING: place 2 NOP operations after
NOP                  ; the Unlock sequence to avoid all possible
                     ; pipeline conflict in STEAK programs
; Now, R0 contains error code if any, or zero
; and R1 contains STEAK revision code.
```

6 - READ STATUS COMMAND

The STEAK Read Status command allows to check:

– If Vpp voltage is present and > 11 V,
– The current revision of STEAK,
– The device internal code identifier.

6.1 - Current STEAK revision

The content of R1 register is modified by STEAK Read Status command, and the returned value is the current STEAK revision code. This code is composed of the major revision (on the 8 MSB of R1), and minor revision (on the 8 LSB of R1).

Example: R1 = 0100h means STEAK major revision is 1, minor revision 0: the STEAK revision is noted as rev. 1.0 (qualified revision).

6.2 - Management of error returned by STEAK Read Status Command

STEAK Read Status Command routine is just performing checks and returns an error code that describe a detected problem. Here are a guide of to interpret STEAK Read Status command returned error:

Error code 01 (flash protection is active):

– *Signification:* the Flash Protection is activated.

Error code 02 (Vpp failed):

– *Signification:* the internal Vpp voltage in the flash is not stabilized.

Error code 05 (CPU period out of range : must be between 30ns and 200ns):

– *Signification:* the CPU period given in R4 is out of valid range. This parameter is requested by STEAK programming commands to set the duration of time some waiting loops inside the STEAK routines.

Error code 06 (Not enough free space on system stack for proper operation):

– *Signification:* the STEAK erasing routine needs at least 50 words on System Stack. STEAK routine performs the following check: if (SP - STKOV) < 100 then return error 06.
– *What can be done:* change the initialisation setting of SYSCON (bitfield STKSZ) to provide a bigger stack size, or flush the System Stack to external memory before calling STEAK erasing command, and then restore it after STEAK return.

Error code FF (Bad STEAK command):

– *Signification:* the content of R0 register is not equal to a code of an implemented STEAK commands.

6.3 - Read Status using STEAK: code example

The following code is provided as an example for reading the STEAK status:

```
; code hereafter assumes that flash is mapped in segment 0
; i.e. bit ROMS1 = ‘0’ in SYSCON register
; Flash must also be enabled, i.e. bit ROMEN = ‘1’ in SYSCON.
ReadStatus:
MOV     R0, #07777h  ; 7777h: Read Status command
MOV     R4, #050d    ; 50ns is 20MHz CPU clock frequency
MOV     R7, #00000h  ; R7 used for Flash trigger sequence
#define FCR 00000h
EXTS    #0, #2       ; flash is mapped in segment 0
MOV     FCR, R7      ; first part
MOV     [R7], R7     ; second part
NOP                  ; WARNING: place 2 NOP operations after
NOP                  ; the Unlock sequence to avoid all possible
                     ; pipeline conflict in STEAK programs
; Now, R0 contains error code if any, or zero
; and R1 contains STEAK revision code.
```

7 - REVISION HISTORY

The revision of this application note is 1.0, released on the 16th of May 2000.