



# STD5NM60

N-CHANNEL 600V - 0.8Ω - 5A DPAK

MDmesh™ Power MOSFET

PRELIMINARY DATA

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STD5NM60	600V	<0.9Ω	5 A

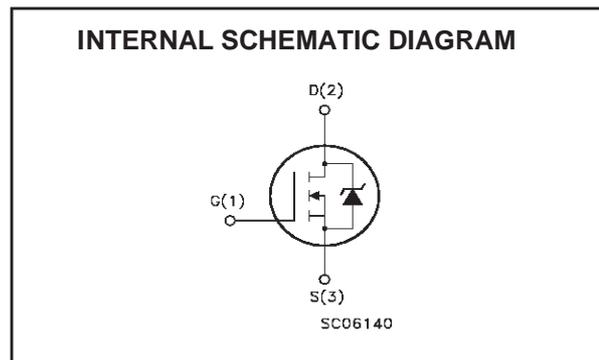
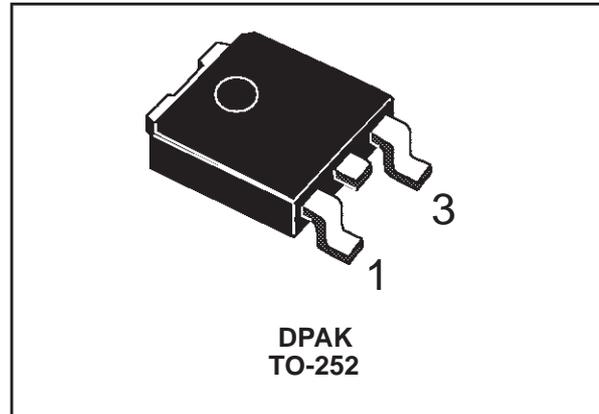
- TYPICAL R<sub>DS(on)</sub> = 0.8Ω
- HIGH dv/dt AND AVALANCHE CAPABILITIES
- 100% AVALANCHE TESTED
- LOW INPUT CAPACITANCE AND GATE CHARGE
- LOW GATE INPUT RESISTANCE
- TIGHT PROCESS CONTROL AND HIGH MANUFACTURING YIELDS

## DESCRIPTION

The MDmesh™ is a new revolutionary MOSFET technology that associates the Multiple Drain process with the Company's PowerMESH™ horizontal layout. The resulting product has an outstanding low on-resistance, impressively high dv/dt and excellent avalanche characteristics. The adoption of the Company's proprietary strip technique yields overall dynamic performance that is significantly better than that of similar completion's products.

## APPLICATIONS

The MDmesh™ family is very suitable for increase the power density of high voltage converters allowing system miniaturization and higher efficiencies.



## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	600	V
V <sub>DGR</sub>	Drain-gate Voltage (R <sub>GS</sub> = 20 kΩ)	600	V
V <sub>GS</sub>	Gate- source Voltage	±30	V
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 25°C	5	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 100°C	3.1	A
I <sub>DM</sub> (●)	Drain Current (pulsed)	20	A
P <sub>TOT</sub>	Total Dissipation at T <sub>C</sub> = 25°C	50	W
	Derating Factor	0.4	W/°C
dv/dt(1)	Peak Diode Recovery voltage slope	6	V/ns
T <sub>stg</sub>	Storage Temperature	-65 to 150	°C
T <sub>j</sub>	Max. Operating Junction Temperature	150	°C

(●)Pulse width limited by safe operating area

(1)|I<sub>SD</sub><5A, di/dt<200A/μs, V<sub>DD</sub><V<sub>(BR)DSS</sub>, T<sub>J</sub><T<sub>JMAX</sub>

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## STD5NM60

### THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	2.5	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5	°C/W
Rthc-sink	Thermal Resistance Case-sink Typ	0.5	°C/W
T <sub>l</sub>	Maximum Lead Temperature For Soldering Purpose	300	°C

### AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I <sub>AR</sub>	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T <sub>j</sub> max)	5	A
E <sub>AS</sub>	Single Pulse Avalanche Energy (starting T <sub>j</sub> = 25 °C, I <sub>D</sub> = I <sub>AR</sub> , V <sub>DD</sub> = 50 V)	400	mJ

### ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0	600			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max Rating V <sub>DS</sub> = Max Rating, T <sub>C</sub> = 125 °C			1 10	μA μA
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ±30V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	3	4	5	V
R <sub>DS(on)</sub>	Static Drain-source On Resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 2.5A		0.8	0.9	Ω
I <sub>D(on)</sub>	On State Drain Current	V <sub>DS</sub> > I <sub>D(on)</sub> × R <sub>DS(on)max</sub> , V <sub>GS</sub> = 10V	5			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub> (1)	Forward Transconductance	V <sub>DS</sub> > I <sub>D(on)</sub> × R <sub>DS(on)max</sub> , I <sub>D</sub> = 2.5A		2.4		S
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25V, f = 1 MHz, V <sub>GS</sub> = 0		412		pF
C <sub>OSS</sub>	Output Capacitance			94		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			10		pF
R <sub>G</sub>	Gate Input Resistance	f=1 MHz Gate DC Bias = 0 Test Signal Level = 20mV Open Drain		3		Ω

Note: 1. Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %.

**ELECTRICAL CHARACTERISTICS (CONTINUED)**
**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 300V, I_D = 2.5A$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see test circuit, Figure 3)		16		ns
$t_r$	Rise Time			9		ns
$Q_g$	Total Gate Charge	$V_{DD} = 400V, I_D = 5A,$ $V_{GS} = 10V$		13		nC
$Q_{gs}$	Gate-Source Charge			3		nC
$Q_{gd}$	Gate-Drain Charge			11		nC

**SWITCHING OFF**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	$V_{DD} = 480V, I_D = 5A,$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see test circuit, Figure 5)		20		ns
$t_f$	Fall Time			29		ns
$t_c$	Cross-over Time			30		ns

**SOURCE DRAIN DIODE**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain Current				5	A
$I_{SDM(2)}$	Source-drain Current (pulsed)				20	A
$V_{SD(1)}$	Forward On Voltage	$I_{SD} = 5A, V_{GS} = 0$			1.5	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 5A, di/dt = 100A/\mu s, V_{DD} = 100V, T_j = 150^\circ C$ (see test circuit, Figure 5)		300		ns
$Q_{rr}$	Reverse Recovery Charge			1.8		$\mu C$
$I_{RRM}$	Reverse Recovery Current			12		A

Note: 1. Pulsed: Pulse duration = 300  $\mu s$ , duty cycle 1.5 %.

2. Pulse width limited by safe operating area.

Fig. 1: Unclamped Inductive Load Test Circuit

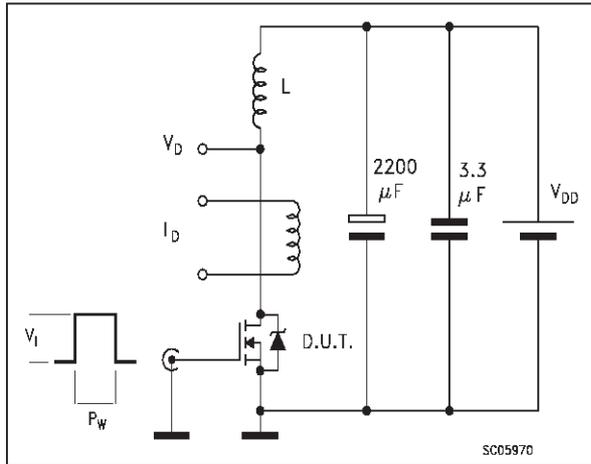


Fig. 2: Unclamped Inductive Waveform

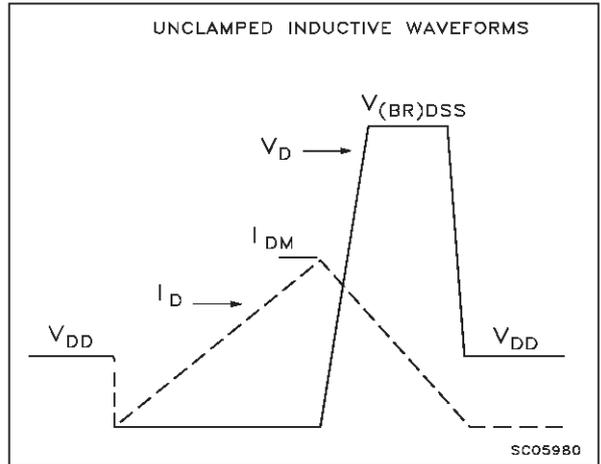


Fig. 3: Switching Times Test Circuit For Resistive Load

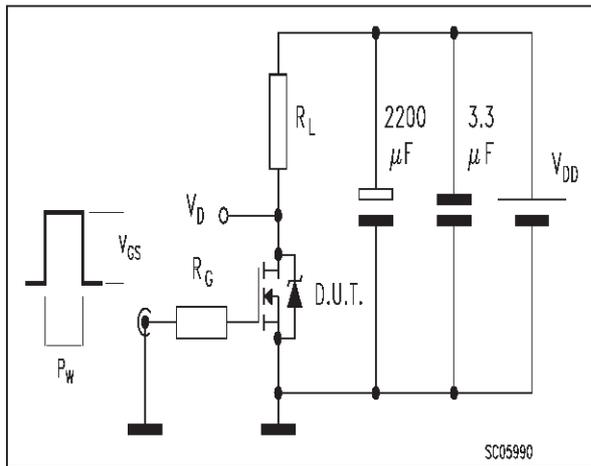


Fig. 4: Gate Charge test Circuit

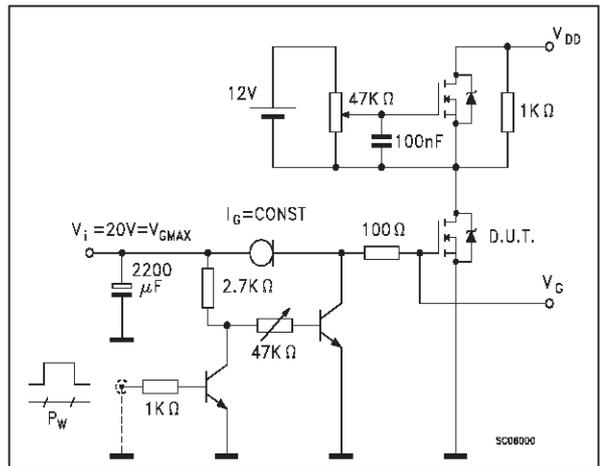
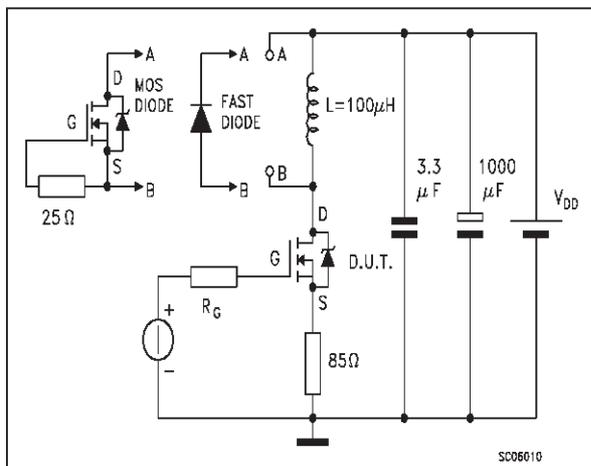
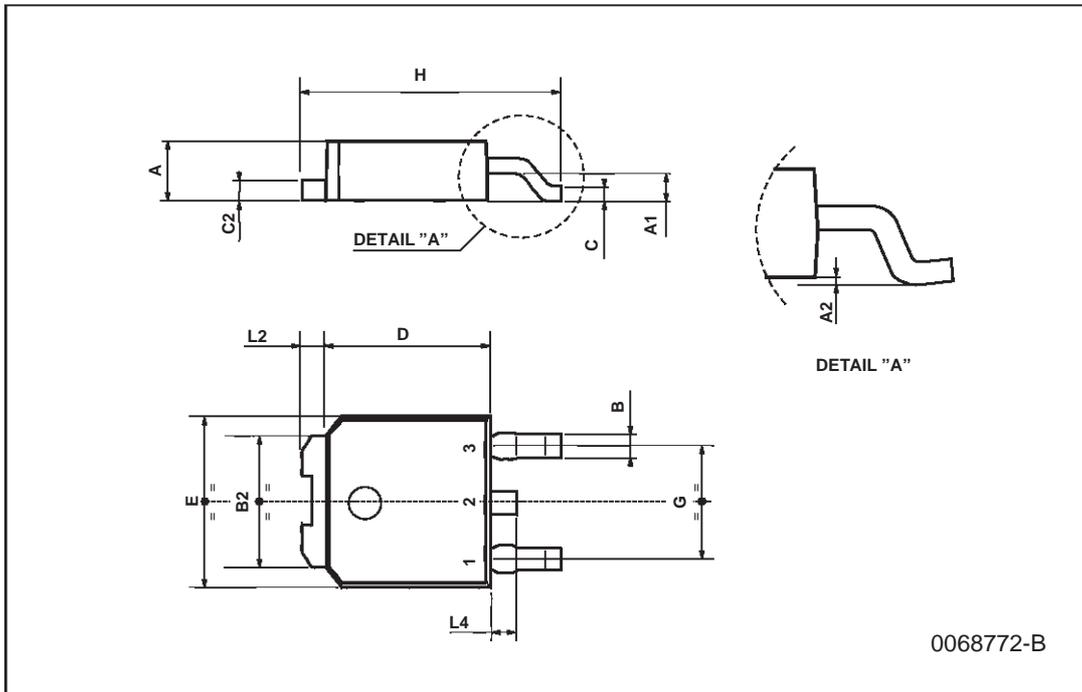


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-252 (DPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
B2	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L2		0.8			0.031	
L4	0.6		1	0.023		0.039



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