AN1160
APPLICATION NOTE

Connecting the TMS320C31 Microcontroller to M29 Series Flash Memories

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INTRODUCTION

This application note describes the connection of an M29F016B Flash memory to a TMS320C31 Digital Signal Processor. The application note can be used as a reference for other Flash memory devices and other microcontrollers. The application note discusses the Bus Architectures of the Flash and the TMS320C31. The additional features of the Flash, Reset/Block Temporary Unprotect and Ready/Busy Output are also discussed.

The information in this application note is useful to hardware engineers who are about to design a new circuit using a Flash memory.

ADVANTAGES OF FLASH

Flash memories can be used to store both code and data for DSPs in the TMS320 family of DSPs. The TMS320C31 bus only recognizes 32-bit wide memory, all data types are 32-bits wide (including **char**). However, the boot-loader can be configured to load the application code from the 8-bit wide Flash into 32-bit wide SRAM on power-up. This allows the TMS320C31 to boot from low cost, readily available memory and the M29F016B is ideally suited to this.

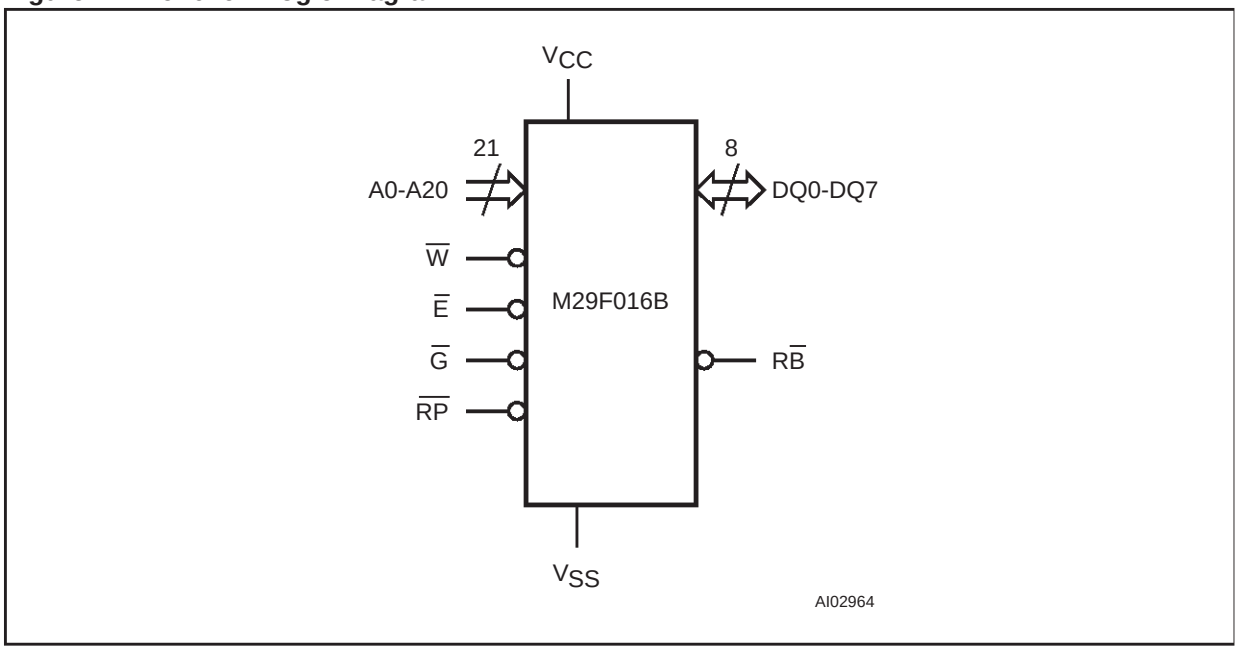
Unlike EPROM, Flash can be used to store data as well as code; the TMS320C31 can erase old, unwanted data and replace it. The application software can also be updated so that field upgrades of products can be performed without disassembling the product.

It is usual to write separate boot and application programs so that the application program can be upgraded without changing the boot program. If the upgrade fails then the DSP will still boot and it will be possible to reattempt to upgrade the application. The boot code should be programmed into the Flash before the Flash is fitted to the circuit board, otherwise the DSP will need to be booted from its serial port or JTAG emulator. Often the block containing the boot program is protected so it cannot become corrupt.

FLASH BUS ARCHITECTURE

Take a look at the bus on the M29F016B, Figure 1 shows the Logic Diagram. The memory has separate Address and Data Buses. The control lines are Chip Enable ($\overline{E}$), Output Enable ($\overline{G}$) and Write Enable ($\overline{W}$). Also, Ready/Busy Output (R/$\overline{B}$) and Reset/Block Temporary Unprotect ($\overline{RP}$) are present.

Figure 1. M29F016B Logic Diagram

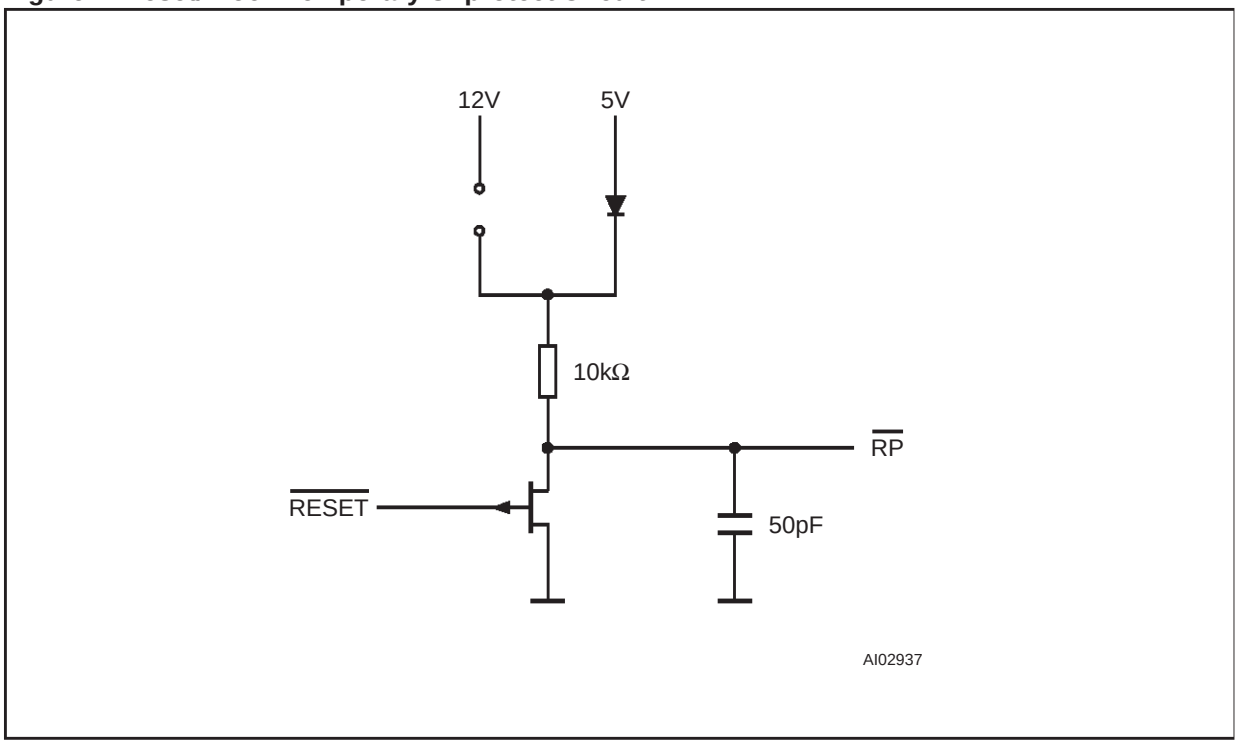


The Reset/Block Temporary Unprotect pin ($\overline{RP}$) accepts three states: Reset (V_{IL}), Not Reset (V_{IH}) and Block Temporary Unprotect (V_{ID}). Reset and Not Reset are the usual signals for a $\overline{RESET}$ line. The third state, Block Temporary Unprotect is used to temporarily unprotect blocks that have been specifically protected in the memory. Many applications do not protect any blocks and therefore connect the $\overline{RP}$ pin directly to the system $\overline{RESET}$ signal.

Figure 2 gives an example of how the connection between the system's $\overline{RESET}$ pin and the M29F016B's $\overline{RP}$ pin can be made. The circuit makes use of a jumper to enable Block Temporary Unprotect. Many applications will provide the 12V from an external source, in which case the jumper can be replaced by a connector. The advantage with the circuit, as it stands, is that the system reset will override Block Temporary Unprotect and cause the Flash to reset. Only four additional components are required.

Before the jumper is inserted, and when $\overline{RESET}$ is High, V_{IH}, $\overline{RP}$ is connected to 5V through the 10kΩ resistor and the diode. The current required by $\overline{RP}$ is very low, in the order of 1µA at 5V. The voltage drop in the resistor and the diode at these currents will keep $\overline{RP}$ very close to 5V. When the jumper is fitted the diode ceases to conduct and $\overline{RP}$ rises to 12V as the capacitor charges. The time-constant of a 10kΩ resistor and a 50pF capacitor is 500ns, satisfying the t_{PHPHH} rise-time requirements of the M29F016B. During a reset, $\overline{RESET}$ is Low, V_{IL}, and the JFET is switched on, bringing $\overline{RP}$ close to ground. The current consumption during a reset rises due to the current through the 10kΩ resistor.

Figure 2. Reset/Block Temporary Unprotect Circuit



Although the use of a jumper may not be the most elegant solution, it is a practical one because it maintains the security level offered by Block Protection. There is little point in having the Block Temporary Unprotect pin under software control. The whole point of the Block Protection feature is to protect against software failure. Allowing the Block Temporary Unprotect feature to be under the control of software is nearly equivalent to not protecting the blocks in the first place.

The Ready/Busy Output ($R\overline{B}$) provides a simple mechanism for determining if the Flash is busy or not. By connecting the Ready/Busy pin up to an interrupt line of the microcontroller it is possible to program the Flash under interrupt control, freeing the DSP to perform other tasks while the Flash is programming. Otherwise the Flash must be polled in order to find out if program or erase operations have completed. Ready/Busy is an open drain output and, therefore, requires a pull-up resistor to bring the line up to V_{CC} when the Flash is ready.

One situation that the software must be aware of is the error situation. When a program or erase error occurs Ready/Busy will remain low until the error is cleared. A timer, or polling algorithm, should be used to catch this situation and deal with it correctly.

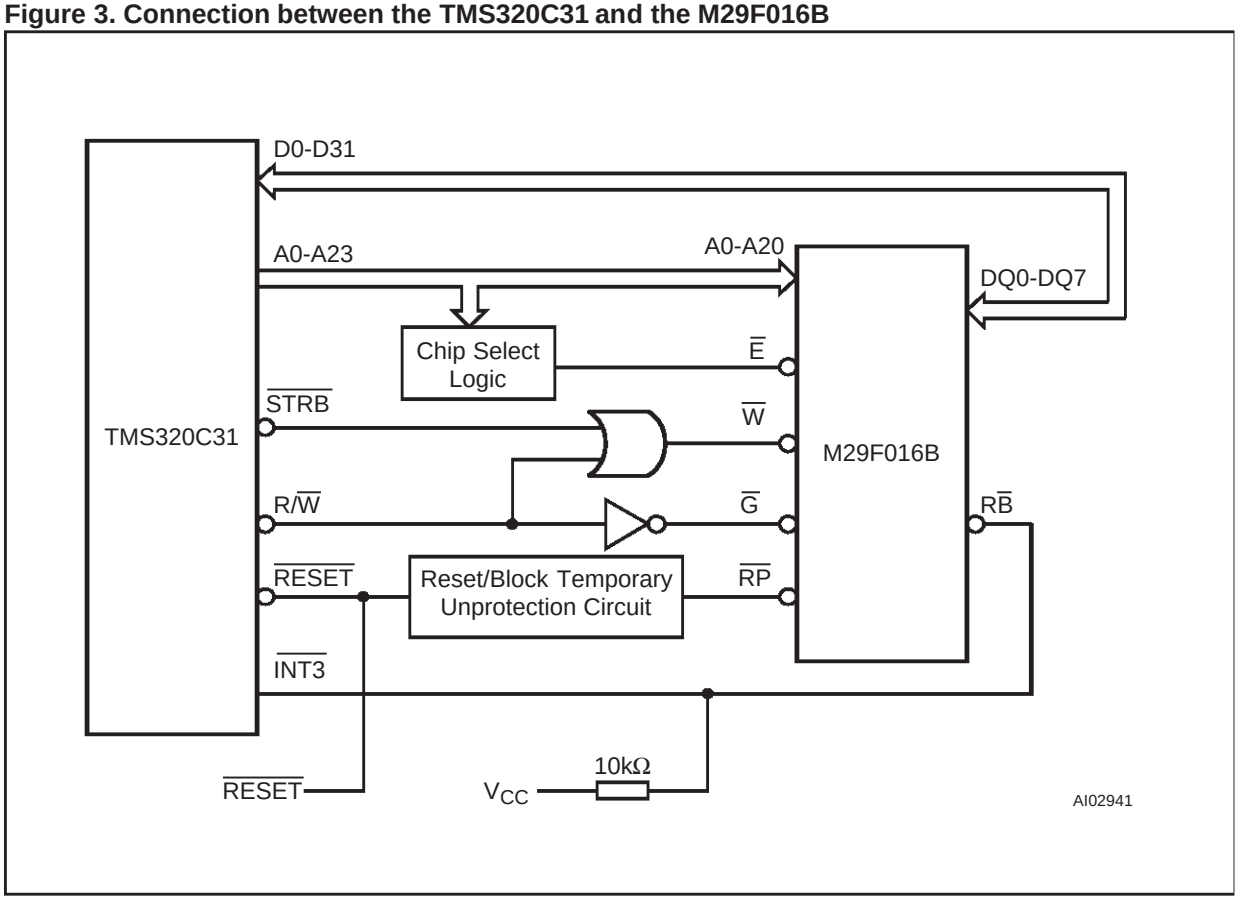
TMS320C31 BUS ARCHITECTURE

The TMS320C31 has a 32-bit data bus and 24-bit address bus. In order to reduce the complexity the bus only supports 32-bit accesses. For devices with smaller widths than 32-bits the unused bits have to be masked by the software after read operations. The $\overline{STRB}$ signal indicates that a bus access is currently taking place, the $\overline{RDY}$ signal is used by external devices to indicate that they are ready and the R/$\overline{W}$ signal indicates if the access is a read or a write.

The TMS320C31 has an internal wait-state generator that can be used to extend the access times for slower devices on the bus. The end of a cycle can be determined by either the $\overline{RDY}$ input or the wait-state generator. Bank-switching detection can also be employed to add in an additional wait-state when changing from one type of memory to another; this extends the end of the access cycle so devices that take too long to tri-state their outputs do not cause bus contention with fast devices. The TMS320C31 always inserts an additional wait-state when writing compared to reading; this additional wait-state also helps the tri-state time of external devices.

The connection between the TMS320C31 and the M29F016B Flash is shown in Figure 3. The $\overline{RDY}$ signal has not been shown in the diagram as it is assumed that the internal wait-state generator will be used to generate the correct access times.

Figure 3. Connection between the TMS320C31 and the M29F016B



TIMING REQUIREMENTS

The read timings (from the Flash's perspective) are shown using one wait-state in Table 1 and Figure 4; the write timings are shown in Table 2 and Figure 5. The TMS320C31 always uses one additional wait-state for write cycles compared to read cycles. Bank switching has been assumed for the tri-state times.

Table 1. Principal Read Timing Requirements

M29F016B				TMS320C31		
Symbol	**55**	**70**	**90**	**f_{CLKIN} = 40MHz**	**f_{CLKIN} = 50MHz**	**f_{CLKIN} = 60MHz**
t_{AVAV}	55	70	90	89	71	58
t_{AVQV}	55	70	90	75	61	49
t_{ELQV}	55	70	90	70	56	44
t_{GLQV}	30	30	35	111	90	74
t_{EHQZ}	18	20	20	89	80	66
t_{OH}	0	0	0	0	0	0

Figure 4. Principal Read Timing Waveforms

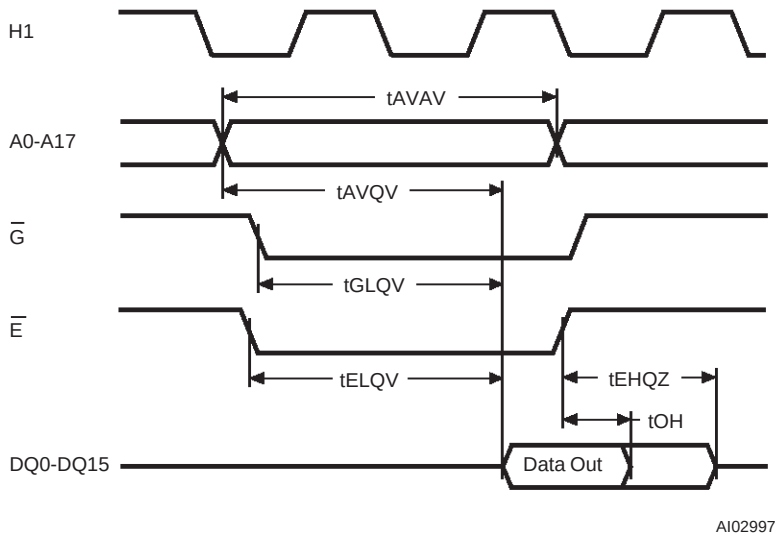
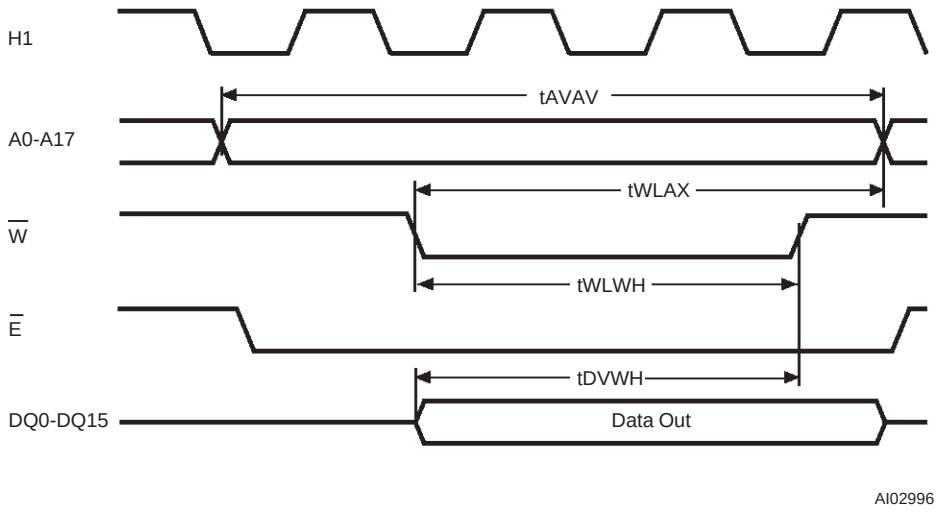


Table 2. Principal Write Timing Requirements, Write Enable Controlled

M29F016B				TMS320C31		
Symbol	**55**	**70**	**90**	**f_{CLKIN} = 40MHz**	**f_{CLKIN} = 50MHz**	**f_{CLKIN} = 60MHz**
t_{AVAV}	55	70	90	139	111	92
t_{WLWH}	40	45	45	89	70	56
t_{DVWH}	25	30	45	83	66	54
t_{WHWL}	20	20	20	44	35	28
t_{WLAX}	40	45	45	89	70	56

Figure 5. Principal Write Timing Waveforms



It can be seen that the M29F016B-55 can be used with one wait-state for the 50MHz clock speed, the M29F016B-70 can be used for the 40MHz clock speed, but the faster, 60MHz clock cannot be satisfied by any of the parts. An additional wait-state will be required to work above 60MHz.

CONCLUSIONS

The M29F016B, and other Flash memory parts from STMicroelectronics, can be easily connected to the TMS320C31 and other DSP with minimal glue logic. One or two wait-state solutions can be realized. The Block Temporary Unprotect feature can be designed in easily and the software overhead for programming the Flash can be reduced by connecting the Ready/Busy Output pin to an interrupt line.

If you have any questions or suggestion concerning the matters raised in this document please send them to the following electronic mail address:

ask.memory@st.com (for general enquiries)

Please remember to include your name, company, location, telephone number and fax number.