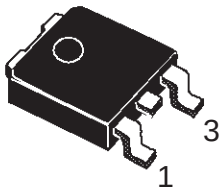
STD15NF10

N-CHANNEL 100V - 0.073Ω - 15A DPAK
LOW GATE CHARGE STripFET™ POWER MOSFET

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STD15NF10	100 V	< 0.08 Ω	15 A

- TYPICAL $R_{DS}(on)$ = 0.073Ω
- EXCEPTIONAL dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- APPLICATION ORIENTED CHARACTERIZATION

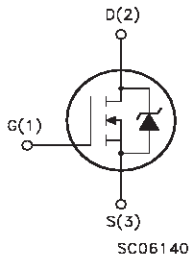


DPAK
TO-252

DESCRIPTION

This Power Mosfet series realized with STMicroelectronics unique STripFET process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high-efficiency isolated DC-DC converters for Telecom and Computer application. It is also intended for any application with low gate charge drive requirements.

INTERNAL SCHEMATIC DIAGRAM



APPLICATIONS

- HIGH-EFFICIENCY DC-DC CONVERTERS
- UPS AND MOTOR CONTROL

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	100	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	100	V
V_{GS}	Gate- source Voltage	±20	V
I_D	Drain Current (continuos) at T_C = 25°C	15	A
I_D	Drain Current (continuos) at T_C = 100°C	10	A
I_{DM} (●)	Drain Current (pulsed)	60	A
P_{TOT}	Total Dissipation at T_C = 25°C	45	W
	Derating Factor	0.3	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	9	V/ns
E_{AS} (2)	Single Pulse Avalanche Energy	75	mJ
T_{stg}	Storage Temperature	–65 to 175	°C
T_j	Max. Operating Junction Temperature	175	°C

(●) Pulse width limited by safe operating area

(1) I_{SD} ≤24A, di/dt ≤300A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX.}$
(2) Starting T_j = 25°C, I_D = 24A, V_{DD} = 50V

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	3.33	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose	300	°C

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0	100			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating			1	µA
		V_{DS} = Max Rating, T_C = 125 °C			10	µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ±20V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250µA	2	3	4	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V, I_D = 12 A		0.073	0.08	Ω
$I_{D(on)}$	On State Drain Current	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$, V_{GS} = 10V	15			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$, I_D = 7.5 A		12		S
C_{iss}	Input Capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		870		pF
C_{oss}	Output Capacitance			125		pF
C_{rss}	Reverse Transfer Capacitance			52		pF

ELECTRICAL CHARACTERISTICS (CONTINUED)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	V_{DD} = 50V, I_D = 12 A		58		ns
t_r	Rise Time	R_G = 4.7Ω V_{GS} = 10V (see test circuit, Figure 3)		45		ns
Q_g	Total Gate Charge	V_{DD} = 80 V, I_D = 24 A,		30		nC
Q_{gs}	Gate-Source Charge	V_{GS} = 10V		6		nC
Q_{gd}	Gate-Drain Charge			10		nC

SWITCHING OFF

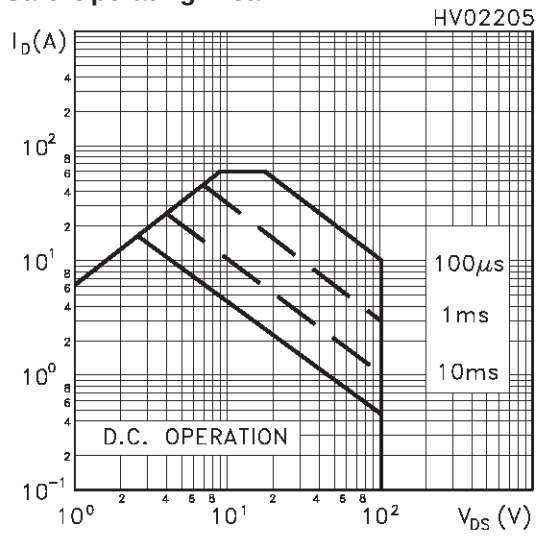
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off-Delay Time	V_{DD} = 50 V, I_D = 12 A, R_G = 4.7Ω, V_{GS} = 10V (see test circuit, Figure 3)		49		ns
t_f	Fall Time			17		ns
$t_{d(off)}$	Off-voltage Rise Time	Vclamp = 80V, I_D = 24 A R_G = 4.7Ω, V_{GS} = 10V		43		ns
t_f	Fall Time	(see test circuit, Figure 5)		21		ns
t_c	Cross-over Time			39		ns

SOURCE DRAIN DIODE

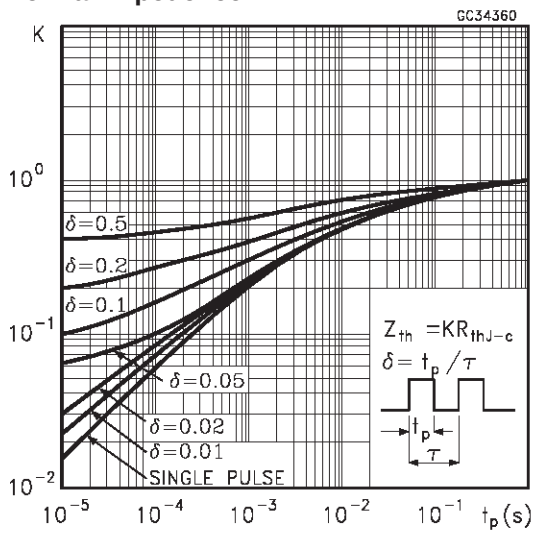
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				15	A
I_{SDM} (1)	Source-drain Current (pulsed)				60	A
V_{SD} (2)	Forward On Voltage	I_{SD} = 15 A, V_{GS} = 0			1.5	V
t_{rr}	Reverse Recovery Time	I_{SD} = 15 A, di/dt = 100A/µs, V_{DD} = 30 V, T_j = 150°C (see test circuit, Figure 5)		100		ns
Q_{rr}	Reverse Recovery Charge			375		nC
I_{RRM}	Reverse Recovery Current			7.5		A

Note: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

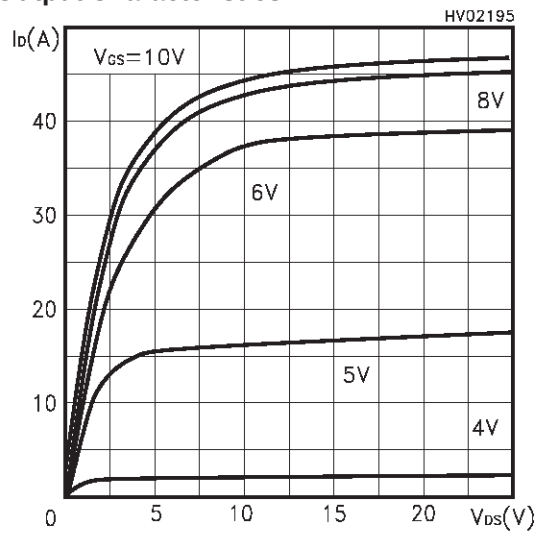
Safe Operating Area



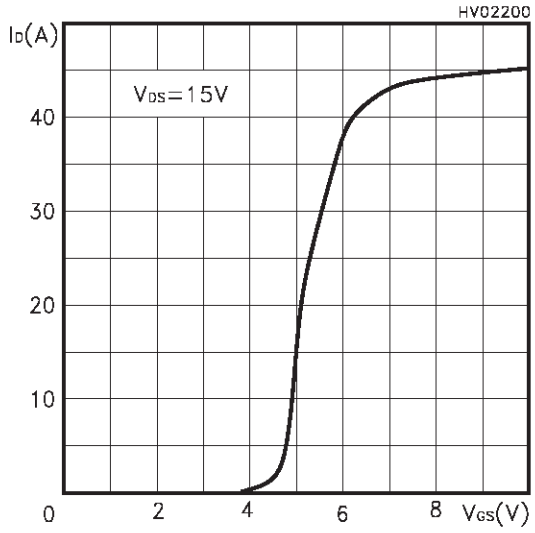
Thermal Impedence



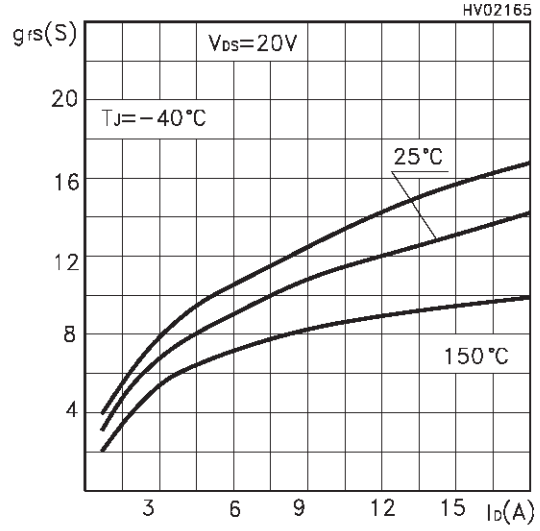
Output Characteristics



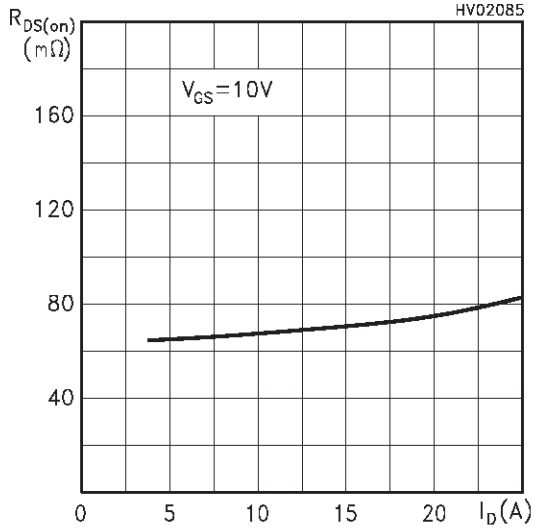
Transfer Characteristics



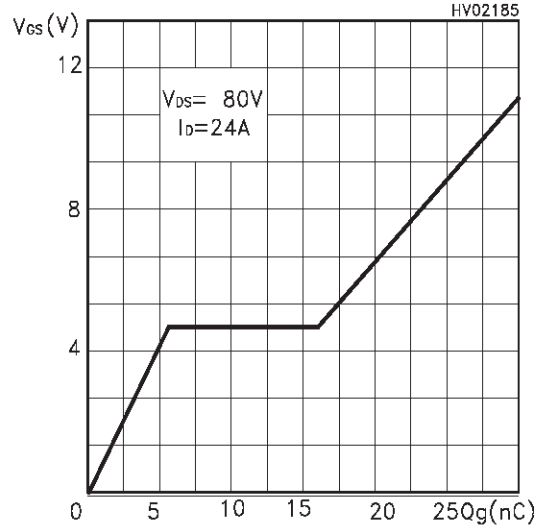
Transconductance



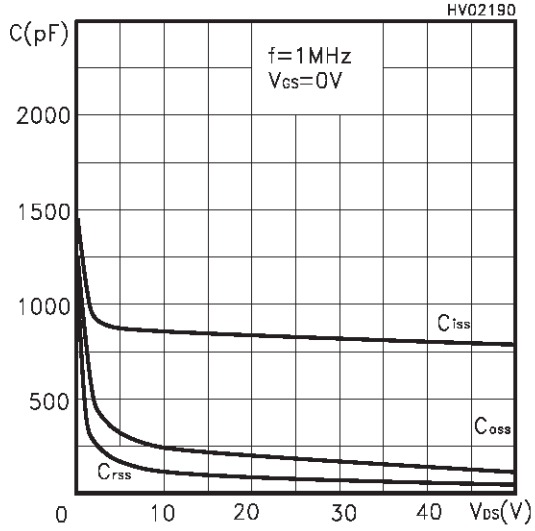
Static Drain-source On Resistance



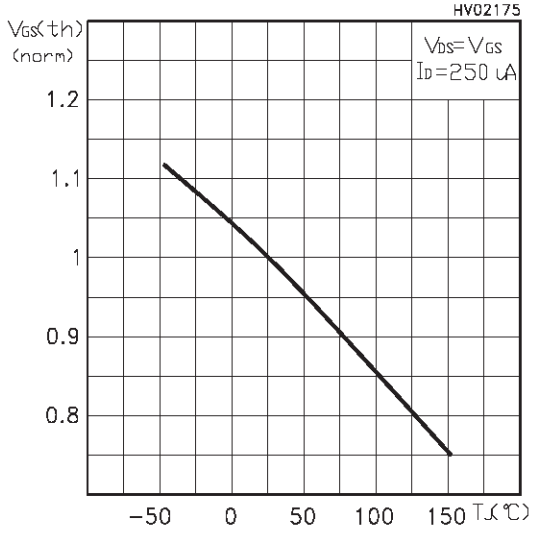
Gate Charge vs Gate-source Voltage



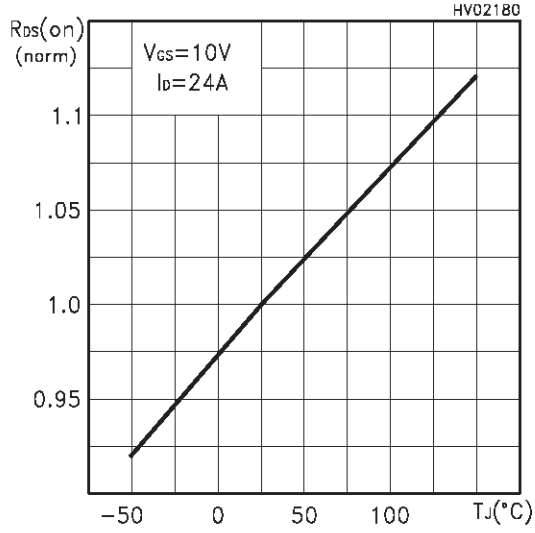
Capacitance Variations



Normalized Gate Thereshold Voltage vs Temp.



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

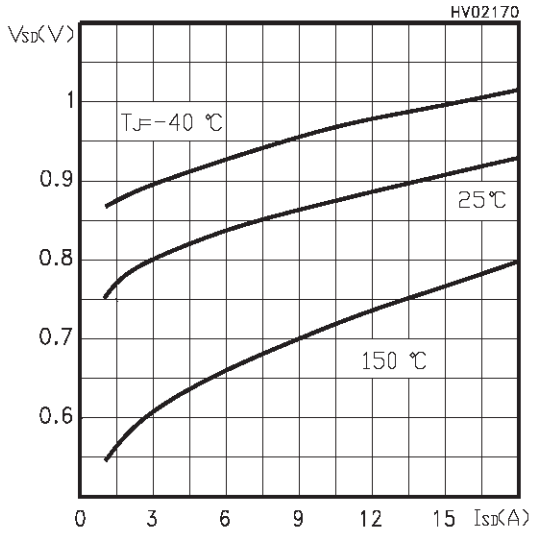


Fig. 1: Unclamped Inductive Load Test Circuit

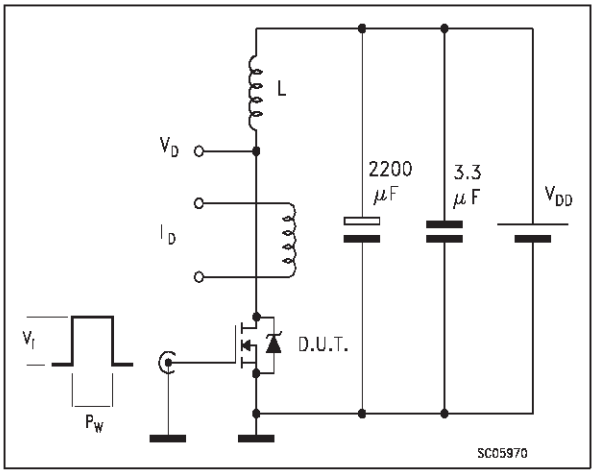


Fig. 2: Unclamped Inductive Waveform

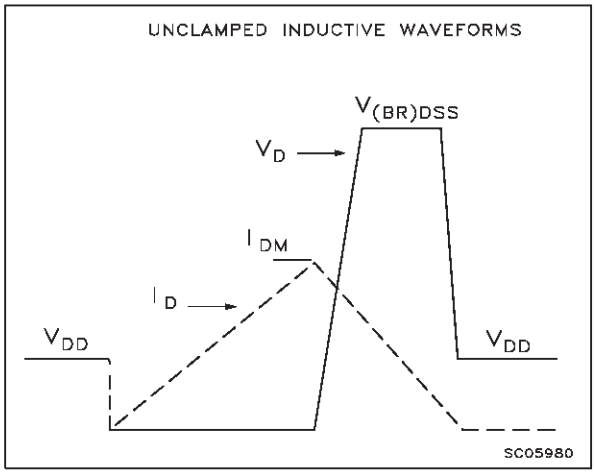


Fig. 3: Switching Times Test Circuit For Resistive Load

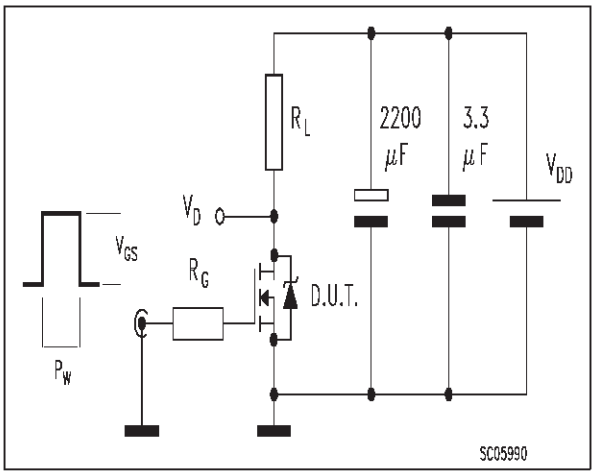


Fig. 4: Gate Charge test Circuit

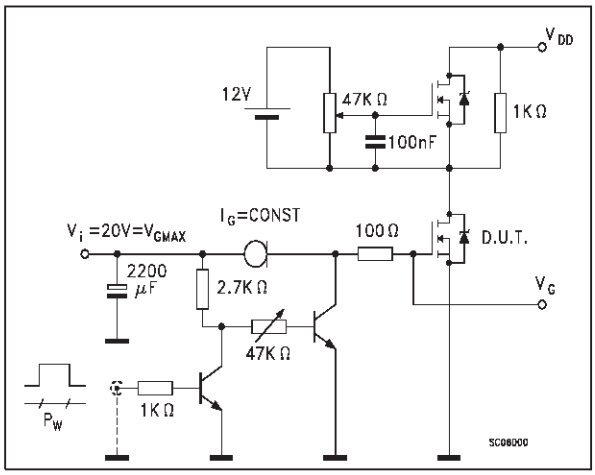
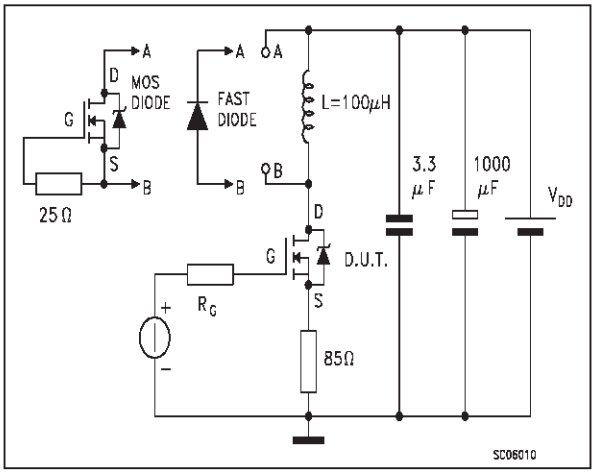
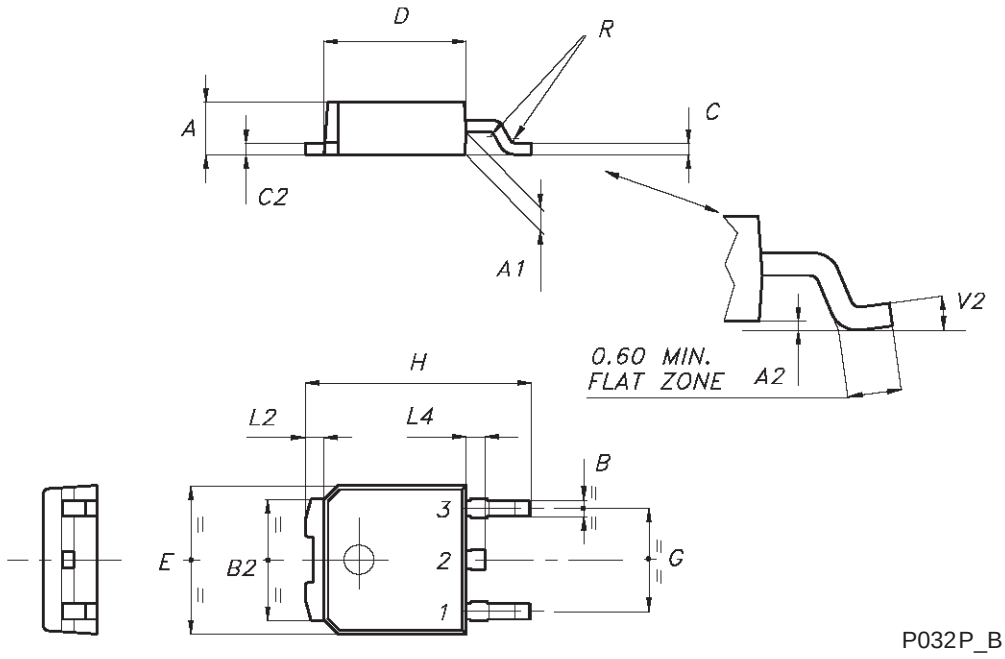


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-252 (DPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.20		2.40	0.087		0.094
A1	0.90		1.10	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.90	0.025		0.035
B2	5.20		5.40	0.204		0.213
C	0.45		0.60	0.018		0.024
C2	0.48		0.60	0.019		0.024
D	6.00		6.20	0.236		0.244
E	6.40		6.60	0.252		0.260
G	4.40		4.60	0.173		0.181
H	9.35		10.10	0.368		0.398
L2		0.8			0.031	
L4	0.60		1.00	0.024		0.039
V2	0^o		8^o	0^o		0^o



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