AN1258
APPLICATION NOTE

VIPer20 DEMOBOARD STAND-BY APPLICATION

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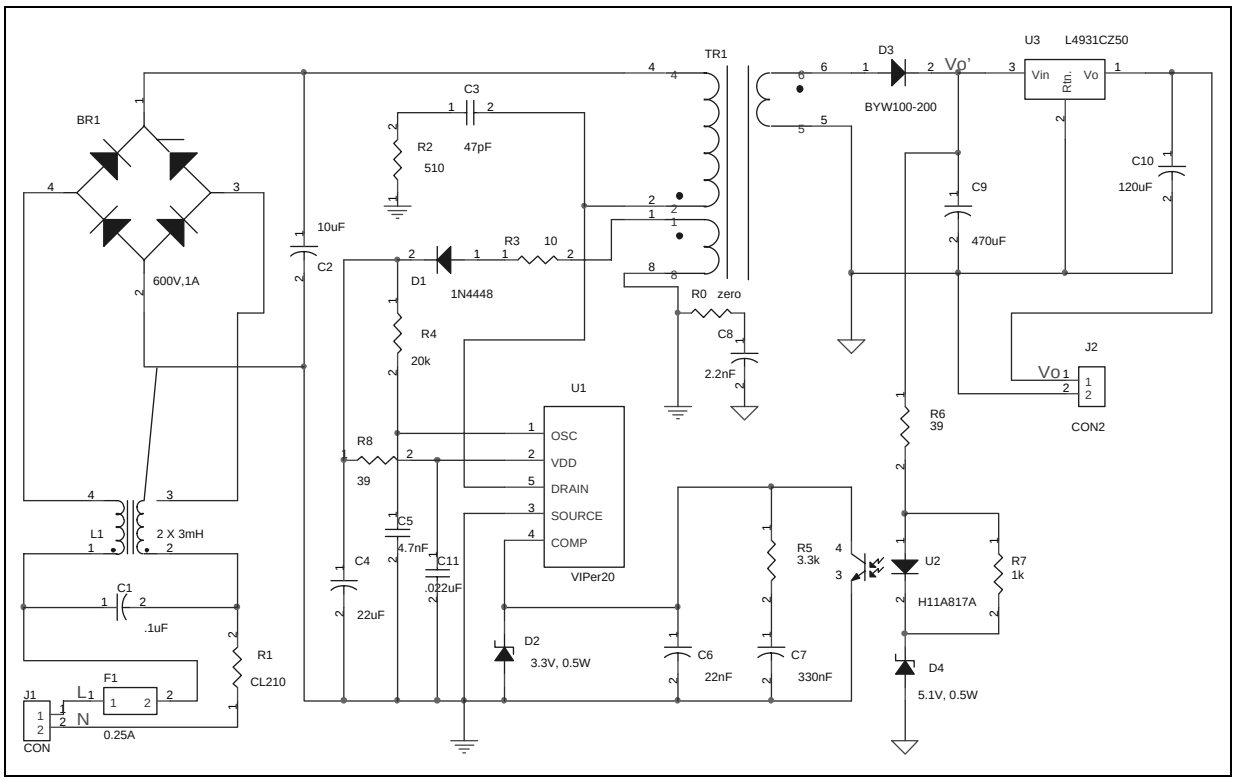
1. ABSTRACT

This general flyback circuit can be used to produce any output voltage in primary or secondary mode regulation and is suitable for a multiple output power supply. This application is for a low input power standby power supply and uses theVIPer20DIP.

2. INTRODUCTION.

The VIPer20 technology contains a state of the art PWM circuit and a Vertical Power MOSFET, which is avalanche rugged, on the same silicon chip. It is suitable for off line wide range input voltage flyback power supplies of up to 10W (20W for high input voltage range) in discontinuous mode. This solution has the advantage of using few external components compared to a discrete solution, can be used for primary or secondary regulation, has a burst mode in standby for Blue Angel operation, an external pin is used to set the operating frequency up to 200kHz, an external pin is provided for compensation, has current mode control, a built in current limit and contains thermal protection.

Figure 1: Stand-by Application Circuit



The following description is for a standby application with a 5V output voltage, an input power of 1W and a wide range input voltage (see figure 1). TheVIPer20 used is an eight pin dip rated for 620V maximum with a maximum peak drain current of 0.5A. In the circuit at maximum load, the device has a maximum voltage of 510V at 264VAC and a maximum peak current of 0.17A at 70VAC. This circuit is operating at 24kHz and is set up for primary regulation or secondary regulation with an optoisolator.

The circuit contains an input fuse (F1), an inrush thermistor (R1), EMI filtering (C1, L1, C8), and a snubber circuit (C3, R2). C6, C7 and R5 are used for compensation. D2 can be used to limit the maximum output power. C11 and R8 provide extra immunity for lightning strike. The output transformer (TR1) is built by Cramer Coil & Transformer Co., Inc. (CVP 10-001).

The following component values can be used with the schematic for 5V at 0.02A minimum to a maximum output current (Io maximum in table 2) with an input voltage range of 70 to 264VAC. The 5V load current, Io, is listed for an input power of 1W measured at 115VAC. Case (1) values, of table 1, are shown in figure 1.

Table 1: Cases Observed

Case	L2 or U3	R3	R7	D4 ± 2%	Vo'	Vo ± 5%	Io at Pin= 1W	Io max
1	U3	10	1k	5.1V	6.2 ±5%	5V	0.09A	0.22
2	U3	1	-	-	7.3 ±10%	5V	0.07A	0.2
3	L2	1	180	4.3V	5.1 ±5%	5.1V	0.11A	0.27

For case 1 the 5V output is produced with secondary regulation, using a low drop three terminal regulator, U3, and a pre-regulated input voltage at Vo' (see figure 1). In case 2 the 5V output is produced with primary regulation and a three terminal regulator U3. The value of R3 is changed and components L2, R6, U2, R7 and D4 in figure 1 are not used. In case 3 the 5V can be produced directly with secondary regulation. A10uH inductor, L2, is used instead of U3 and the values of R3, R7 and D4 are changed in figure 1 respectively. For wide range temperature applications, the output voltage tolerance may exceed ±5%.

The output transformer, TR1, is optimized for case 1 but can also be designed for case 3 and for primary mode regulation in case 2 with a standard three terminal regulator.

Table 2: Operating Conditions

Parameter	Limits
Input voltage range	70 to 264 Vac
Input Frequency range	50/60 Hz
Temperature range	10 to 55°C
Output voltage	5V (see Table 1)
Output power (discontinuous)	(see Table 1)
Output power (peak)	1.5W
Line regulation	U3 spec.
Load regulation	U3 spec.
Efficiency	(see Figure 6)
Output ripple voltage	<20mv typical

Table 3: Components Listing

Reference	Value	Part Number	Manufacturer
BR1	600V, 1A		
C1	0.1µF, 250V		
C2	10µF, 400V		
C3	47pF, 1kV		
C4	22µF, 25V		
C5	4.7nF, 50V		
C6	22nF, 50V		
C7	330nF, 50V		
C8	2.2nF, “Y”, 20V		
C9	470µF, 16V		
C10	120µF, 16V		
C11	0.022µF, 50V		
D1		1N4448	STMicroelectronics
D2	3.3V, 0.5W		
D3		BYW100-200	STMicroelectronics
D4	5.1V, 0.5W		
F1	0.25A, 5x20mm		
J1	5mm	CON	Phoenix
J2	5mm	CON2	Phoenix
L1	2x3mH	RN202-1/02	Schaffner
L2	10µH		
R0	0Ω		
R1		CL210	NTC
R2	510Ω, 0.25W, 5%		
R3	10Ω, 0.25W, 5%		
R4	20KΩ, 0.25W, 5%		
R5	3.3KΩ, 0.25W, 5%		
R6	39Ω, 0.25W, 5%		
R7	1KΩ, 0.25W, 5%		
R8	39Ω, 0.25W, 5%		
TR1		CVP 10-001	Cramer Coil & Transf.
U1		VIPer20DIP	STMicroelectronics
U2		H11A817A	
U3		L4931CZ50	STMicroelectronics

3. WAVE FORMS.

Figures 2 and 3 show typical wave forms of the drain source voltage and the drain current for an input voltage of 115 VAC and maximum load current.

Figure 2: Drain Source Voltage and Drain Current

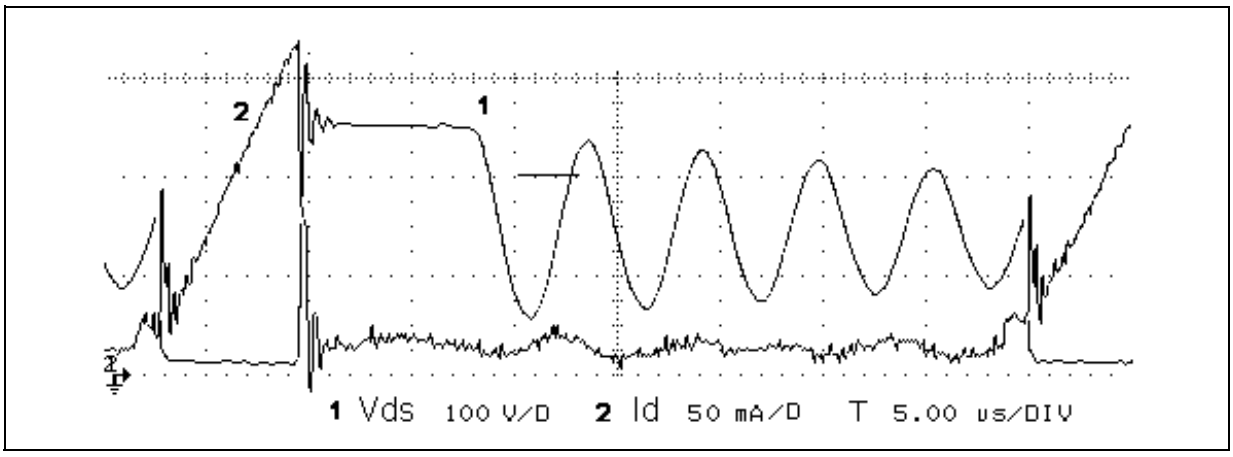
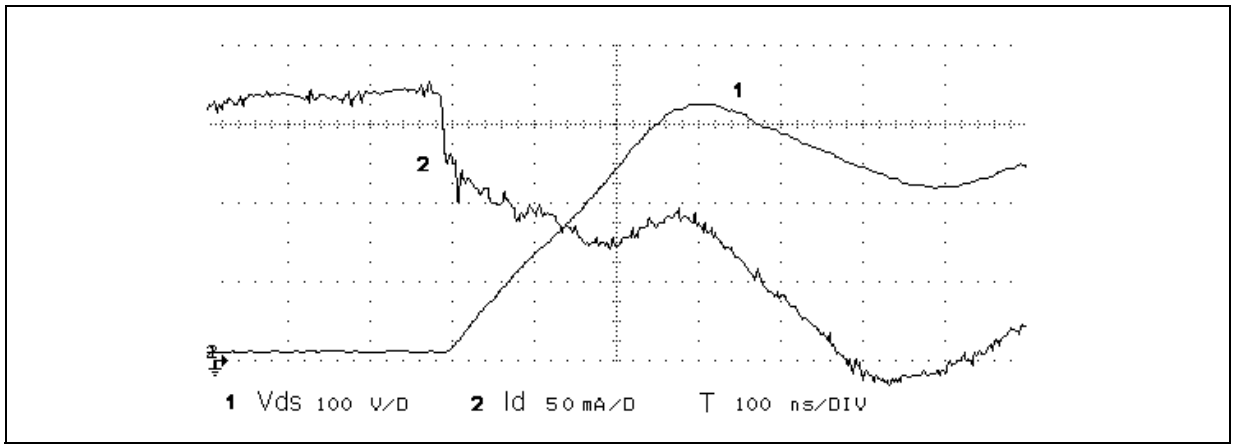


Figure 3: Drain Source Voltage and Drain Current



4. BOARD LEGEND.

The components for the major loop (the bulk capacitor C2, the primary on the output transformer TR1 and the VIPer20 U1) are placed in close proximity so that the current loop area is as small as possible. Also, components on the secondary (output rectifier D3, capacitors C9, C10, and transformer output winding TR1) are placed to reduce the current loop area.

Figure 4 and 5 show the VIPer20 Demo Board printed circuit board layout. Note that the width of the current loop area used is as small as possible and still meet the voltage spacing requirements.

Figure 4: PC Board Top Legend

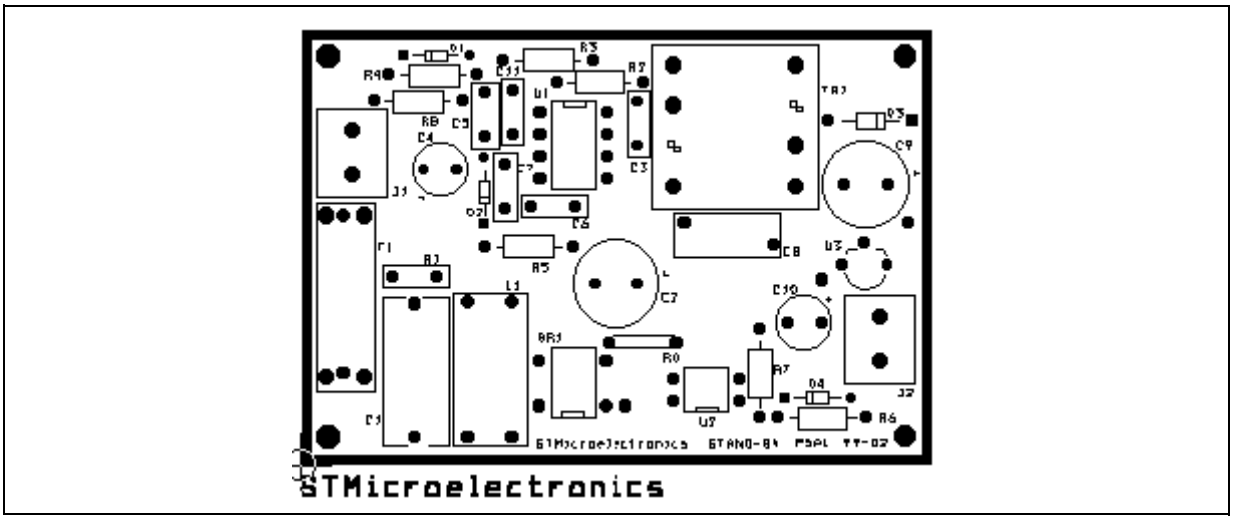
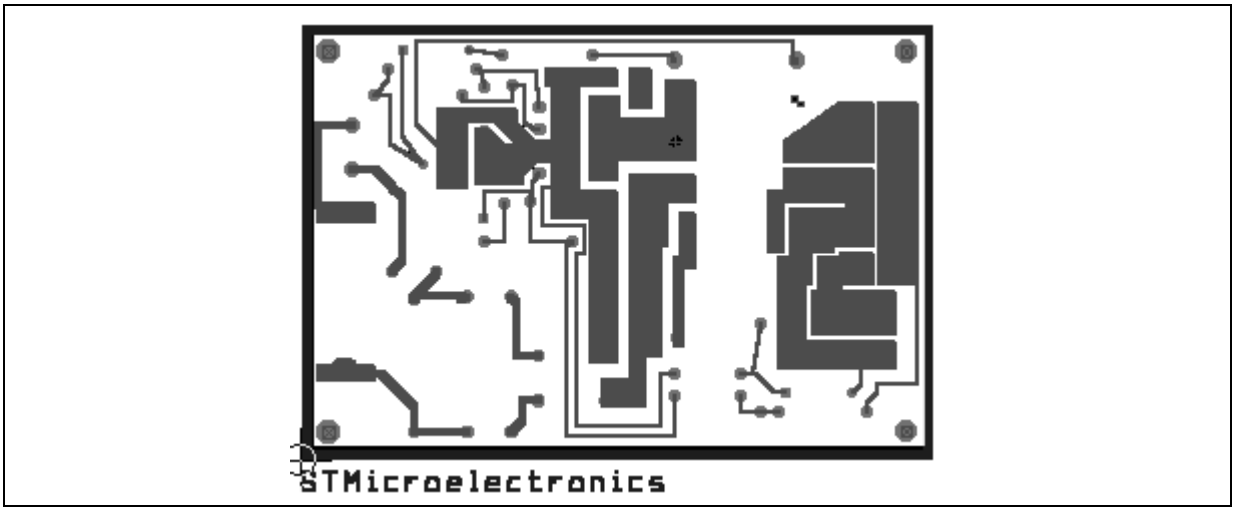


Figure 5: PC Board Bottom Foil



5. GENERAL CIRCUIT DESCRIPTION.

The VIPer20 Demo Board is designed as a discontinuous flyback regulator where the energy is stored in the transformer TR1, with primary winding 2-4, when the VIPer (U1) is on and delivered to the output, 6-5, and auxiliary winding, 1-8, when the VIPer is off. The auxiliary winding provides the bias voltage for the VIPer at the Vdd pin 2. The frequency of operation is determined externally by R4 and C5 at oscillator pin 1. The output voltage, Vo, is regulated with the three terminal regulator U3. The U3 input voltage, Vo', is pre-regulated via the optoisolator, U2, with R6, R7, and D4 in order to reduce the input power. The components R5, C6 and C7 are used for compensation.

6. THERMAL CONSIDERATIONS.

The demo board is single sided and utilizes one ounce copper for all of the traces. A wide area of copper is used for a pad, on the demo board, to act as a heat sink for the VIPer20 Dip which will reach a peak Ids current of 0.5A before a thermal limit. The components which have a thermal limitation for a higher output power application are the three terminal regulator, U3 (250mA Io max), and the output transformer, TR1 (300mA).

7. TRANSFORMER CONSIDERATIONS.

The output transformer has a primary inductance of 5mH, a ferrite core EE16 with an AL of 150 and is primary - secondary Hi Pot tested to 4000VAC for 1 second. It is wound with a split primary - half on the bottom and half on the top with the auxiliary and output windings in the middle.

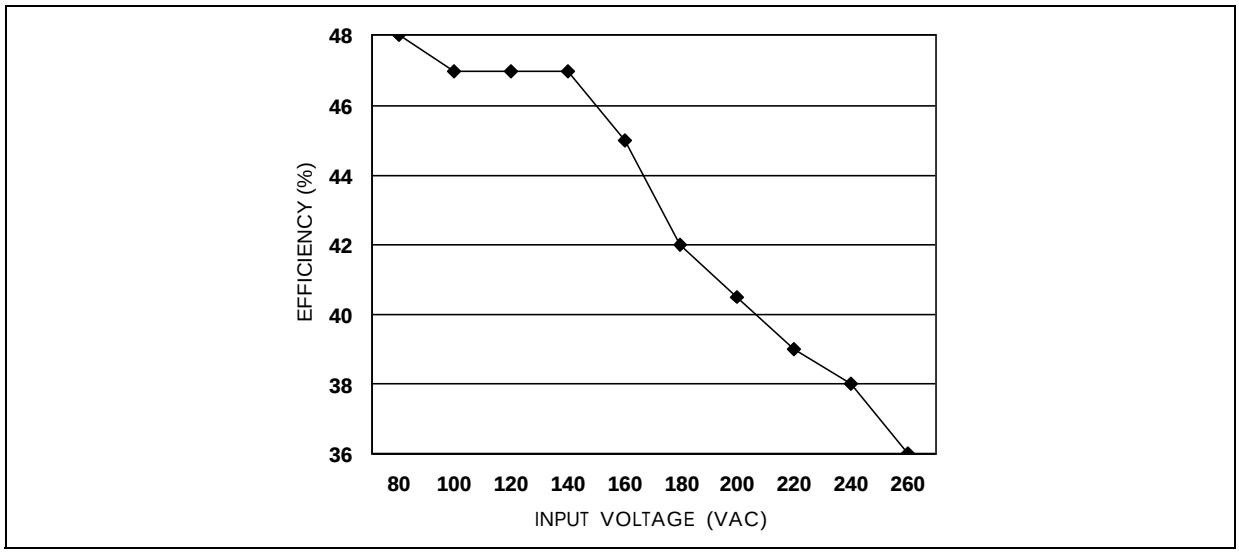
8. PERFORMANCE CONSIDERATIONS.

A three terminal regulator may be used for the lowest output noise and ripple. A 5V output produced directly can be used for the lowest input power but the output voltage regulation is worse with temperature. A low frequency of operation will reduce the input power and a higher frequency will reduce the size of the transformer. A lower leakage inductance transformer will allow a lower power snubber circuit to reduce the input power. A larger bulk capacitor or full bridge will reduce the input ripple voltage and allow operation at a lower input line or higher load.

9. COST CONSIDERATIONS.

A single rectifier can be used instead of an input bridge. Note that the input ripple voltage will be two times as much compared to the full bridge. Primary mode regulation can be used without a three terminal regulator for a greater than 5% regulation requirement. Primary mode regulation can be used with a standard three terminal regulator for 5% regulation. If good coupling and better regulation can be achieved, the input power can be reduced with a lower transformer output voltage for the three terminal regulator input voltage V'. The efficiency, in figure 6, is for the VIPer20 demo board for various input voltages at an input power of one Watt. Also, the efficiency divided by 100 is the output power for an input power of 1W.

Figure 6: Efficiency vs. Vin at Pin=1W



For various input voltages, the effeciency for the VIPer20 demoboard is 1W (see figure 6). Also, the effeciency divided by 100 is the output power for an input power of 1W.