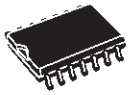
74LVX74

LOW VOLTAGE DUAL D-TYPE FLIP FLOP WITH PRESET AND CLEAR

- HIGH SPEED:
  f_{MAX} = 145 MHz (TYP.) at V_{CC} = 3.3V
- INPUT VOLTAGE LEVEL:
  V_{IL} = 0.8V, V_{IH} = 2V at V_{CC} = 3V
- LOW POWER DISSIPATION:
  I_{CC} = 2 µA (MAX.) at T_A = 25 °C
- LOW NOISE:
  V_{OLP} = 0.3 V (TYP.) at V_{CC} = 3.3V
- SYMMETRICAL OUTPUT IMPEDANCE:
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN)
- BALANCED PROPAGATION DELAYS:
  $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:
  V_{CC} (OPR) = 2V to 3.6V (1.2V Data Retention)
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 74
- IMPROVED LATCH-UP IMMUNITY
- POWER DOWN PROTECTION ON INPUTS



SOP

TSSOP

ORDER CODES		
PACKAGE	**TUBE**	**T & R**
SOP	74LVX74M	74LVX74MTR
TSSOP		74LVX74TTR

DESCRIPTION

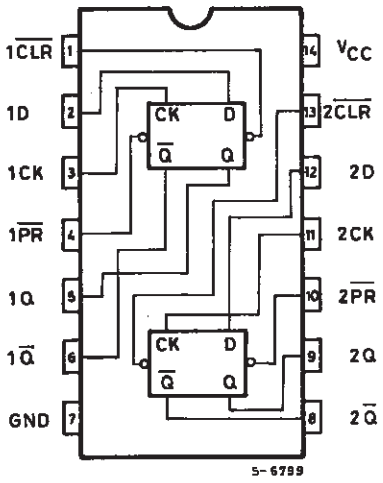
The 74LVX74 is a low voltage CMOS DUAL D-TYPE FLIP FLOP WITH PRESET AND CLEAR NON INVERTING fabricated with sub-micron silicon gate and double-layer metal wiring C^2MOS technology. It is ideal for low power and low noise 3.3V applications.

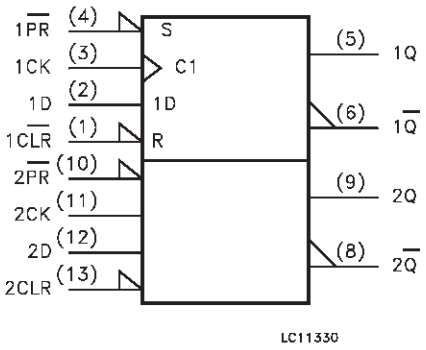
A signal on the D INPUT is transferred to the Q OUTPUT during the positive going transition of the clock pulse.

CLEAR and PRESET are independent of the clock and accomplished by a low setting on the appropriate input.

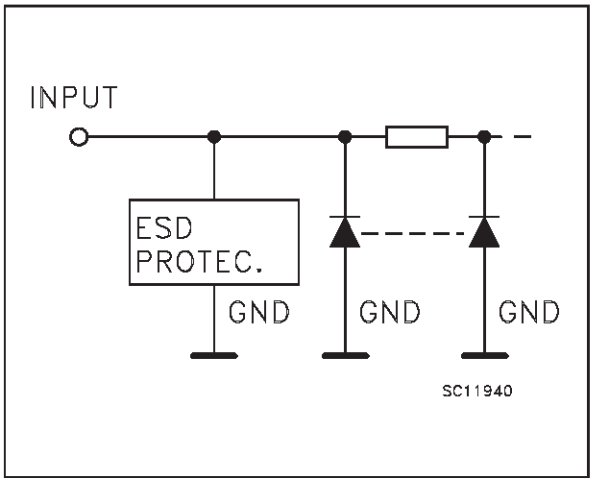
All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS





INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

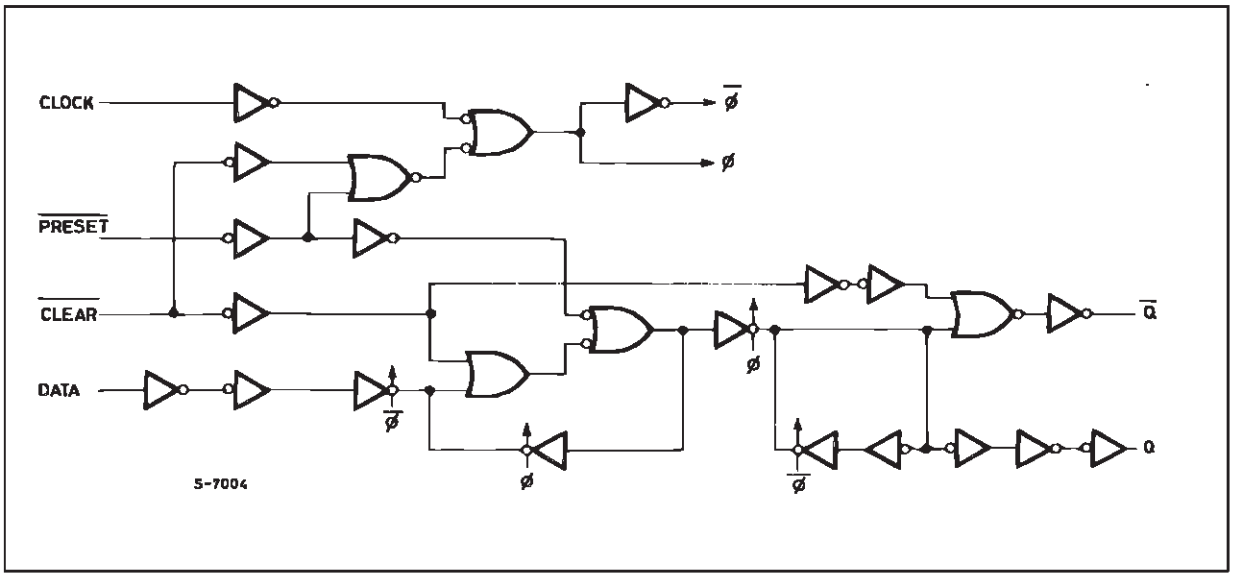
PIN No	SYMBOL	NAME AND FUNCTION
1, 13	$1\overline{CLR}$, $2\overline{CLR}$	Asyncronous Reset - Direct Inputs
2, 12	1D, 2D	Data Inputs
3, 11	1CK, 2CK	Clock Inputs (LOW-to-HIGH, Edge-Triggered)
4, 10	$1\overline{PR}$, $2\overline{PR}$	Asyncronous Set - Direct Inputs
5, 9	1Q, 2Q	True Flip-Flop Outputs
6, 8	$1\overline{Q}$, $2\overline{Q}$	Complement Flip-Flop Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

TRUTH TABLE

INPUTS				OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PR}$	D	CK	Q	$\overline{Q}$	
L	H	X	X	L	H	CLEAR
H	L	X	X	H	L	PRESET
L	L	X	X	H	H	
H	H	L	⌐	L	H	
H	H	H	⌐	H	L	
H	H	X	⌙	Q_n	$\overline{Q}_n$	NO CHANGE

X: Don't Care

LOGIC DIAGRAM



This logic diagram has not be used to esimate propagation delays

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7.0	V
V_I	DC Input Voltage	-0.5 to 7.0	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	-20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
T_{stg}	Storage Temperature	-65 to +150	^oC
T_L	Lead Temperature (10 sec)	300	^oC

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (note 1)	2 to 3.6	V
V_I	Input Voltage	0 to 5.5	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature:	-40 to +85	^oC
dt/dv	Input Rise and Fall Time (V_{CC} = 3V) (note 2)	0 to 100	ns/V

1) Truth Table guaranteed: 1.2V to 3.6V
2) V_{IN} from 0.8V to 2V

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions		Value					Unit
		V_{CC} (V)		T_A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0		1.5			1.5		V
		3.0		2.0			2.0		
		3.6		2.4			2.4		
V_{IL}	Low Level Input Voltage	2.0				0.5		0.5	V
		3.0				0.8		0.8	
		3.6				0.8		0.8	
V_{OH}	High Level Output Voltage	2.0	I_O=-50 µA	1.9	2.0		1.9		V
		3.0	I_O=-50 µA	2.9	3.0		2.9		
		3.0	I_O=-4 mA	2.58			2.48		
V_{OL}	Low Level Output Voltage	2.0	I_O=50 µA		0.0	0.1		0.1	V
		3.0	I_O=50 µA		0.0	0.1		0.1	
		3.0	I_O=4 mA			0.36		0.44	
I_I	Input Leakage Current	3.6	V_I = 5V or GND			±0.1		±1	µA
I_{CC}	Quiescent Supply Current	3.6	V_I = V_{CC} or GND			2		20	µA

DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Conditions		Value					Unit
		V_{CC} (V)		T_A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
V_{OLP}	Dynamic Low Voltage Quiet Output (note 1, 2)	3.3	C_L = 50 pF		0.3	0.5			V
V_{OLV}				-0.5	-0.3				
V_{IHD}	Dynamic High Voltage Input (note 1, 3)	3.3				2			
V_{ILD}	Dynamic Low Voltage Input (note 1, 3)	3.3		0.8					

1) Worst case package
2) Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V, (n -1) outputs switching and one output at GND
3) max number of data inputs (n) switching. (n-1) switching 0V to 3.3V. Inputs under test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}). f=1MHz

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3$ ns)

Symbol	Parameter	Test Condition			Value					Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time CK to Q or $\overline{Q}$	2.7	15			7.3	15.0	1.0	18.5	ns
		2.7	50			9.8	18.5	1.0	22.0	
		3.3(*)	15			5.7	9.7	1.0	11.5	
		3.3(*)	50			8.2	13.2	1.0	15.0	
t_{PLH} t_{PHL}	Propagation Delay Time $\overline{PR}$ or $\overline{CLR}$ to Q or $\overline{Q}$	2.7	15			8.4	15.6	1.0	18.5	ns
		2.7	50			10.9	19.1	1.0	22.0	
		3.3(*)	15			6.6	10.1	1.0	12.0	
		3.3(*)	50			9.1	13.6	1.0	15.5	
t_w	Minimum Pulse Width HIGH or LOW, CK	2.7	50				8.5		10.0	ns
		3.3(*)	50				6.0		7.0	
$t_{w(L)}$	Minimum Pulse Width LOW, $\overline{PR}$ or $\overline{CLR}$	2.7	50				8.5		10.0	ns
		3.3(*)	50				6.0		7.0	
t_s	Minimum Setup Time D to CK HIGH or LOW	2.7	50				8.0		9.5	ns
		3.3(*)	50				5.5		6.5	
t_h	Minimum Hold Time D to CK HIGH or LOW	2.7	50				0.5		0.5	ns
		3.3(*)	50				0.5		0.5	
t_{REM}	Minimum Removal Time $\overline{PR}$ or $\overline{CLR}$ to CK	2.7	50				6.5		7.5	ns
		3.3(*)	50				5.0		5.0	
f_{MAX}	Maximum Clock Frequency	2.7	15		55	135		50		MHz
		2.7	50		45	60		40		
		3.3(*)	15		95	145		80		
		3.3(*)	50		60	85		50		
t_{OSLH} t_{OSHL}	Output to Output Skew Time (note 1, 2)	2.7	50				1.5		1.5	ns
		3.3(*)	50				1.5		1.5	

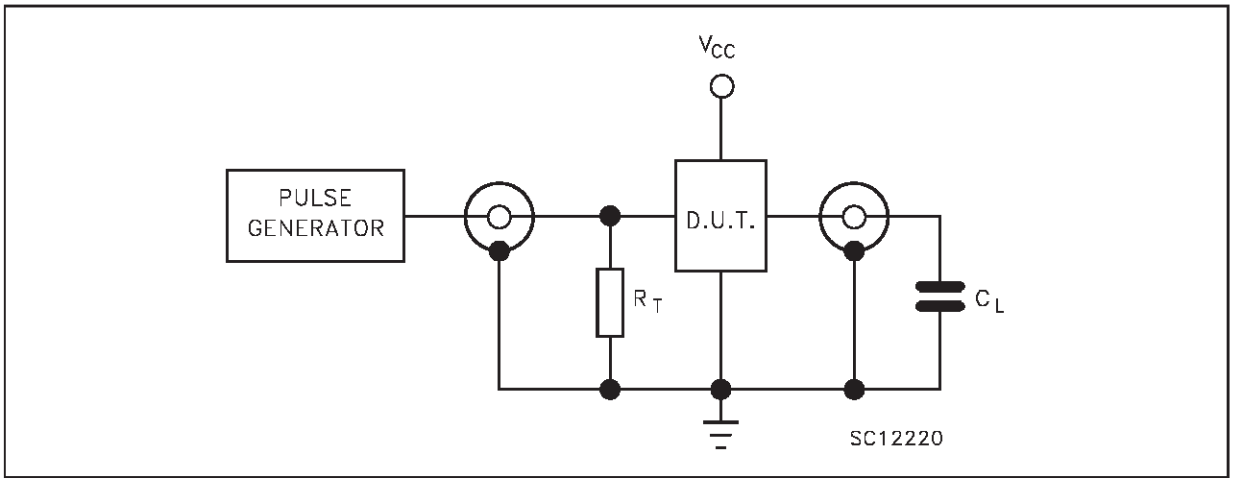
1) Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW
2) Parameter guaranteed by design
(*) Voltage range is 3.3V ± 0.3V

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions		Value					Unit
		V_{CC} (V)		T_A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
C_{IN}	Input Capacitance	3.3			4	10		10	pF
C_{PD}	Power Dissipation Capacitance (note 1)	3.3	f_{IN} = 10 MHz		25				pF

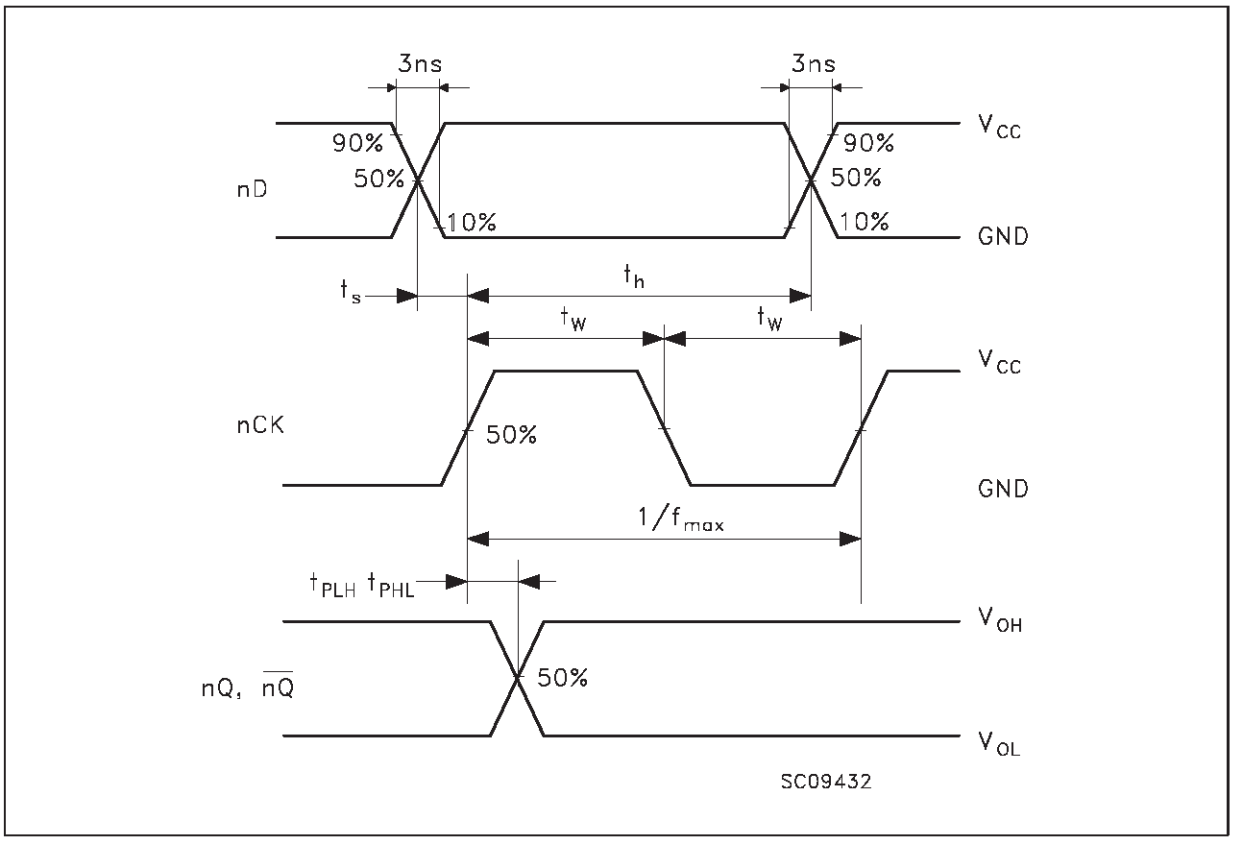
1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \bullet V_{CC} \bullet f_{IN} + I_{CC}/2$ (per circuit)

TEST CIRCUIT

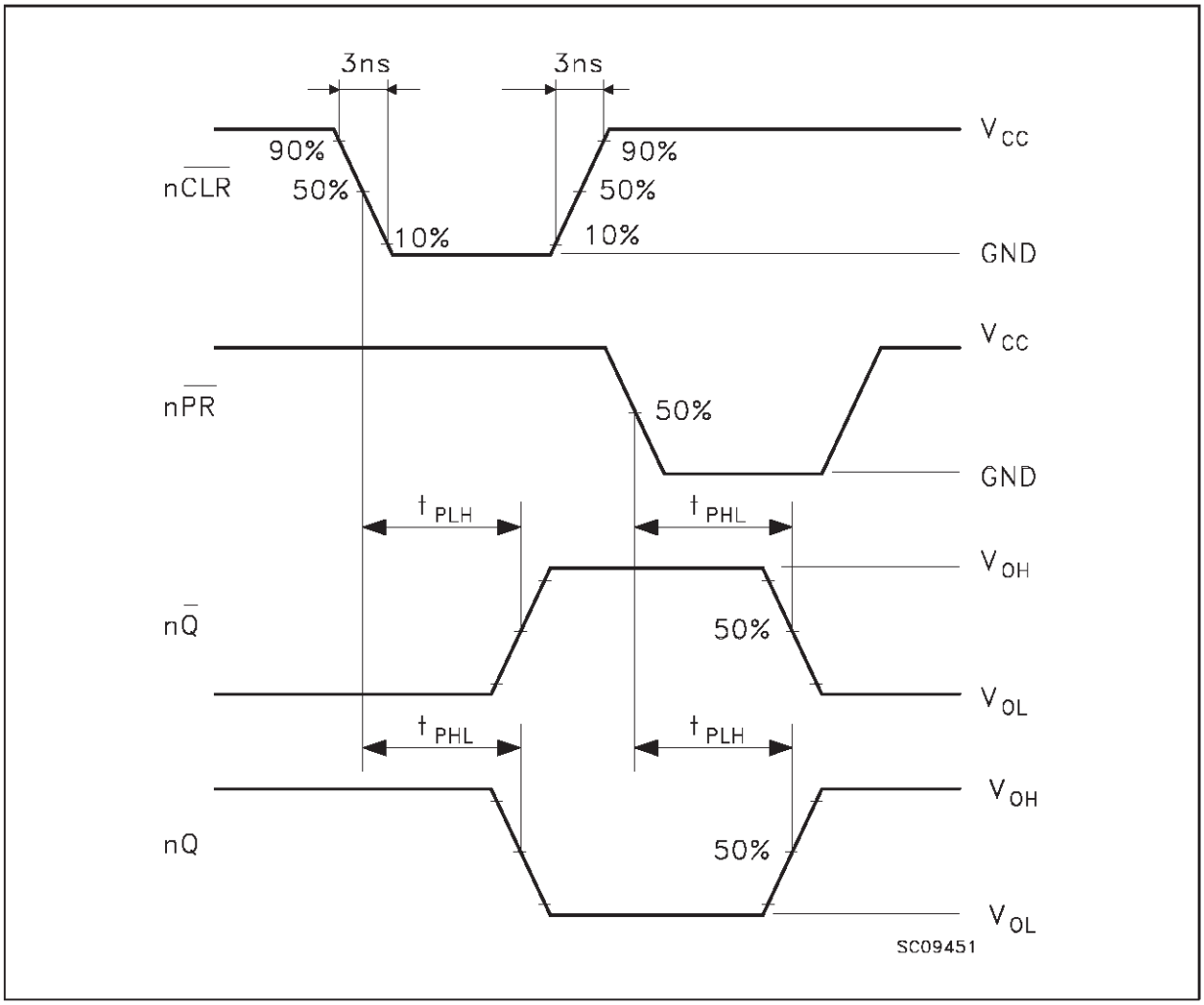


C_L = 15/50 pF or equivalent (includes jig and probe capacitance)
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

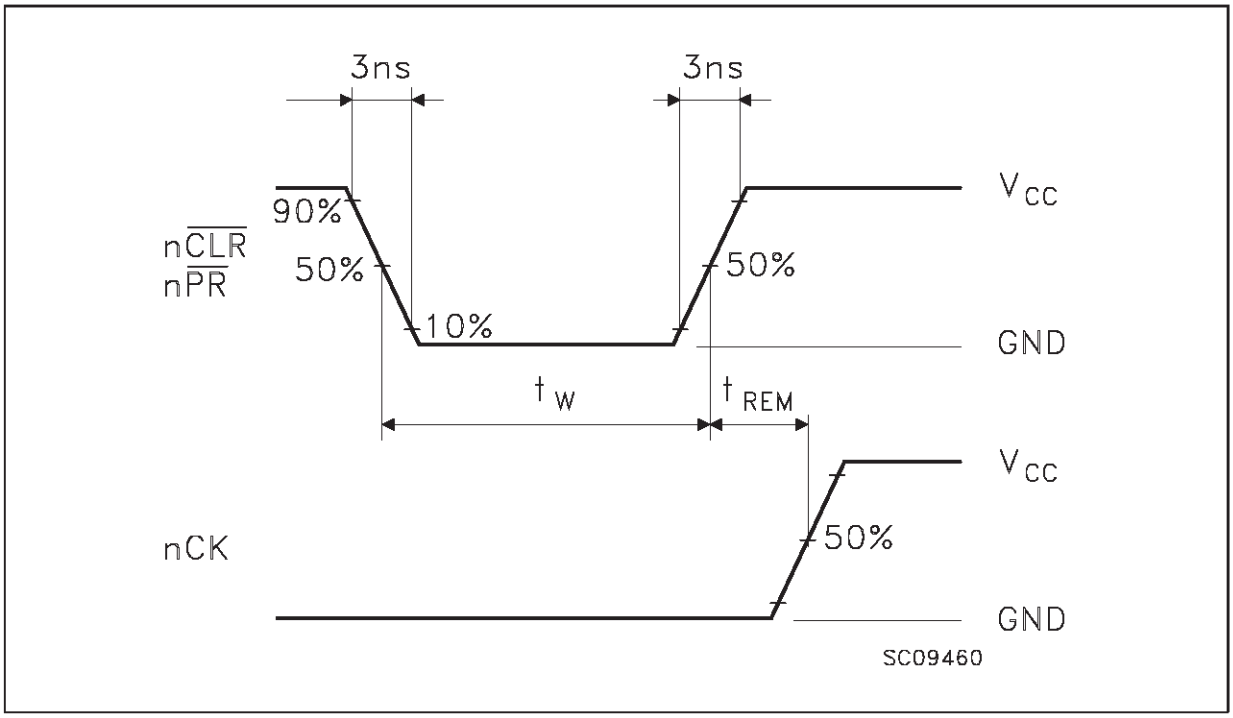
WAVEFORM 1: PROPAGATION DELAYS, SETUP AND HOLD TIMES (f=1MHz; 50% duty cycle)



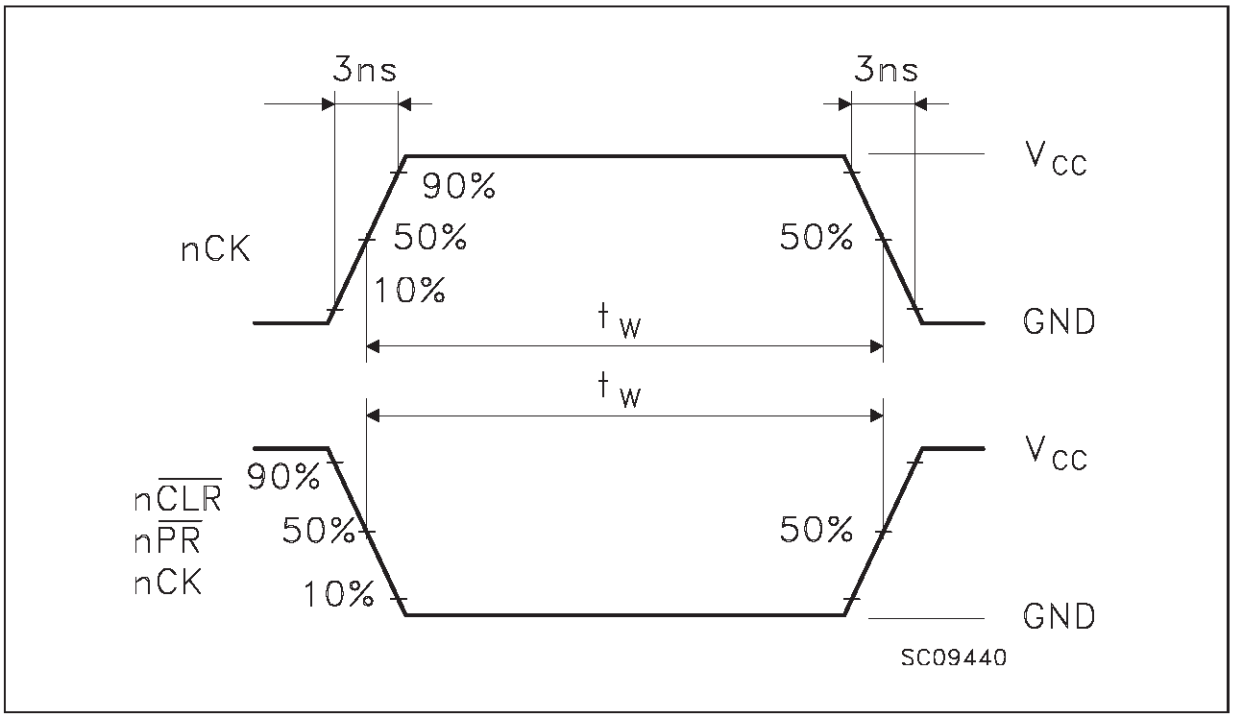
WAVEFORM 2: PROPAGATION DELAYS (f=1MHz; 50% duty cycle)



WAVEFORM 3: RECOVERY TIMES (f=1MHz; 50% duty cycle)

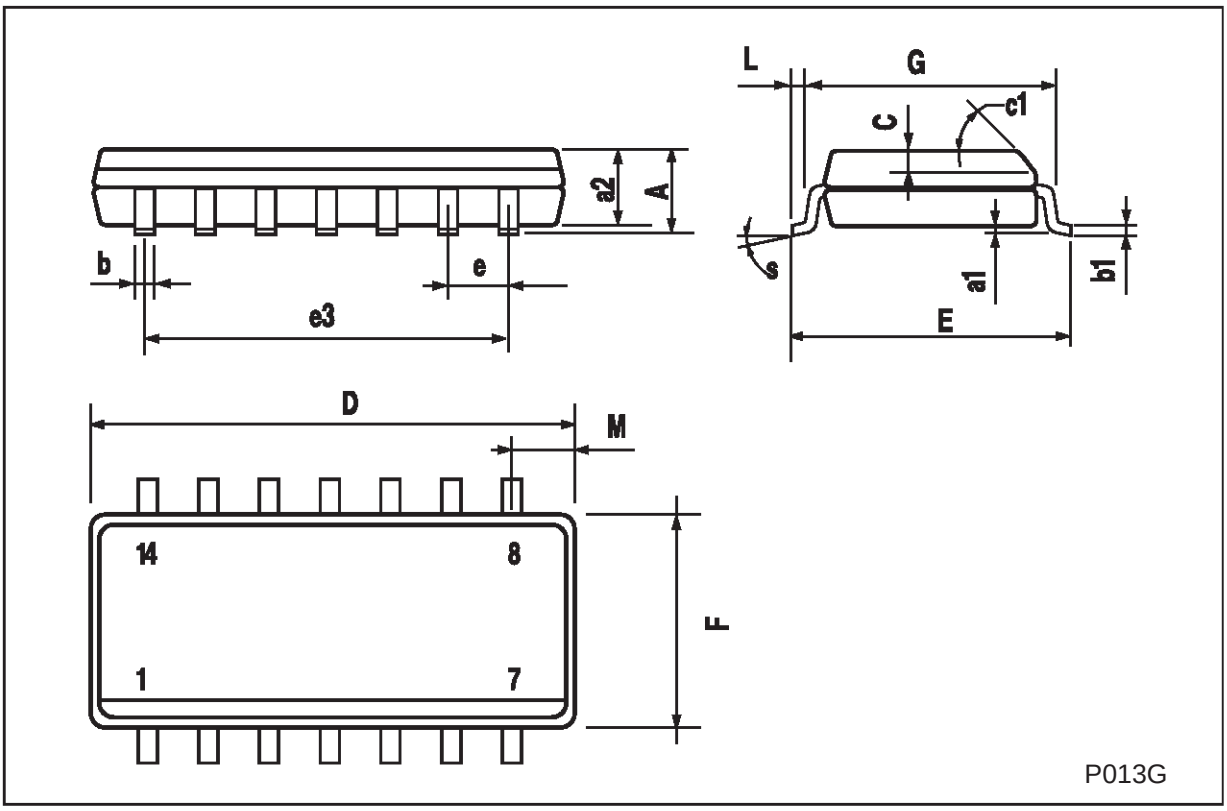


WAVEFORM 4: PULSE WIDTH



SO-14 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45 (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S	8 (max.)					



P013G

TSSOP14 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.1			0.433
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.85	0.9	0.95	0.335	0.354	0.374
b	0.19		0.30	0.0075		0.0118
c	0.09		0.20	0.0035		0.0079
D	4.9	5	5.1	0.193	0.197	0.201
E	6.25	6.4	6.5	0.246	0.252	0.256
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0^o	4^o	8^o	0^o	4^o	8^o
L	0.50	0.60	0.70	0.020	0.024	0.028