



## TDA9209

### 150 MHz PIXEL VIDEO CONTROLLER FOR MONITORS INCLUDING CUT-OFF INPUTS AND VIDEO DETECTION

#### FEATURE

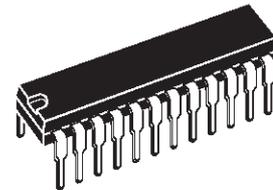
- 150 MHz PIXEL RATE
- 2.7 ns RISE AND FALL TIME
- I<sup>2</sup>C BUS CONTROLLED
- GREY SCALE TRACKING VERSUS BRIGHTNESS
- OSD MIXING
- NEGATIVE FEED-BACK FOR DC COUPLING APPLICATION
- INTERNAL POSITIVE FEED-BACK FOR LCD APPLICATION
- 0.5–4.5 V DACs FOR BLACK LEVEL RESTORATION (AC-COUPLING APPLICATION) OR CUT-OFF CONTROLS (FOR DC-COUPLING APPLICATION USING THE ST AMPLIFIERS TDA9533/9530)
- BEAM CURRENT ATTENUATION (ABL)
- PEDESTAL CLAMPING ON OUTPUT STAGE
- POSSIBILITY OF LIGHT OR DARK GREY OSD BACKGROUND
- OSD INDEPENDENT CONTRAST CONTROL
- ADJUSTABLE BANDWIDTH
- INPUT BLACK LEVEL CLAMPING WITH BUILT-IN CLAMPING PULSE
- STAND-BY MODE
- 5 V TO 8 V POWER SUPPLY
- VIDEO DETECTION

#### DESCRIPTION

The TDA9209 is an I<sup>2</sup>C Bus controlled RGB pre-amplifier designed for Monitor application, able to mix the RGB signals coming from any OSD device. The usual Contrast, Brightness, Drive and Cut-Off Controls are provided.

In addition, it includes the following features:

- OSD contrast,
- Bandwidth adjustment,
- Grey background,
- Internal back porch clamping pulse generator.



**SHRINK DIP24**  
(Shrink Plastic Package)

**ORDER CODE:** TDA9209

The RGB incoming signals are amplified and shaped to drive any commonly used video amplifiers without intermediate follower stages. Even though encapsulated in a 24-pin package only, this IC allows any kind of CRT Cathode coupling :

- AC coupling with DC restore,
- DC coupling with Feed-back from Cathodes,
- DC coupling with Cut-Off controls of the Video amplifier (ST Amplifiers TDA9533/9530).

As for any ST Video pre-amplifier, the TDA9209 is able to drive a real load without any external interface.

One of the main advantages of ST devices is their ability to sink and source currents while most of the devices from our competitors have problems to sink large currents.

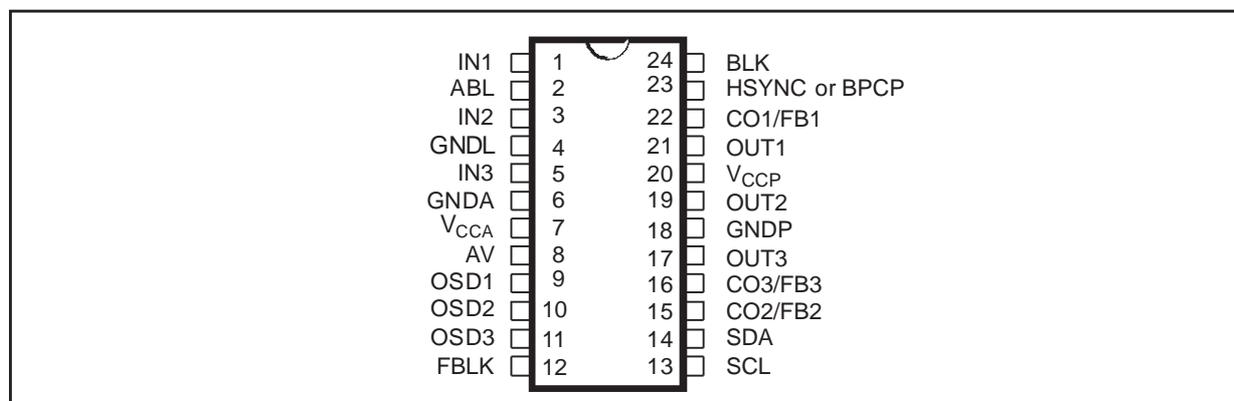
These driving capabilities combined with an original output stage structure suppress any static current on the output pins and therefore reduce dramatically the power dissipation of the device.

Extensive integration combined with high performance and advanced features make the TDA9209 one of the best choice for any CRT Monitor in the 14" to 17" range.

Perfectly matched with the ST Video Amplifiers TDA9530/33, these 2 products offer a complete solution for high performance and cost-optimized Video Board Application.

Version 4.4

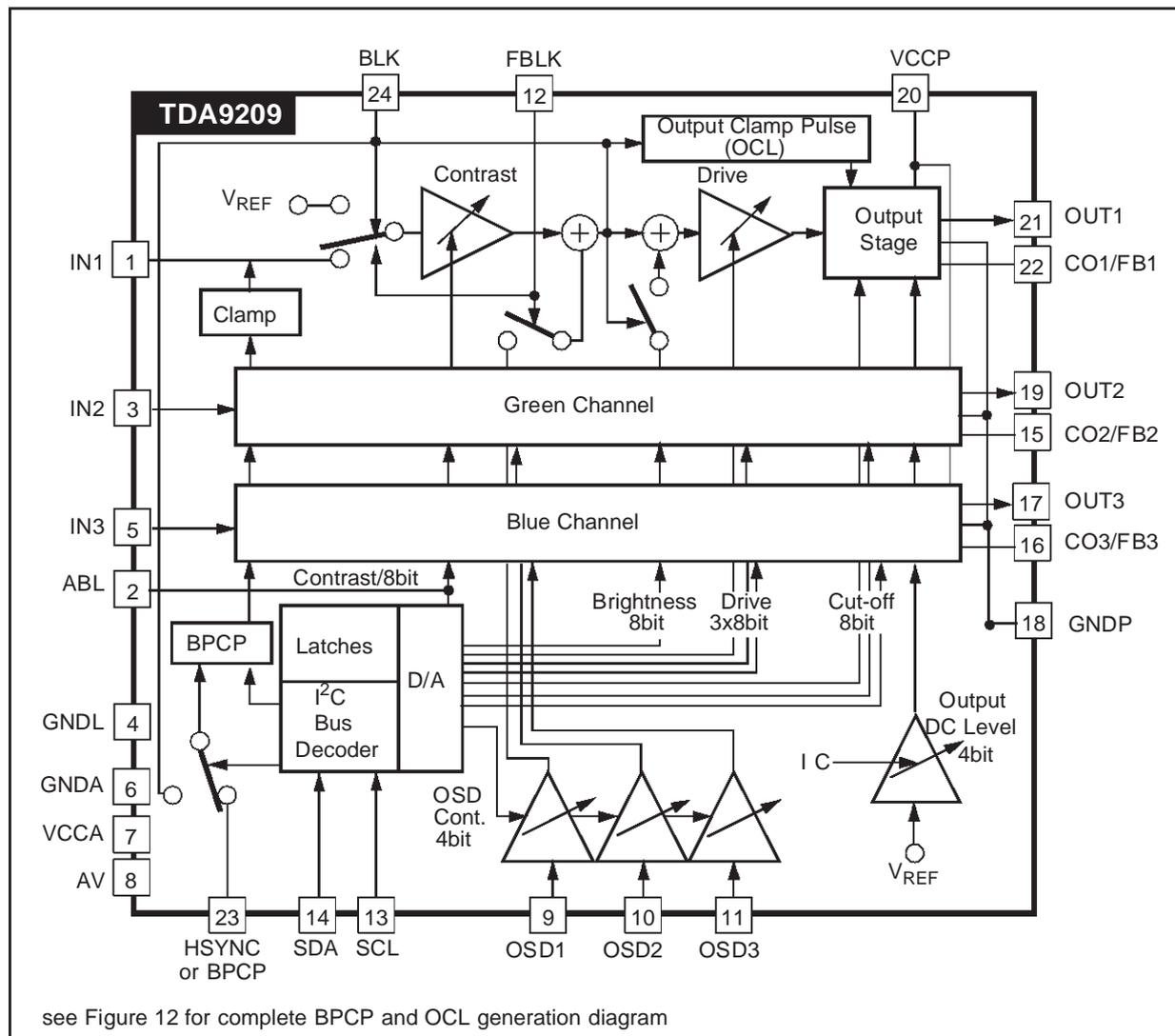
## 1 PIN CONNECTIONS



## 2 PIN DESCRIPTION

Pin Number	Symbol	Description
1	IN1	Red Video Input
2	ABL	ABL Input
3	IN2	Green Video Input
4	GNDL	Logic Ground
5	IN3	Blue Video Input
6	GNDA	Analog Ground
7	VCCA	Analog V <sub>CC</sub> (5V)
8	AV	Active Video Output
9	OSD1	Red OSD Input
10	OSD2	Green OSD Input
11	OSD3	Blue OSD Input
12	FBLK	Fast Blanking
13	SCL	SCL
14	SDA	SDA
15	CO2/FB2	Green Cut-off Output/Feedback Input
16	CO3/FB3	Blue Cut-off Output/Feedback Input
17	OUT3	Blue Video Output
18	GNDP	Power Ground
19	OUT2	Green Video Output
20	VCCP	Power V <sub>CC</sub> (5 V to 8 V)
21	OUT1	Red Video Output
22	CO1/FB1	Red Cut-off Output/Feedback Input
23	HSYNC/BPCP	HSYNC/BPCP
24	BLK	Blanking Input

### 3 BLOCK DIAGRAM



### 4 FUNCTIONAL DESCRIPTION

#### 4.1 RGB Input

The three RGB inputs have to be supplied through coupling capacitors (100 nF).

The maximum input peak-to-peak video amplitude is 1 V.

The input stage includes a clamping function. The clamp uses the input serial capacitor as a "memory capacitor".

To avoid a discharge of the serial capacitor during the line (due to leakage current), the input voltage is referenced to the ground.

The clamp is gated by an internally generated "Back Porch Clamping Pulse" (BPCP). Register 8 allows to choose the way to generate this BPCP (see Figure 1).

When bit 0 is set to 0, the BPCP is synchronized on the trailing or leading edge of HSYNC (Pin 23) (bit 1 = 0: trailing edge, bit 1 = 1: leading edge).

Additionally, the IC automatically works with either positive or negative HSYNC pulses.

- When bit 0 is set to 1, BPCP is synchronized on the leading edge of the blanking pulse BLK (Pin 24). One can use a positive or negative blanking pulse by programming bit 0 in Register 9 (See I<sup>2</sup>C Table 3).
- BPCP width can be adjusted with bit 2 and 3 (see Register 8, I<sup>2</sup>C table 2).
- If the application already provides the Back Porch Clamping Pulse, bit 4 must be set to 1 (providing a direct connection between Pin 23 and internal BPCP).

**4.2 Blanking Input**

The Blanking pin (FBLK) is TTL compatible.

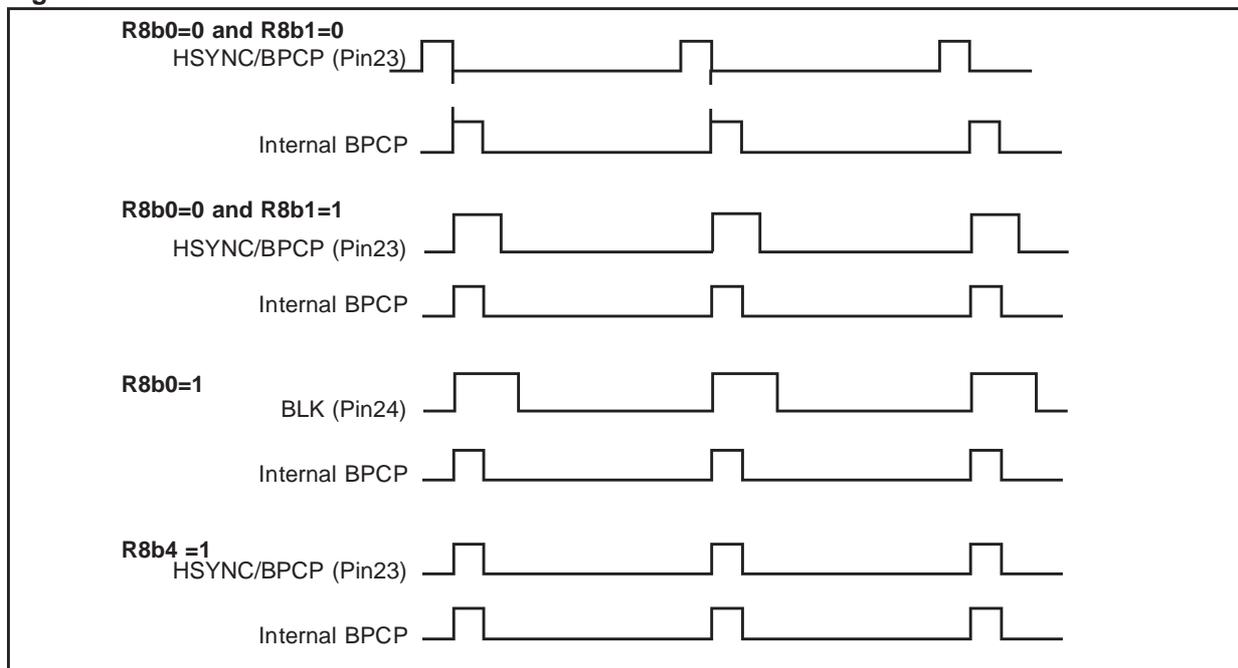
The Blanking pulse can be:

- positive or negative
- line or Composite-type (but not Frame-type).

**4.3 Contrast Adjustment (8 bit)**

The contrast adjustment is made by controlling simultaneously the gain of the three internal amplifiers through the I<sup>2</sup>C bus interface. Register 1 allows the adjustment in a range of 48 dB.

**Figure 1.**



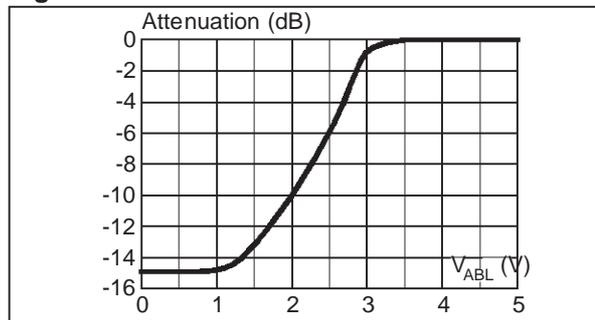
**4.4 ABL Control**

The TDA9209 includes an ABL (automatic beam limitation) input to attenuate the RGB Video signals depending on the beam intensity.

The operating range is 2 V (from 3 V to 1 V). A typical 15 dB maximum attenuation is applied to the output signal whatever the contrast adjustment is. (See Figure 2).

When the ABL feature is not used, the ABL input (Pin 2) must be connected to a 5 V supply voltage.

**Figure 2.**



#### 4.5 Brightness Adjustment (8 bit)

Brightness adjustment is controlled by the I<sup>2</sup>C Bus via Register 2. It consists of adding the same DC voltage to the three RGB signals, after contrast adjustment. When the blanking pulse equals 0, the DC voltage is set to a value which can be adjusted between 0 and 2V with 8mV steps (see Figure 3).

The DC output level is forced to the "Infra Black" level ( $V_{DC}$ ) when the blanking pulse is equal to 1.

#### 4.6 Drive Adjustment (3 x 8 bit)

In order to adjust the white balance, the TDA9209 offers the possibility of adjusting separately the overall gain of each channel thanks to the I<sup>2</sup>C bus (Registers 3, 4 and 5).

The very large drive adjustment range (48 dB) allows different standards or custom color temperatures.

It can also be used to adjust the output voltages at the optimum amplitude to drive the CRT drivers, keeping the whole contrast control for the end-user only.

The drive adjustment is located after the Contrast, Brightness and OSD switch blocks, so it does not affect the white balance setting when the BRT is adjusted. It also operates on the OSD portion of the signal.

#### 4.7 Cut-off Adjustment (Infra Black)

The cut-off voltage (Infra Black:  $V_{DC}$ ) is the level of the output during the blanking period. This level is sampled after each line during an internal pulse (OCL) generated during the blanking pulse (see Figure 11).

A sample-and-hold block controls the  $V_{DC}$  level.

In case of AC coupling application,  $V_{DC}$  is adjustable simultaneously on the 3 channels from 0.4 to 2.5V via the 4-bit DCL register (register 6, see Table 1 on page 15).

In case of DC coupling,  $V_{DC}$  is adjustable separately for each channel from 0.2 to 2.5V via the 8-bit cut-off registers (registers 10, 11 and 12, see Table 1 on page 15).

#### Caution:

Register 6: out of the 0 to 15 cut-off adjustment steps, the first 3 steps are not allowed.

Registers 10, 11 and 12: out of the 0 to 256 cut-off adjustment steps, the first 40 steps are not allowed.

#### 4.8 OSD Inputs

The TDA9209 allows to mix the OSD signals into the RGB main picture. The four pins dedicated to this function are the following:

- Three TTL RGB inputs (Pins 9, 10, 11) connected to the three outputs of the corresponding OSD processor.
- One TTL fast blanking input (Pin 12) also connected to the FBLK output of the OSD processor.

When a high level is present on the FBLK, the IC acts as follows:

- The three main picture RGB input signals (IN1, IN2, IN3) are internally switched to the internal input clamp reference voltage.
- The three output signals are set to the voltage corresponding to the three OSD input logic states (0 or 1). (See Figure 3).

If the OSD input is at low level, the output and brightness voltages ( $V_{BRT}$ ) are equal.

If the OSD input is at high level, the output voltage is  $V_{OSD}$ , where  $V_{OSD} = V_{BRT} + OSD$  and OSD is an I<sup>2</sup>C bus-controlled voltage.

OSD varies between 0 V to 4.9 V by 320 mV steps via Register 7 (4 bit). The same variation is applied simultaneously to the three channels providing the OSD contrast.

The grey color can be obtained on output signals when:

- OSD1 = 1, OSD2 = 0 and OSD3 = 1,
- A special bit (bit 5 or 6) in Register 9 is set to 1.

If R9b5 is set to 1, light grey is obtained on output.

If R9b6 is set to 1, dark grey is obtained on output.

In the case where R9b5 and R9b6 are set to 0, the normal operation is provided on output signals.

**4.9 Output Stage**

The overall waveforms of the output signal are shown in Figure 3. The three output stages, which are large bandwidth output amplifiers, are able to deliver up to 4.4 V<sub>PP</sub> for 0.7 V<sub>PP</sub> on input.

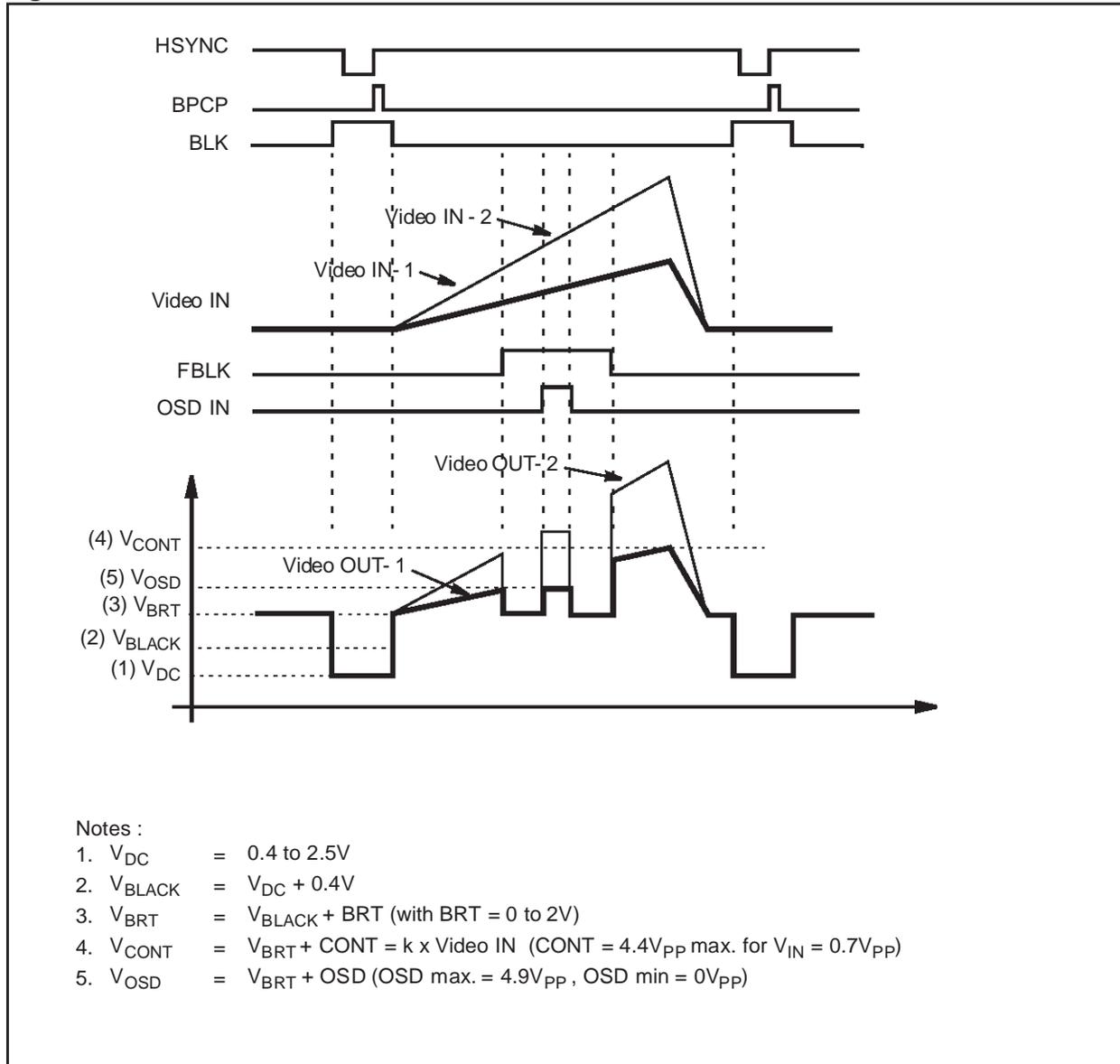
When a high level is applied on the BLK input (Pin 24), the three outputs are forced to "Infra

Black" level (V<sub>DC</sub>) thanks to a sample and hold circuit (described below).

The black level (which is the output voltage outside the blanking pulse with minimum brightness and no Video input signals) is 400 mV higher than V<sub>DC</sub>.

The brightness level (V<sub>BRT</sub>) is then obtained by programming register 2 (see Table 1 on page 15).

**Figure 3. Waveforms VOUT, BRT, CONT, OSD**



#### 4.10 Bandwidth Adjustment

An advanced feature: Bandwidth adjustment, is implemented on the TDA9209.

For applications where rise/fall time  $>5.5\text{ns}$ , this feature must not be used and the bandwidth has to be set to 0 (dec) (register 13, see Table 1 on page 15).

For applications where rise/fall time  $<5.5\text{ns}$ , this feature offers several advantages:

- Depending on the external capacitive load and on the peak-to-peak output voltage, this adjustment avoids getting any slew-rate phenomenon.
- Electromagnetic radiation (EMI). Slowing down the signal of rise/fall time will decrease the EMI without significantly deteriorating the rise/fall time of the CRT driver.
- Video signal response. Using this adjustment will allow to optimize the high frequency transient phenomena.
- Still picture mode. In this mode, high video swing is of greater interest than rise/fall time. The bandwidth adjustment can be used to avoid any slew-rate phenomenon at the CRT driver output and to reduce EMI.

#### 4.11 CRT Cathode Coupling

The powerful multiplex capability of the TDA9209 allows to use the device with several kinds of CRT cathode coupling.

##### AC coupling with DC restore (Figure 4)

In this mode the output DC level ( $V_{DC}$ ) is adjusted simultaneously for the 3 channels from 0.5 V to 2.35 V via Register 6 (4 bit). The cut-off voltage is programmed independently for each channel from

0.17 V to 4.6 V using registers 10, 11, 12 (8 bit each, see Table 1 on page 15).

##### DC Coupling with cut-off controls on Video Amplifier (with TDA9533/ 9530, Figure 5)

The functioning and programming of the TDA9209 are the same as for the previous mode, except for the cut-off control which is now performed via the Video amplifier cut-off input .

In AC coupling and DC coupling with cut-off control, bit 2, 3 and 4 in Register 9 must be set to 1.

##### DC Coupling Mode (Figure 6)

This is the most commonly used configuration enabling to build a powerful video system on a small PCB Board and giving a substantial cost saving compared with any other solution available on the market.

The preamplifier outputs control directly the cut-off levels.

The output DC level ( $V_{DC}$ ) is adjusted independently for each channel from 0.5 V to 2.5 V via registers 10, 11 and 12.

In DC coupling mode, bit 2 must be set to 1 and bit3 to 0 in Register 9.

##### DC Coupling with feedback mode (Figure 7)

In this mode, the feedback voltage issued from the cathode is sent to the TDA9209. This voltage is compared to a reference from the cut-off DC level DAC by the sample and hold circuit who also controls the DC voltage of the feedback input in a range of 0.5 V to 2.5 V.

Each channel is independently controlled via Registers 10, 11 and 12.

In DC coupling with feedback mode, bit 2 and bit 4 must be set to 0 in Register 9.

Figure 4. AC Coupling

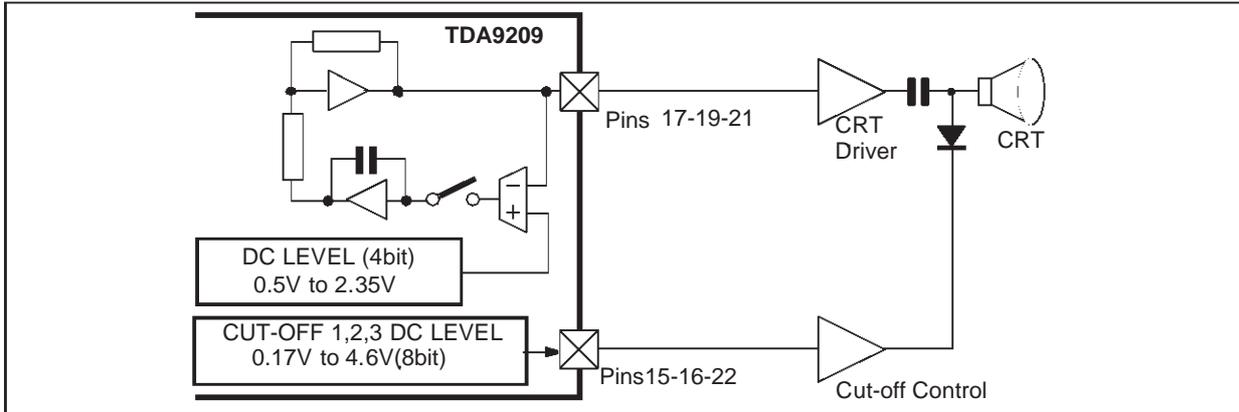


Figure 5. DC Coupling with Cut-off Control

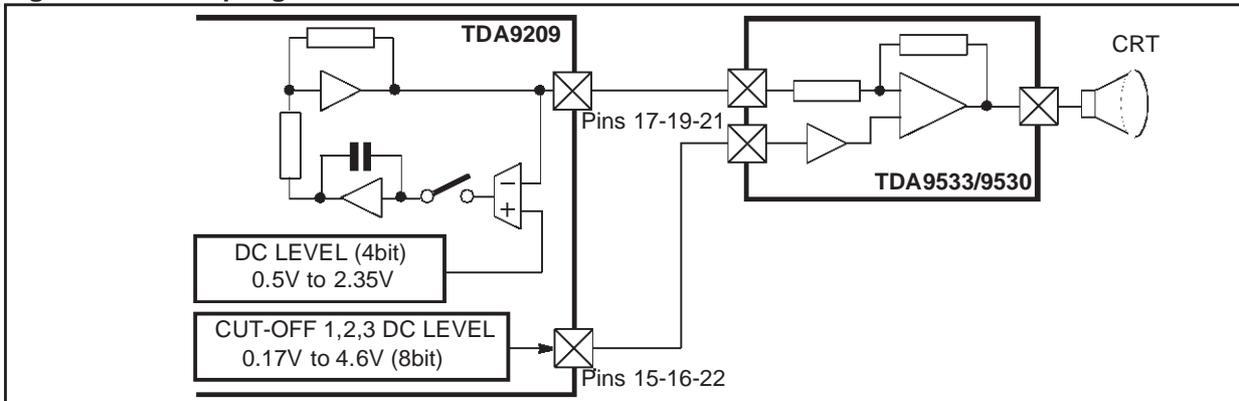


Figure 6. DC Coupling

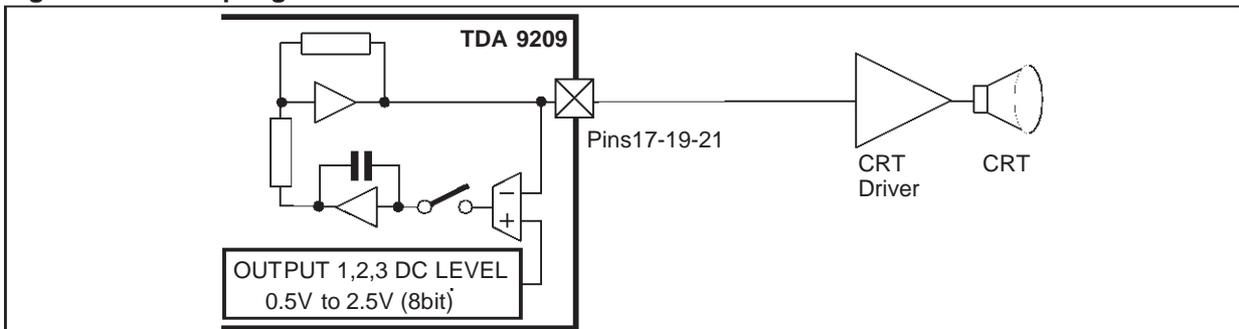
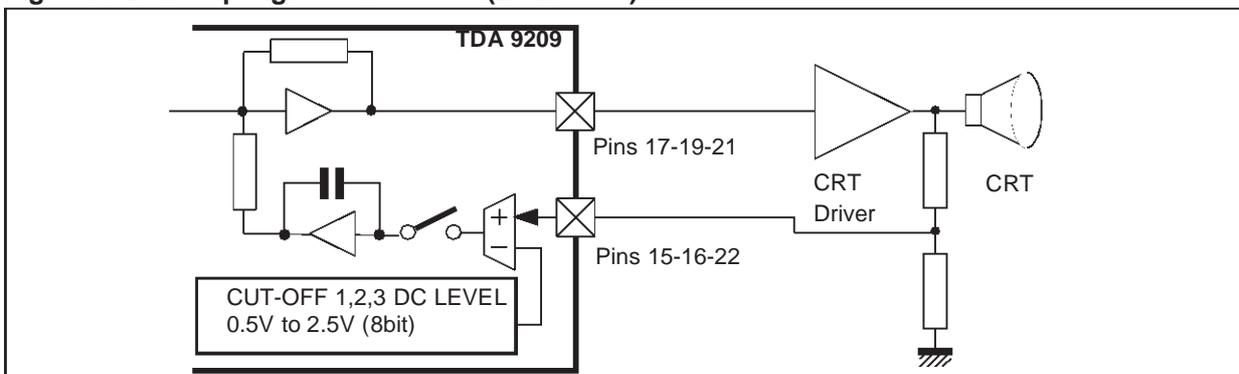


Figure 7. DC Coupling with Feedback (LCD mode)



### 4.12 Stand-by Mode

The TDA9209 has a stand-by mode. As soon as the  $V_{CC}$  power (Pin 20) gets lower than 3V (typ.), the device is set in stand-by mode whatever the voltage on analog  $V_{CCA}$  (Pin 7) is. The analog blocks are internally switched-off while the logic parts (I<sup>2</sup>C bus, power-on reset) are still supplied.

In stand-by mode, the power consumption is below 20 mW.

### 4.13 Serial Interface

The 2-wire serial interface is an I<sup>2</sup>C interface. The slave address of TDA9209 is DC hex.

A6	A5	A4	A3	A2	A1	A0	W
1	1	0	1	1	1	0	0

The host MCU can write into the TDA9209 registers. Read mode is not available.

In order to write data into the TDA9209, after the “start” message, the MCU must send the following data (see Figure 8):

- the I<sup>2</sup>C address slave byte with a low level for the R/W bit,
- the byte to the internal register address where the MCU wants to write data,
- the data.

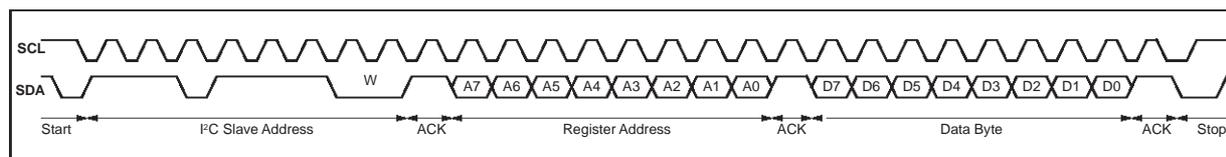
All bytes are sent with MSB bit first. The transfer of written data is ended with a “stop” message.

When transmitting several data, the register addresses and data can be written with no need to repeat the start and slave addresses.

### 4.14 Power-on Reset

A power-on reset function is implemented on the TDA9209 so that the I<sup>2</sup>C registers have a determined status after power-on. The Power-on reset threshold for a rising supply on  $V_{CCA}$  (Pin 7) is 3.8 V (typ.) and 3.2V when the  $V_{CC}$  decreases.

Figure 8. I<sup>2</sup>C Write Operation



### 4.15 Video detection (see Figure 9)

The video detection consists of three fast comparators and a OR function.

The positive input of each comparator is connected to the input video pin (R, G, or B).

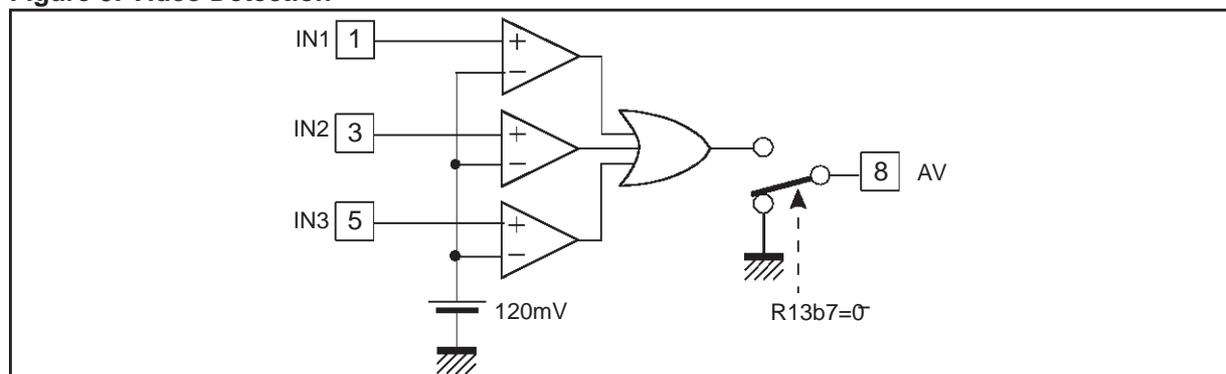
The negative inputs are connected together to a reference voltage. This voltage is the threshold of the comparators. The typical threshold voltage is 120 mV. The three comparator outputs are con-

nected to the OR inputs. Active Video output can be inhibited by using bit 7 in Register 13 :

- R13b7 = 0                      AV inhibited
- R13b7 = 1                      AV validated

When AV output is validated, the AV output reaches 5V when at least one of the 3 video inputs gets higher than 3.8V (typ.), and decreases to 0V if the 3 input voltages get lower than 3.2V (typ.).

Figure 9. Video Detection



### 4.16 Specific Application Conditions

#### Functioning with 5 V Power $V_{CC}$

To simplify the application, it is possible to supply the power  $V_{CC}$  with 5 V (instead of 8 V nominal) at the expense of output swing voltage.

#### Functioning without Blanking Pulse

If no blanking pulse is applied to the TDA9209, the internal BPCP can be connected to the sample and hold circuit (Register 8, bit 7 = 1 and BLK pin grounded) so that the output DC level is still controlled by I<sup>2</sup>C.

To ensure the device correct behavior in the worst possible conditions, the Brightness Register must be set to 0.

## 5 ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Pin	Value	Units
$V_{CCA}$ Max.	Supply Voltage on Analog $V_{CC}$	7	5.5	V
$V_{CCP}$ Max.	Supply Voltage on Power $V_{CC}$	20	8.8	V
$V_{in}$ Max.	Voltage at any Input Pins (except Video inputs) and Input/Output Pins	-	5.5	V
$V_I$ Max.	Voltage at Video Inputs	1, 3, 5	1.4	V
$T_{stg}$	Storage Temperature	-	-	°C
$T_{oper}$	Operating Junction Temperature	-	+150	°C

## 6 THERMAL DATA

Symbol	Parameter	Value	Units
$R_{th(j-a)}$	Max. Junction-ambient Thermal Resistance	69	°C/W
$T_j$	Typ. Junction Temperature at $T_{amb} = 25^\circ\text{C}$	80	°C

## 7 DC ELECTRICAL CHARACTERISTICS

$T_{amb} = 25^\circ\text{C}$ ,  $V_{CCA} = 5\text{V}$ ,  $V_{CCP} = 8\text{V}$ , unless otherwise specified.

Symbol	Parameter	Test Condition s	Min.	Typ.	Max.	Units
$V_{CCA}$	Analog Supply Voltage	Pin 7	4.5	5	5.5	V
$V_{CCP}$	Power Supply Voltage	Pin 20	4.5	8	8.8	V
$I_{CCA}$	Analog Supply Current	$V_{CCA} = 5\text{V}$		70		mA
$I_{CCP}$	Power Supply Current	$V_{CCP} = 8\text{V}$		55		mA
$V_I$	Video Input Voltage Amplitude			0.7	1	V
$V_o$	Output Voltage Range		0.5		$V_{CCP} - 0.5$	V
$V_{IL}$	Low Level Input Voltage	OSD, FBLK, BLK, HSYNC			0.8	V
$V_{IH}$	High Level Input Voltage		2.4			V
$I_{IN}$	Input Current	OSD, FBLK, BLK	-1		1	μA
$R_{HS}$	Input Resistor	HSYNC		40		kΩ

## 8 AC ELECTRICAL CHARACTERISTICS

$T_{amb} = 25^{\circ}\text{C}$ ,  $V_{CCA} = 5\text{V}$ ,  $V_{CCP} = 8\text{V}$ ,  $V_i = 0.7 V_{PP}$ ,  $C_{LOAD} = 5\text{pF}$   
 $R_S = 100\Omega$ , serial between output pin and  $C_{LOAD}$ , unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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### VIDEO INPUTS (PINS 1, 3, 5)

$V_i$	Video Input Voltage Amplitude	Max. Contrast and Drive		0.7	1	V
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### VIDEO OUTPUT SIGNAL (PINS 17, 19, 21) - GENERAL

GAM	Maximum Gain	Max Contrast and Drive (CRT = DRV = 254 dec)		16		dB
VOM	Maximum Video Output Voltage (Note 1)	Max Contrast and Drive (CRT = DRV = 254 dec)		4.4		V
VON	Nominal Video Output Voltage	Contrast and Drive at POR (CRT = DRV = 180 dec)		2.2		V
CAR	Contrast Attenuation Range	From max. Contrast (CRT=254 dec) to min. Contrast (CRT = 1 dec)		48		dB
DAR	Drive Attenuation Range	From Max. Drive (DRV = 254 dec) to min Drive (DRV = 1 dec)		48		dB
GM	Gain Matching	Contrast and Drive at POR		$\pm 0.1$		dB
$t_R, t_F$	Rise Time, Fall Time (Note 1)	$V_{OUT} = 2 V_{PP}$ (BW = 15 dec) $V_{OUT} = 2 V_{PP}$ (BW = 0 dec)		2.7 4.3		ns ns
BW	Large Signal Bandwidth	$V_{OUT} = 2 V_{PP}$		130		MHz
BW	Bandwidth Adjustment Range	$V_{OUT} = 2 V_{PP}$ Minimum bandwidth (BW = 0 dec) Maximum bandwidth (BW = 15 dec)		80 130		MHz MHz
CT	Crosstalk between Video Outputs	$V_{OUT} = 2 V_{PP}$ @ f = 10 MHz @ f = 50 MHz		60 35		dB dB

### VIDEO OUTPUT SIGNAL — BRIGHTNESS

BRTmax	Maximum Brightness Level	Max. Brightness (BRT = 255 dec) and Max. Drive (DRV = 254 dec)		2		V
BRTmin	Minimum Brightness Level	Min. Brightness (BRT = 0 dec) and Max. Drive (DRV = 254 dec)		0		V
VIP	Insertion Pulse			0.4		V
BRTM	Brightness Matching	Brightness and Drive at POR		$\pm 10$		mV

### VIDEO OUTPUT SIGNAL — OSD

OSDmax	Maximum OSD Output Level	Max. Drive (DRV = 254 dec) Max. OSD (OSD = 15 dec)		4.9		V
OSDmin	Minimum OSD Output Level	Min. OSD (OSD = 0 dec)		0		V

### VIDEO OUTPUT SIGNAL — DC LEVEL (AC COUPLING MODE)

DCLmax	Maximum Output DC Level	Max. DCL (DCL= 15 dec)		2.35		V
DCLmin	Minimum Output DC Level	Min. DCL (DCL = 3 dec)		0.5		V
DCLstep	Output DC Level Step			155		mV

### VIDEO OUTPUT SIGNAL — DC LEVEL (DC COUPLING MODE)

DCLmax	Maximum Output DC Level	Max. Cut-off (Cut-off = 255 dec)		2.5		V
DCLmin	Minimum Output DC Level	Min. Cut-off (Cut-off = 40 dec)		0.4		V
DCLstep	Output DC Level Step			10		mV

**Note 1:** Assuming that  $V_{OM}$  remains within the range of  $V_o$  (between 0.5V and  $V_{CCP} - 0.5V$ )  
 $t_R, t_F$  are calculated values, assuming an ideal input rise/fall time of 0ns ( $t_R = \sqrt{t_{ROUT}^2 + t_{RIN}^2}$ ,  $t_F = \sqrt{t_{FOUT}^2 + t_{FIN}^2}$ )

**AC ELECTRICAL CHARACTERISTICS (continued)**

$T_{amb} = 25^{\circ}\text{C}$ ,  $V_{CCA} = 5\text{V}$ ,  $V_{CCP} = 8\text{V}$ ,  $V_i = 0.7 V_{PP}$ ,  $C_{LOAD} = 5 \text{ pF}$ , unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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**CUT-OFF OUTPUTS (AC COUPLING MODE) - (Pins 15, 16, 22)**

COmax	Maximum Cut-off Output Level	Max. Cut-off (Cut-off = 255 dec) and Sourced Current = 200 $\mu\text{A}$		4.7		V
COmin	Minimum Cut-off Output Level	Min. Cut-off (Cut-off = 0 dec) and Sunked Current = 2mA		0.1		V
COTD	Cut-off Output Voltage Drift	$T_j$ Variation = 100 $^{\circ}\text{C}$		0.5		%
COHlin	Maximum Cut-off Output Voltage (linear region)	Cut-off = 235dec (Sourced Current = 200 $\mu\text{A}$ )		4.6		V
COLlin	Minimum Cut-off Output Voltage (linear region)	Cut-off = 10 dec (Sunked current = 2mA)		0.17		V
COstep	Cut-off Output Step (linear region)			20		mV

**FEEDBACK INPUTS (DC WITH FEEDBACK MODE)**

VFBmax	Controlled Feedback Input Level Maximum	Max. Cut-off (Cut-off = 255 dec)		2.5		V
VFBmin	Controlled Feedback Input Level Minimum	Min. Cut-off (Cut-off = 1 dec)		20		mV
VFBstep	Controlled Feedback Input Level Step			10		mV
IFB	input Current on Feedback inputs	$V \leq 2.5\text{V}$		50		$\mu\text{A}$

**ABL (PIN 2)**

GABLmin	ABL Mini Attenuation	$V_{ABL} \geq 3.2 \text{ V}$		0		dB
GABLmax	ABL Maxi Attenuation	$V_{ABL} = 1 \text{ V}$		15		dB
$V_{ABL}$	ABL Threshold Voltage	For output attenuation		3		V
IABLhigh	High ABL Input Current	$V_{ABL} = 3.2\text{V}$		0		$\mu\text{A}$
IABLlow	Low ABL Input Current	$V_{ABL} = 1\text{V}$		-2		$\mu\text{A}$

**VIDEO DETECTION**

VTHAV	Comparator Threshold			120		mV
DELAY	Delay between Video Output and AV output	3pF load on AV out (Pin8)		10		ns
PixAV	Minimum pixel width	$V_{in} = 0.7V_{PP}$		10		ns

## 9 I<sup>2</sup>C ELECTRICAL CHARACTERISTICS

$T_{amb} = 25^{\circ}\text{C}$ ,  $V_{CCA} = 5\text{V}$ , unless otherwise specified

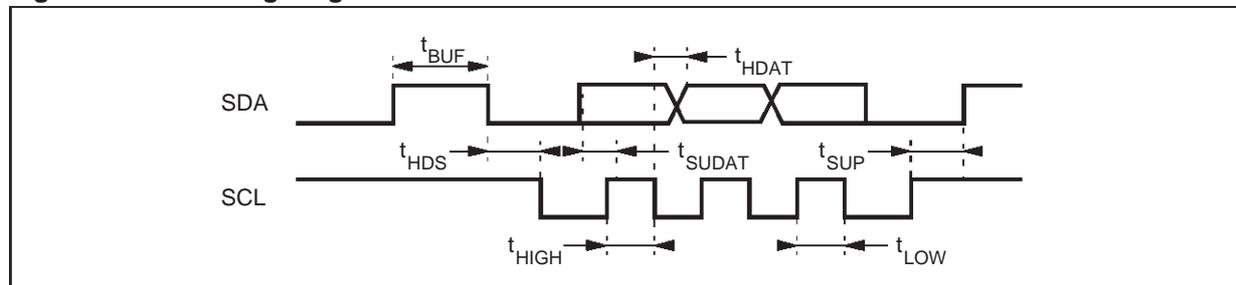
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$V_{IL}$	Low Level Input Voltage	On Pins SDA, SCL			1.5	V
$V_{IH}$	High Level Input Voltage		3			V
$I_{IN}$	Input Current (Pins SDA, SCL)	$0.4\text{ V} < V_{IN} < 4.5\text{ V}$	-10		+10	$\mu\text{A}$
$f_{SCL(\text{Max.})}$	SCL Maximum Clock Frequency		200		0.25	kHz
$V_{OL}$	Low Level Output Voltage	SDA Pin when ACK Sink Current = 6mA			0.6	V

## 10 I<sup>2</sup>C INTERFACE TIMING REQUIREMENTS

(see Figure 11)

Symbol	Parameter	Min.	Typ.	Max.	Units
$t_{BUF}$	Time the bus must be free between two accesses	1300			ns
$t_{HDS}$	Hold Time for Start Condition	600			ns
$t_{SUP}$	Set-up Time for Stop Condition	600			ns
$t_{LOW}$	The Low Period of Clock	1300			ns
$t_{HIGH}$	The High Period of Clock	600			ns
$t_{HDAT}$	Hold Time Data	300			ns
$t_{SUDAT}$	Set-up Time Data	250			ns
$t_R, t_F$	Rise and Fall Time of both SDA and SCL	20		300	ns

Figure 10. I<sup>2</sup>C Timing Diagram



## 11 I<sup>2</sup>C REGISTER DESCRIPTION

**Table 1. Register Sub-addressed - I<sup>2</sup>C Table**

Sub-address		Register Names		POR Value		Max. Value	
Hex	Dec			Hex	Dec	Hex	Dec
01	01	Contrast (CRT) - Note 2	8-bit DAC	B4	180	FE	254
02	02	Brightness (BRT)	8-bit DAC	B4	180	FF	255
03	03	Drive 1 (DRV) - Note 2	8-bit DAC	B4	180	FE	254
04	04	Drive 2 (DRV) - Note 2	8-bit DAC	B4	180	FE	254
05	05	Drive 3 (DRV) - Note 2	8-bit DAC	B4	180	FE	254
06	06	Output DC Level (DCL) - Note 3	4-bit DAC	09	09	0F	15
07	07	OSD Contrast (OSD)	4-bit DAC	09	09	0F	15
08	08	BPCP & OCL	Refer to the I <sup>2</sup> C table 2	04	04		
09	09	Miscellaneous	Refer to the I <sup>2</sup> C table 3	1C	28		
0A	10	Cut Off Out 1 DC Level (Cut-off) - Note 4	8-bit DAC	B4	180	FF	255
0B	11	Cut Off Out 2 DC Level (Cut-off)- Note 4	8-bit DAC	B4	180	FF	255
0C	12	Cut Off Out 3 DC Level (Cut-off)- Note 4	8-bit DAC	B4	180	FF	255
0D	13	Bandwidth Adjustment (BW)- Note 5	4-bit DAC	07	07	0F	15

**Note 2:** For Contrast & Drive adjustment, code 00 (dec) and 255 (dec) are not allowed.

**Note 3:** For Output DC Level, code 00(dec), 01(dec), 02(dec) are not allowed.

**Note 4:** For Cut Off Output DC Level, codes below 40 (dec) are not allowed.

**Note 5:** To be set to 0 (dec) for applications with  $t_R/t_F > 5.5ns$ .

**Table 2. BPCP & OCL Register (R8) - I<sup>2</sup>C Table (see also Figure 11)**

b7	b6	b5	b4	b3	b2	b1	b0	Function	POR Value
			0				0	Internal BPCP triggered by HSYNC	x
			0				1	Internal BPCP triggered by BLK	
			0			0		Internal BPCP synchronized by the trailing edge	x
			0			1		Internal BPCP synchronized by the leading edge	
			0	0	0			Internal BPCP Width = 0.33 $\mu s$	
			0	0	1			Internal BPCP Width = 0.66 $\mu s$	x
			0	1	0			Internal BPCP Width = 1 $\mu s$	
			0	1	1			Internal BPCP Width = 1.33 $\mu s$	
			1					Internal BPCP = BPCP input (Pin 23)	
		0						Normal Operation	x
		1						Reserved (Force BPCP to 1 in test)	
	0							Normal Operation	x
	1							Reserved (Force OCL to 1 in test)	
0								Internal OCL pulse triggered by BLK (pin 24)	x
1								Internal OCL pulse = Internal BPCP	

**Table 3. Miscellaneous Register (R9) - I<sup>2</sup>C Table 3**

b7	b6	b5	b4	b3	b2	b1	b0	Function	POR Value
							0	Positive Blanking Polarity	x
							1	Negative Blanking Polarity	
						0		Soft Blanking = OFF	x
						1		Soft Blanking = ON	
			1	1	1			AC Coupling Mode or DC with Cut-off control	x
			x	0	1			DC Coupling Mode (Note 6)	
			0	x	0			DC Coupling with Feedback Mode	
	0	0						Light Grey on OSD Outputs = OFF	x
	0	1						Light Grey on OSD Outputs = ON	
	0	0						Dark Grey on OSD Outputs = OFF	x
	1	0						Dark Grey on OSD Outputs = ON	
-								Reserved (SOG = OFF)	x
-								Reserved (SOG = ON)	

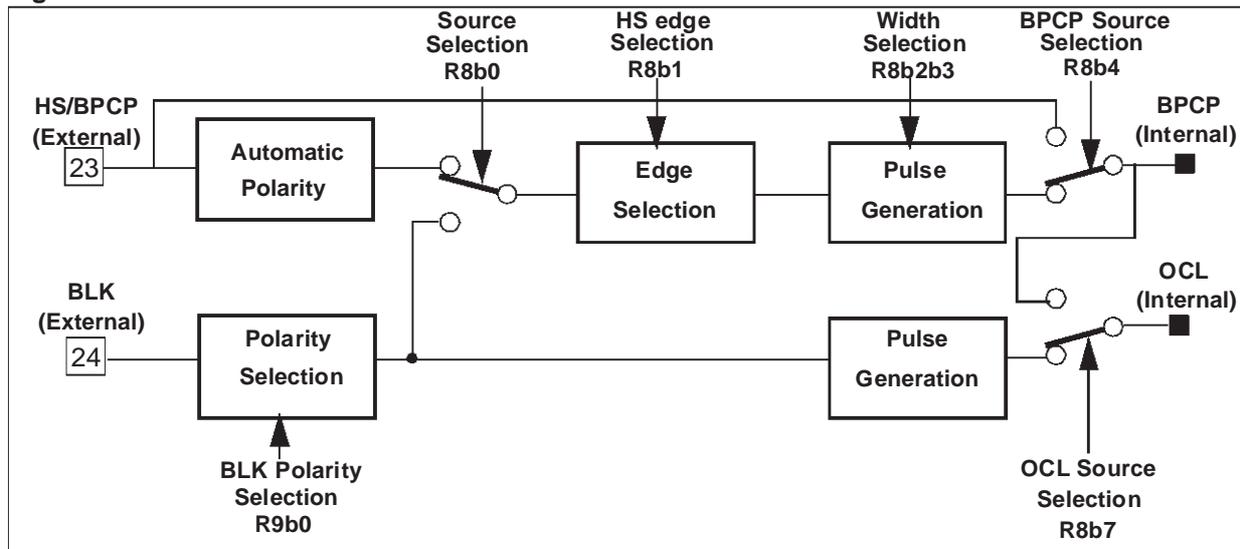
**Note 6:** After Power on, the DC coupling mode must be programmed in register 9 by setting bit 2 =1 and bit3 = 0

**Table 4. Bandwidth Adjustment (R13) - I<sup>2</sup>C Table 4**

b7	b6	b5	b4	b3	b2	b1	b0	Function	POR Value
				1	1	1	1	130 MHz	
				0	1	1	1	100 MHz	x
				0	0	0	0	80 MHz (Note 7)	
		0	0					Normal Operation	x
		0	1					BW DAC output connected to BLK input (for test)	
		1	0					BW DAC complementary output connected to BLK input (for test)	
0	0							Active Video Output Inhibited	x
1	0							Active Video Output Validated	

**Note 7:** For applications with  $t_R/t_F > 5.5ns$ , this register has to be set to 0 (dec).

**Figure 11. BPCP and OCL Generation**



12 INTERNAL SCHEMATICS

Figure 12.

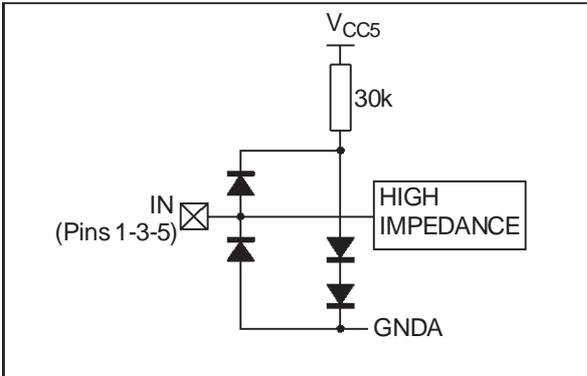


Figure 15.

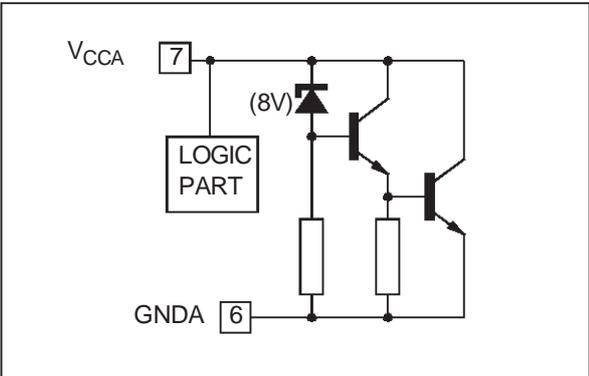


Figure 13.

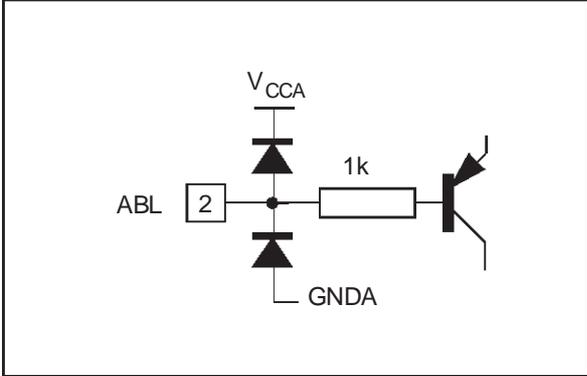


Figure 16.

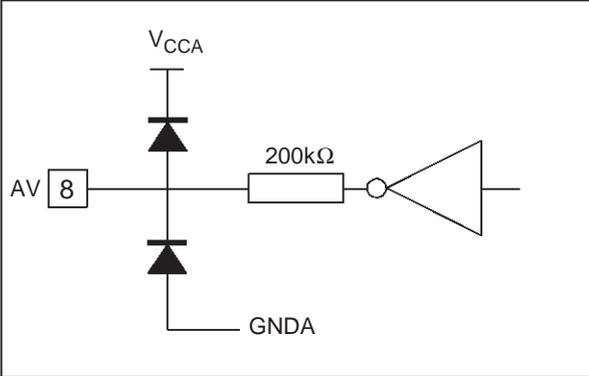


Figure 14.

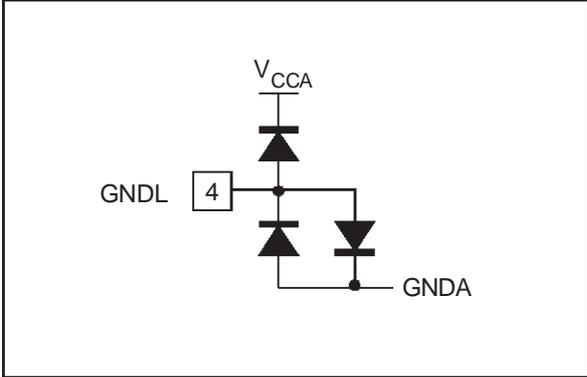


Figure 17.

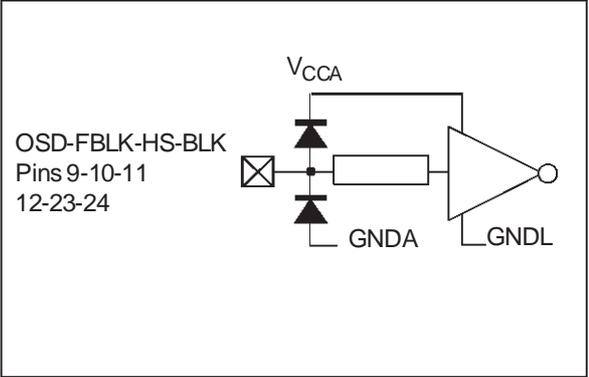


Figure 18.

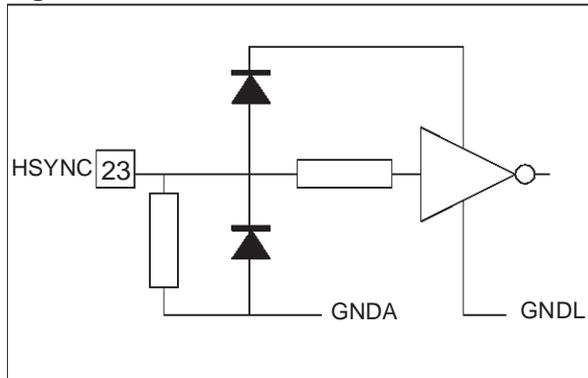


Figure 21.

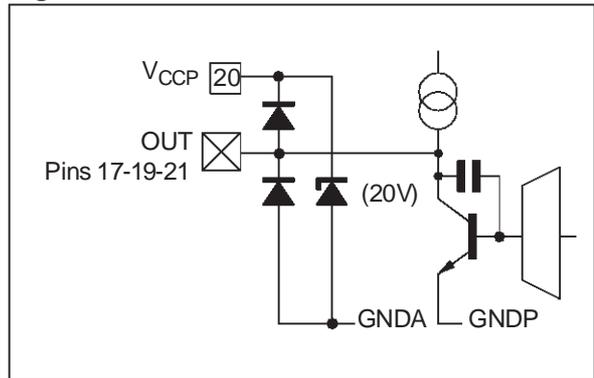


Figure 19.

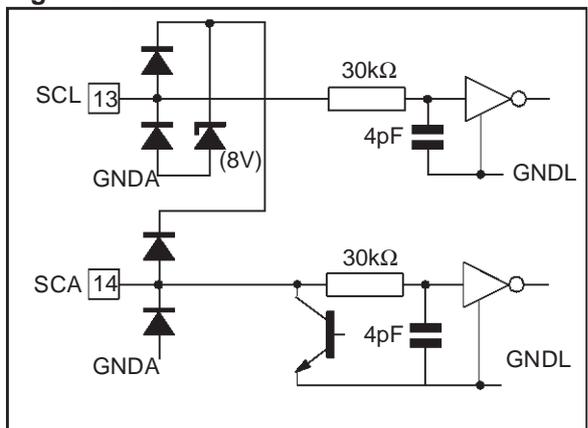


Figure 22.

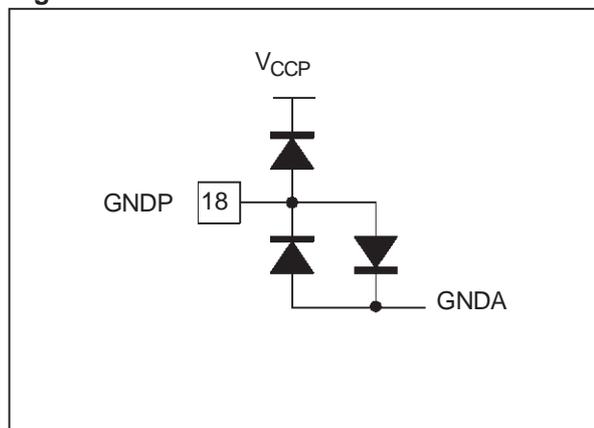


Figure 20.

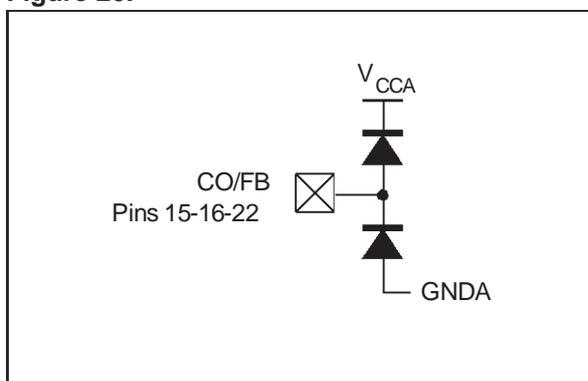


Figure 23. TDA9209/9207 - TDA9533/9530 Demonstration Board: Silk Screen and Trace (scale 1:1)

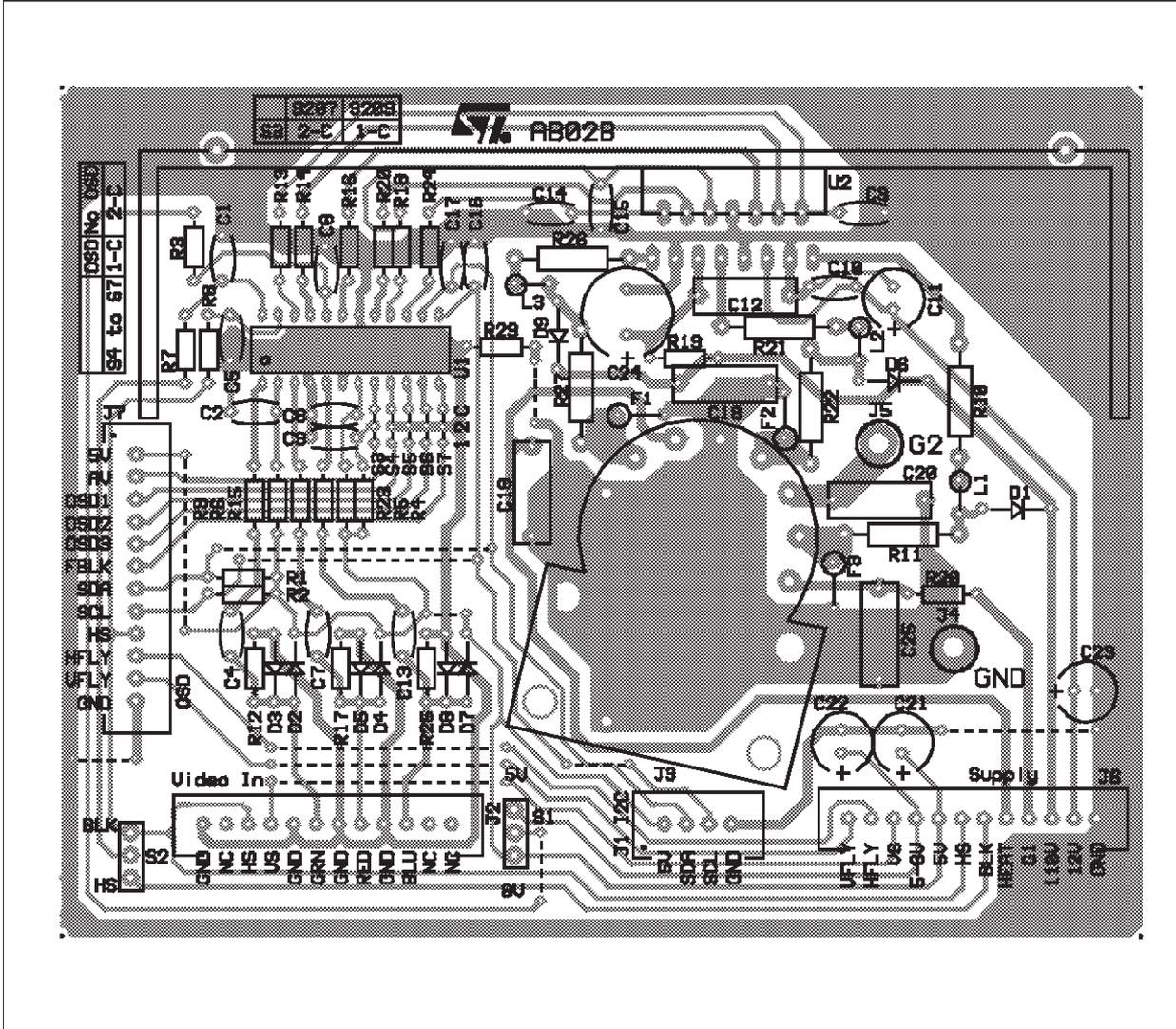
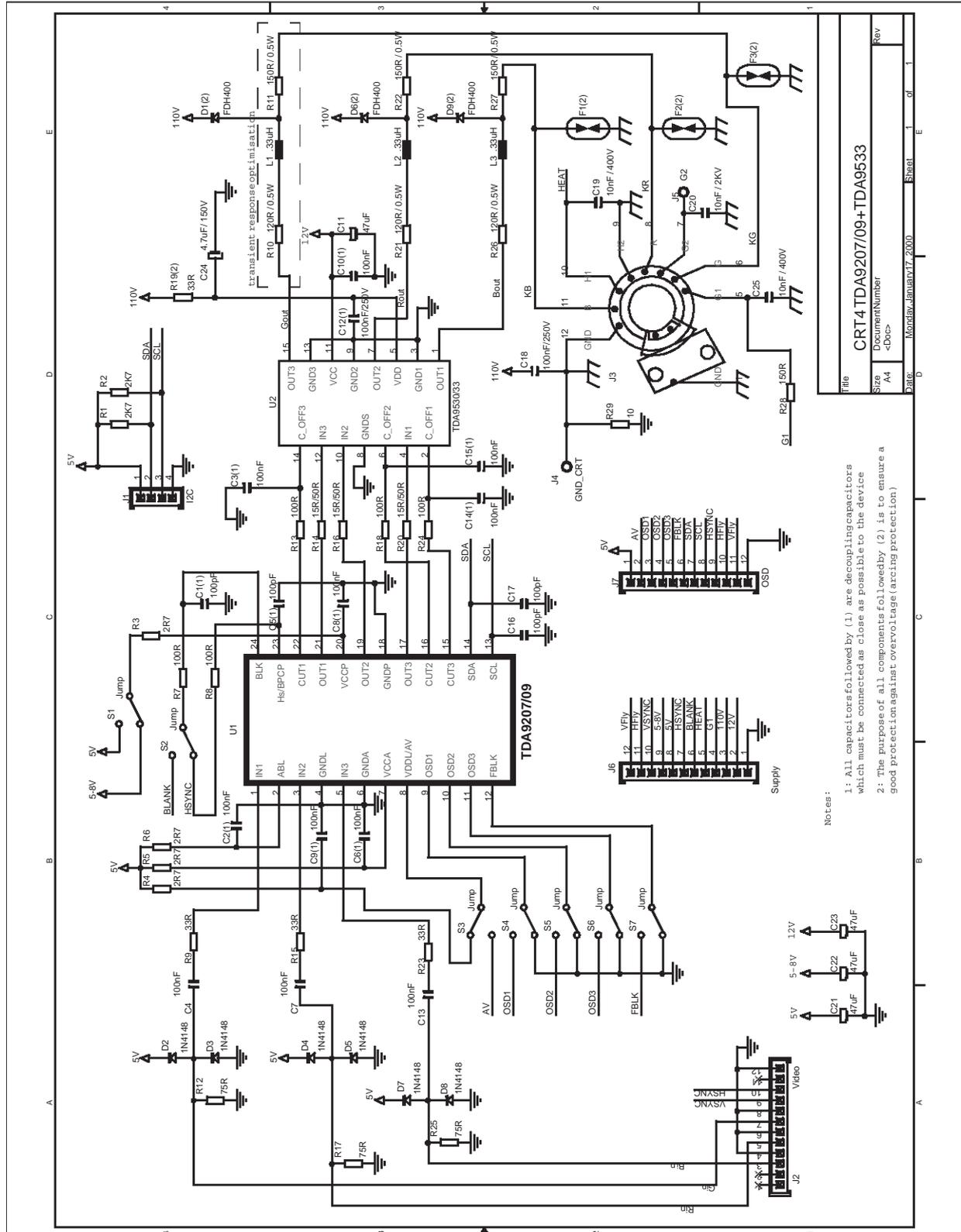


Figure 24. TDA9209/9207 - TDA9533/9530 Demonstration Board Schematic



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Document Number	<Doc>
Rev	
Date	Monday, January 17, 2000
Sheet	1 of 1

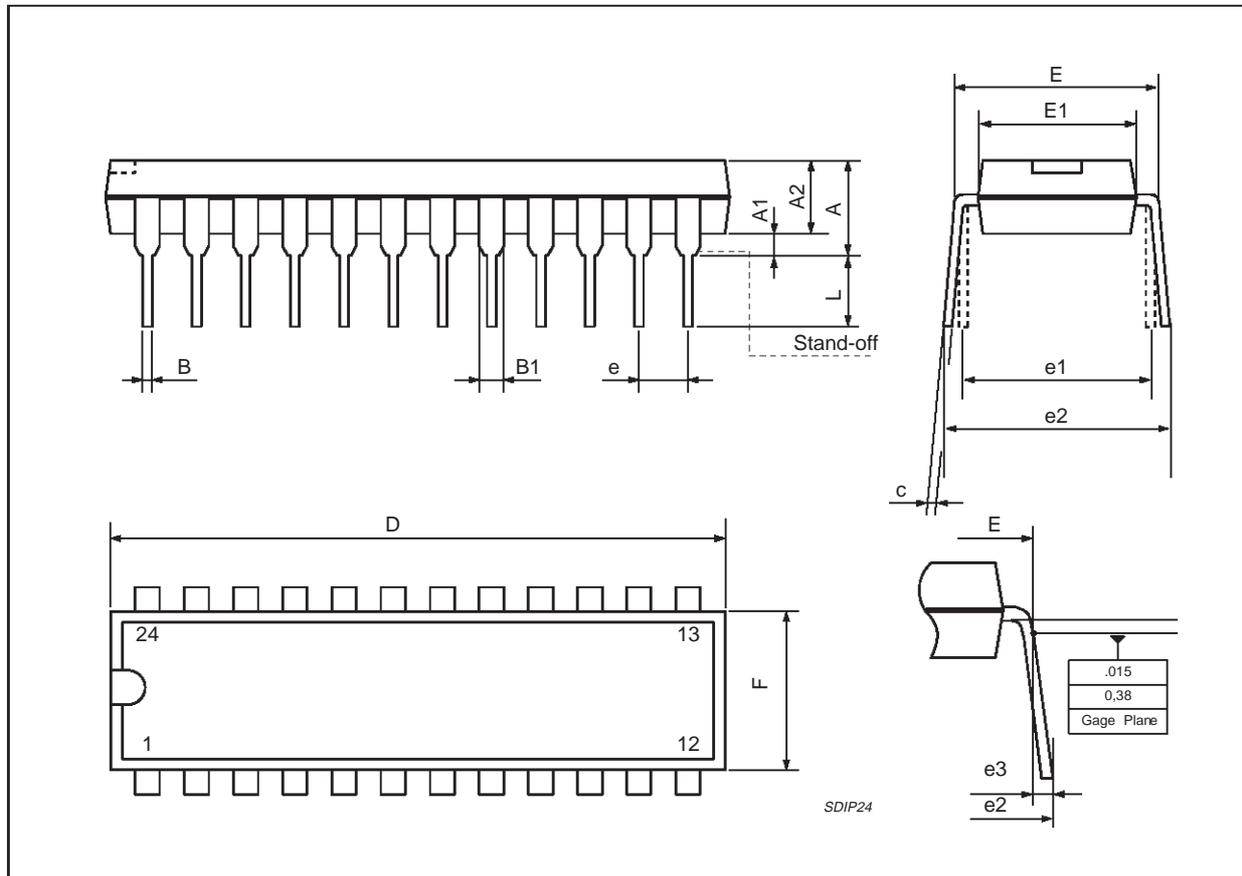
Notes:

- 1: All capacitors followed by (1) are decoupling capacitors which must be connected as close as possible to the device
- 2: The purpose of all components followed by (2) is to ensure a good protection against overvoltage (arcing protection)



## 13 PACKAGE MECHANICAL DATA

### 24 Pins — Plastic Dip (Shrink))



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.08			0.20
A1	0.51			0.020		
A2	3.05	3.30	4.57	0.120	0.130	0.180
B	0.36	0.46	0.56	0.0142	0.0181	0.0220
B1	0.76	1.02	1.14	0.030	0.040	0.045
C	0.23	0.25	0.38	0.0090	0.0098	0.0150
D	22.61	22.86	23.11	0.890	0.90	0.910
E	7.62		8.64	0.30		0.340
E1	6.10	6.40	6.86	0.240	0.252	0.270
e		1.778			0.070	
e1		7.62			0.30	
e2			10.92			0.430
e3			1.52			0.060

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