AN1153
APPLICATION NOTE

M88x3Fxx Programmable Peripheral JTAG Information

The M88x3Fxx complies with the basic IEEE 1149.1 JTAG specification, but does not support boundary scan functions. Instead, the M88x3Fxx supports the In-System-Configuration (ISC) specification of the JTAG interface. The M88x3Fxx can coexist in a JTAG chain with other devices that operate in the boundary scan mode, though, through the use of the BYPASS command.

The M88x3Fxx implements a “pseudo” boundary scan function in that it allows the manipulation of its I/O port pins through special JTAG-ISC commands. This means that the pins on PSD ports A, B, C, and D may be set to high, low, or high-impedance using these JTAG-ISC commands. This is a key feature when other components on the circuit board need to be in a certain state during an ISC session. For example, it may be required to force certain chip select signals for other devices on the board to their inactive state while the M88x3Fxx is being programmed with the JTAG channel.

The IEEE JTAG-ISC specification is still maturing. In spite of this, many systems are in use, by manufacturers today, by means of commonly accepted data file formats that reflect the intent of the ISP specification in its latest form.

There are two files that define ISC functions in a PSD programming environment. One is the Boundary Scan Definition Language (BSDL) file and the other is the Serial Vector Format (SVF) file. The BSDL defines the pins and internal registers of a particular device to be programmed (the JTAG programming model) and the SVF file defines the actions to be taken. These files are interpreted by a device tester or programmer when carrying out the actions specified in the SVF file. (Please see the Texas Instruments web site for general information on JTAG and file formats - *www.ti.com*, performing a search for “JTAG” and “PRIMER”).

PSDSOFT

PSDsoft is a utility that creates SVF files based on the user’s choice of device (within the M88x3Fxx family) and function (program, erase, verify, etc.). ST makes a BSDL file available for each M88x3Fxx device. BSDL files are static by nature. Third-party tester/programmer facilities can blend ST files with BSDL and SVF files from other device manufacturers to create a total chain for the final product.

PROGRAMMING SUPPORT

In addition to providing BSDL and SVF formats to major tester/programmer manufacturers, ST sells a JTAG programmer of its own. FlashLINK is a low cost cable that plugs into a PC/laptop parallel port to support JTAG programming. The target system may operate at 2.7 to 5.5 V_{DC}, the FlashLINK cable “adapts” automatically with no user configuration needed. FlashLINK is controlled by PSDsoft and supports device chaining of multiple FLASH+PSD devices and devices from other manufacturers. The JTAG BYPASS mode is supported to facilitate chaining devices from other manufacturers.

ENHANCED ISP FUNCTION

ST has developed a scheme to speed the ISP function. The scheme employs the optional use of two additional pins beside the four standard JTAG pins.

Standard JTAG pins: TCK, TMS, TDI, TDO

ST enhanced JTAG pins: $\overline{\text{TSTAT}}$, $\overline{\text{TERR}}$

These two optional JTAG pins facilitate hardware flow control for rapid exchange of data. In addition, the M88x3Fxx internally incorporates a JTAG "burst" mode that increments the address pointer automatically between data accesses. Combining these elements allows a complete erase and program cycle of a M88x3Fxx in 11 seconds. This can be achieved with a TCK frequency of 1 MHz. ST's FlashLINK cable assembly will erase and program a M88x3Fxx in approximately 30 seconds (with the FlashLINK TCK at about 200 kHz).

The $\overline{\text{TSTAT}}$ signal indicates the immediate status of the current action in progress. For example, $\overline{\text{TSTAT}}$=0 means the current programming/erasing of a particular byte or sector is not complete, $\overline{\text{TSTAT}}$=1 means the action is finished.

The $\overline{\text{TERR}}$ signal indicates one of two error conditions. Either a time-out of an attempt to program/erase a byte or sector has occurred, or an attempt was made to program a "1" to a Flash memory bit that was already a "0" (Flash memory erases to a "1" and is programmed to a "0"). This signal relieves the device programmer of the task of waiting on a worst-case maximum time-out. As soon as the device programmer sees $\overline{\text{TERR}}$ go active, it stops and handles the error. It is recommended the $\overline{\text{TSTAT}}$ and $\overline{\text{TERR}}$ be used together, not individually.

PROGRAM/ERASE FLOW CONTROL

There are three ways to manage the control of data flowing between a JTAG device programmer and a PSD. PSDsoft allows a choice of these methods and tailors the SVF file to implement the chosen method. These Program/Erase flow control methods are shown below. Option 2 and Option 3 are made possible through ST's enhanced ISP feature.

Option 1: No Flow Control Signals (4 JTAG pins)

This method is the slowest, and is generally not recommended. It involves the device programmer being in an "IDLE" state for a given amount of time for each program or erase action. This idle time must reflect the worst case maximum time for all program/erase actions, since no signal handshaking takes place ($\overline{\text{TSTAT}}$ or $\overline{\text{TERR}}$ is not used).

Option 2: Software Flow Control (4 JTAG pins)

This method involves scanning out the same information that hardware signals $\overline{\text{TSTAT}}$ and $\overline{\text{TERR}}$ provide but in a slower, serial fashion. This method gives a great improvement over Option 1 because the worst-case program/erase time does not have to be assumed.

Option 3: Hardware Flow Control (6 JTAG pins)

The device programmer accesses the $\overline{\text{TSTAT}}$ and $\overline{\text{TERR}}$ handshake signals directly at the PSD pins for each program/erase action. This gives an appreciable improvement over Option 2 because the information at the $\overline{\text{TSTAT}}$ and $\overline{\text{TERR}}$ pins does not have to be scanned out serially. The device programmer may use $\overline{\text{TSTAT}}$ and $\overline{\text{TERR}}$ as edge-level interrupts, or may poll them. A complete M88x3F1x erase and program cycle of 11 seconds is possible using Option 3, with TCK operating at 1 MHz.

The $\overline{\text{TSTAT}}$ and $\overline{\text{TERR}}$ signals may be configured to operate in an open-drain mode, to facilitate connection of several M88x3Fxx devices together on the same circuit board. Please see the section on JTAG Chaining, towards the end of this document, for further details.

The difference between Option 2 and Option 3 becomes very important when long JTAG chains are encountered and programming time is critical. For Option 2, the user has to scan the entire chain to test the $\overline{\text{TSTAT}}$ and $\overline{\text{TERR}}$ bits. Option 3 allows a fast check to be made of the status, independent of the chain length.

MULTIPLEXED JTAG PIN FUNCTIONS

The JTAG pins on Port C of the M88x3Fxx can be multiplexed with other I/O functions when the JTAG functions are not needed. Alternately, the pins may be configured to be dedicated to JTAG at all times. On a blank M88x3Fxx device, the four standard JTAG pins (TCK, TMS, TDI, TDO) are active and ready for JTAG functions.

However, it should be noted that the multiplexing of the JTAG pins with other functions is not supported by the IEEE 1149.1 specification. The multiplexing option is given to the user to maximize the I/O pin count. Multiplexing functions will not pose a problem for users who program their M88x3Fxx devices with FlashLINK.

To be fully compliant with IEEE 1149.1, the user must configure, in PSDsoft, the four standard JTAG pins so that they are dedicated to JTAG functions at all times.

If multiplexing is required, then an additional signal is needed to ensure that the user-specific I/O signals on the circuit assembly do not contend with the JTAG signals during programming. It is recommended that an external signal be used to control the multiplexing. For example, consider a product that uses a programmed M88x3Fxx, and that needs a field update, but that the Port C pins have been put in the I/O mode, and are no longer supporting JTAG. There needs to be a way to reclaim the pins on Port C to support JTAG once again. To solve this problem, one can design the PSD, in PSDsoft, to sense when a JTAG programmer cable is connected to the product, and to force the multiplexed pins to serve JTAG functions.

Instead of using an external signal, it is possible to reclaim the pins for JTAG by other means: an on-board signal generated within the product, for example; or by the microcontroller writing to a PSD control register to enable the JTAG pins.

As an example of multiplexing JTAG signals using FlashLINK, consider Figure 1, which shows the use of an external signal as an input to the M88x3Fxx PLD to enable the JTAG pins. This external signal, called JTAG Enable ($\overline{\text{JEN}}$), can enter the PSD on any valid input pin that is routed to the PLD. $\overline{\text{JEN}}$ must be defined in PSDsoft, and used in an equation that enables four pins on Port C to act as JTAG signals (TCK, TMS, TDI, TDO) when $\overline{\text{JEN}}$ is active. The statements in the PSDabel design file could be as follows:

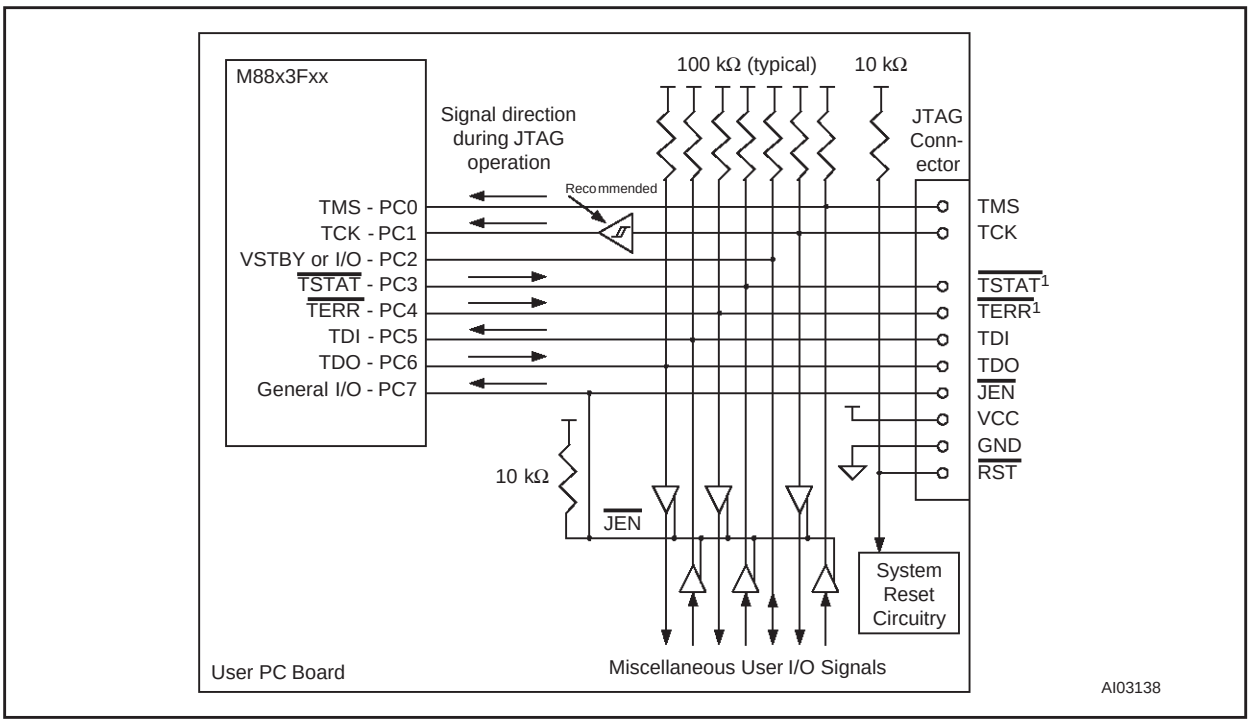
```
JEN pin <optional pin number>;
JTAGSEL = !JEN;
```

This is all that is needed in the PSDabel file to handle the multiplexing of JTAG signals.

In this example, using FlashLINK, all six JTAG pins are available, and any of the three options (1, 2 or 3 as described earlier) can be used. $\overline{\text{JEN}}$ is driven low (active) by the FlashLINK cable prior to any JTAG communications taking place, and remains low until no more JTAG communications are required. When $\overline{\text{JEN}}$ is high (inactive), the four pins become standard I/O signals again. This allows the FlashLINK cable to remain physically connected to the product during development. The two enhanced JTAG pins, $\overline{\text{TSTAT}}$ and $\overline{\text{TERR}}$ become active via a serial JTAG command from the device programmer to the M88x3Fxx.

It is the user's responsibility to ensure that no user-specific logic is driving the JTAG signals during a JTAG operation, and that no user-specific logic is being driven by JTAG signals in a destructive way.

Figure 1. Multiplexed JTAG Signals



Notes: 1. $\overline{\text{TSTAT}}$ and $\overline{\text{TERR}}$ are not part of the IEEE 1149.1 specification

It is the user's responsibility to put the miscellaneous user I/O signals into their high impedance state, so as not to interfere with the JTAG signals while the JTAG pins are operational.

The signal $\overline{\text{JEN}}$ does not have to enter the PSD on pin PC7. $\overline{\text{JEN}}$ can enter on any I/O pin that feeds the PLD.

The $\overline{\text{RST}}$ signal is optional, generated by the FlashLINK cable assembly. Its use is for convenience. It allows the FlashLINK cable to reset the target system board from within PSDsoft. A reset is mandatory after a JTAG ISP of the FLASH+PSD device. $\overline{\text{RST}}$ is active low, and is an open-collector signal.

The power supply, V_{CC} (between 2.7V and 5.5V, and able to supply 15 mA max at 5.5 V) must be routed to the JTAG connector, so that is can be supplied to the FlashLINK cable assembly.

A 10 kΩ pull-up resistor on $\overline{\text{JEN}}$ is needed to ensure that the miscellaneous user I/O signals are not disabled while the FlashLINK cable is disconnected.

Schmitt-trigger buffering on the TCK input is recommended, to reduce the chance of false TCK transitions from spikes, or ringing related to cabling issues.

100 kΩ pull-up resistors on floating inputs are recommended. In this example, some inputs float when no cable is attached to the JTAG connector.

To program the M88x3Fxx in this example, the following sequence is required:

- The device programmer (FlashLINK) first activates the $\overline{JEN}$ signal by driving it low to enable the JTAG functions on the PSD pins.
- Because $\overline{JEN}$ is also connected to the enable lines on the tri-state buffers, the $\overline{JEN}$ signal disables any user-specific signals that are driving multiplexed JTAG pins.
- The four JTAG signals (TCK,TDI,TDO,TMS) are now active.
- The device programmer sends an initialization command over the JTAG channel to the PSD that activates the $\overline{TSTAT}$ and $\overline{TERR}$ signals. After that, all six JTAG pins are enabled and active. The following is an example of the sequence of ST JTAG-ISC commands that are generated by PSDsoft and the FlashLINK cable, transparent to the user, once the user has set up the sequence in the GUI of PSDsoft:

```
ISC-VM-ENABLE  ; enables JTAG interface to write to
               ; registers inside the PSD
ISC-SET-IO     ; sets PSD ports A,B,C,D to desired state
ISC-ENABLE     ; enables more JTAG features including
               ; the TSTAT\ and TERR\ pins
ISC-ERASE      ; erase specified blocks
ISC-PROGRAM    ; program specified blocks
ISC-DISABLE    ; disables JTAG control logic, at this point TSTAT\ and TERR\
               ; pins are disabled but TCK, TMS, TDO, TDI are still active.
```

The pins TCK, TMS, TDO, TDI pins go back to non-JTAG functions as soon as the external $\overline{JEN}$ signal is taken high (inactive).

On a blank M88x3Fxx device, the JTAG pins are enabled, and active, immediately from power-on. However, $\overline{JEN}$ would still be needed to put the miscellaneous user I/O signals in their high impedance state.

Dedicated JTAG pin functions (basic four signals only)

If compliance with IEEE 1149.1, and the multiplexing of the JTAG pins, is not required, the hardware connection, shown in Figure 2, would be appropriate.

The $\overline{RST}$ signal is optional, generated by the FlashLINK cable assembly. Its use is for convenience. It allows the FlashLINK cable to reset the target system board from within PSDsoft. A reset is mandatory after a JTAG ISP of the FLASH+PSD device. $\overline{RST}$ is active low, and is an open-collector signal.

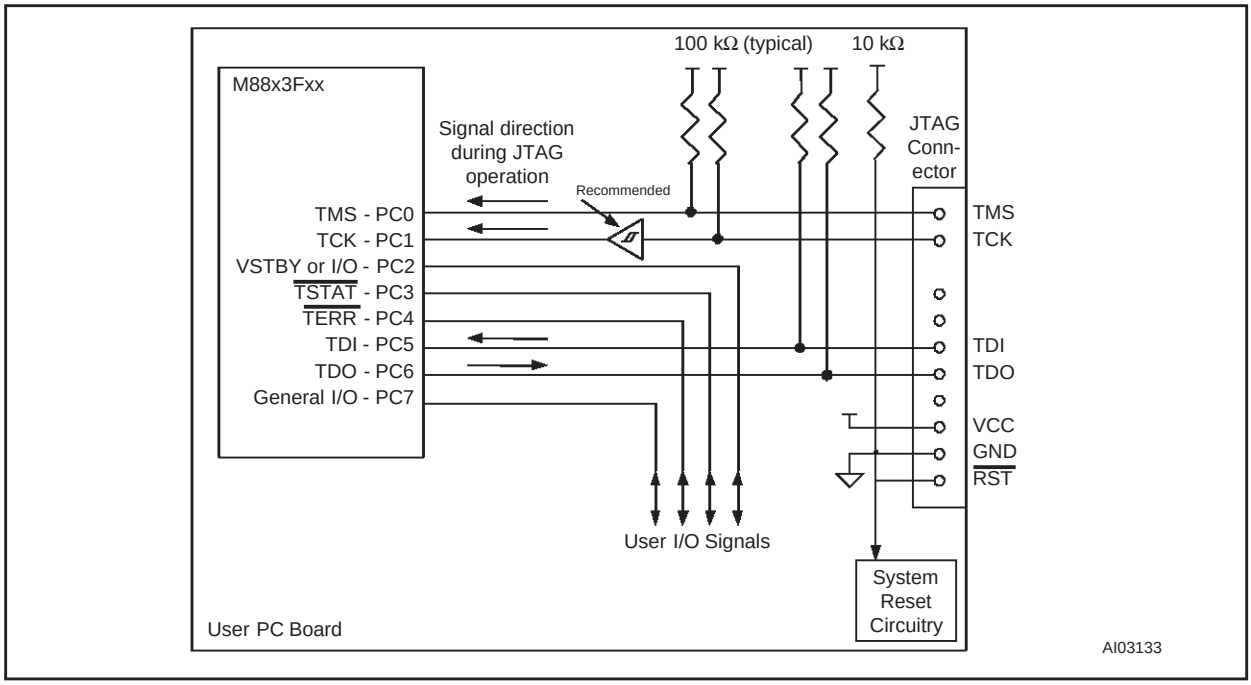
The power supply, V_{CC} (between 2.7 V and 5.5 V, and able to supply 15 mA max at 5.5 V) must be routed to the JTAG connector, so that is can be supplied to the FlashLINK cable assembly.

Schmitt-trigger buffering on the TCK input is recommended, to reduce the chance of false TCK transitions from spikes, or ringing related to cabling issues.

100 kΩ pull-up resistors on floating inputs are recommended. In this example, some inputs float when no cable is attached to the JTAG connector.

In this example, a device programmer has full access to the basic four JTAG pins at all times.

Figure 2. Non-Multiplexed JTAG Signals (basic four signals only)



DEDICATED JTAG PIN FUNCTIONS (ALL SIX SIGNALS)

If the multiplexing of the JTAG pins is to be avoided, and the use of the additional JTAG signals ($\overline{TSTAT}$ and $\overline{TERR}$) is required, the hardware connection, shown in Figure 3, would be appropriate, and any of the three options (1, 2 or 3 as described earlier) can be used.

The $\overline{RST}$ signal is optional, generated by the FlashLINK cable assembly. Its use is for convenience. It allows the FlashLINK cable to reset the target system board from within PSDsoft. A reset is mandatory after a JTAG ISP of the FLASH+PSD device. $\overline{RST}$ is active low, and is an open-collector signal.

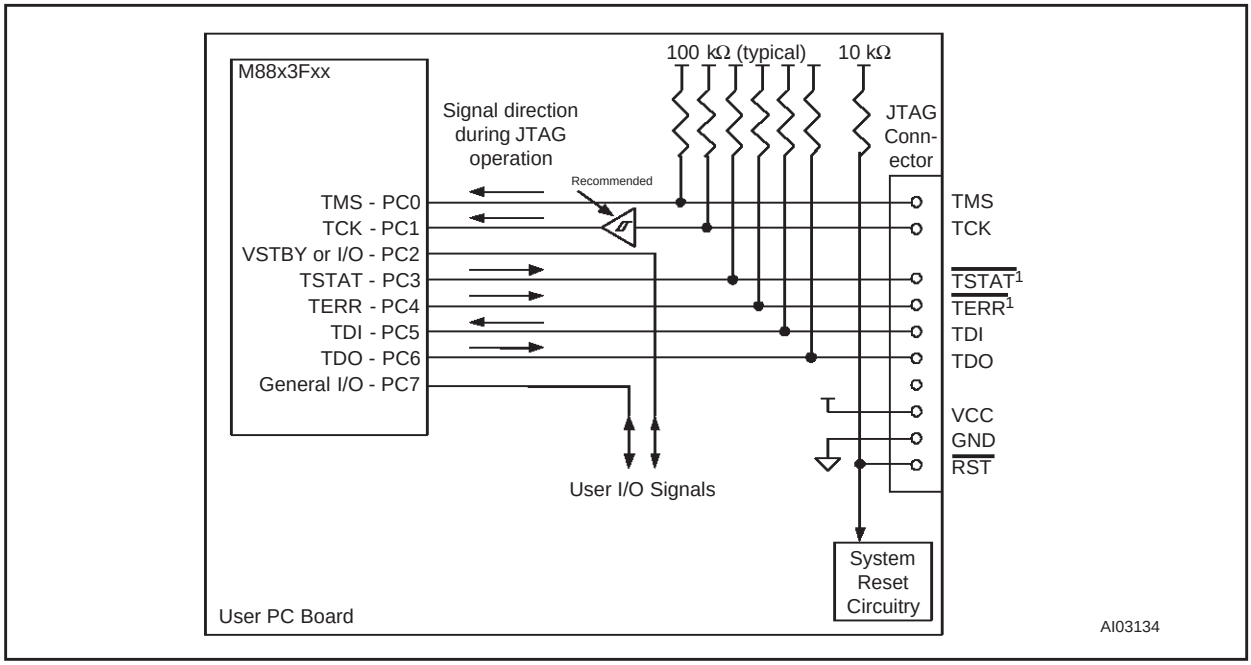
The power supply, V_{CC} (between 2.7V and 5.5V, and able to supply 15 mA max at 5.5 V) must be routed to the JTAG connector, so that is can be supplied to the FlashLINK cable assembly.

Schmitt-trigger buffering on the TCK input is recommended, to reduce the chance of false TCK transitions from spikes, or ringing related to cabling issues.

100 kΩ pull-up resistors on floating inputs are recommended. In this example, some inputs float when no cable is attached to the JTAG connector.

In this example, the device programmer sends an initialization command over the JTAG channel to the PSD to activate the additional $\overline{TSTAT}$ and $\overline{TERR}$ signals. After that, all six JTAG pins are enabled and active.

Figure 3. Non-Multiplexed JTAG Signals (all six signals)



Notes: 1. $\overline{TSTAT}$ and $\overline{TERR}$ are not part of the IEEE 1149.1 specification

ST ENHANCED JTAG ISP CONNECTOR DEFINITION

There is no “standard” JTAG connector with a different pin-out offered by each manufacturer. ST has a specific connector and pin-out for the FlashLINK programmer adapter. The connector scheme on the FlashLINK adapter can accept a standard 14-pin ribbon connector (2 rows of 7 pins on 0.1-inch centers, with standard keying) or any other user-specific connector that can slide on to 0.025-inch square posts. The pin-out for the FlashLINK adapter connector is shown in Figure 4.

A standard ribbon cable is a convenient way to connect to the target circuit board. If a ribbon cable is used, then the receiving connector on the target system should be the same connector type, with the same pin-out as the FlashLINK adapter shown in Figure 4. The JTAG TDI signal comes from the FlashLINK adapter, and should be routed on the target circuit card so that it connects to the TDI input pin of the PSD device. Although the name “TDI” infers “Data In” by convention, it is an output from FlashLINK and an input to the PSD device. Similarly, the JTAG TDO signal is an input, received by the FlashLINK adapter, and comes from the PSD device on the TDO output pin. Figure 1, Figure 2, Figure 3, and Figure 7 can be used as guides.

In Figure 4, it can be noted that the core JTAG signals have been placed on the odd numbered pins (in the right hand column), and that the optional features have been placed on the even numbered pins (in the left hand column).

Figure 4. JTAG Connector Recommended Adapter Pin-out (source)

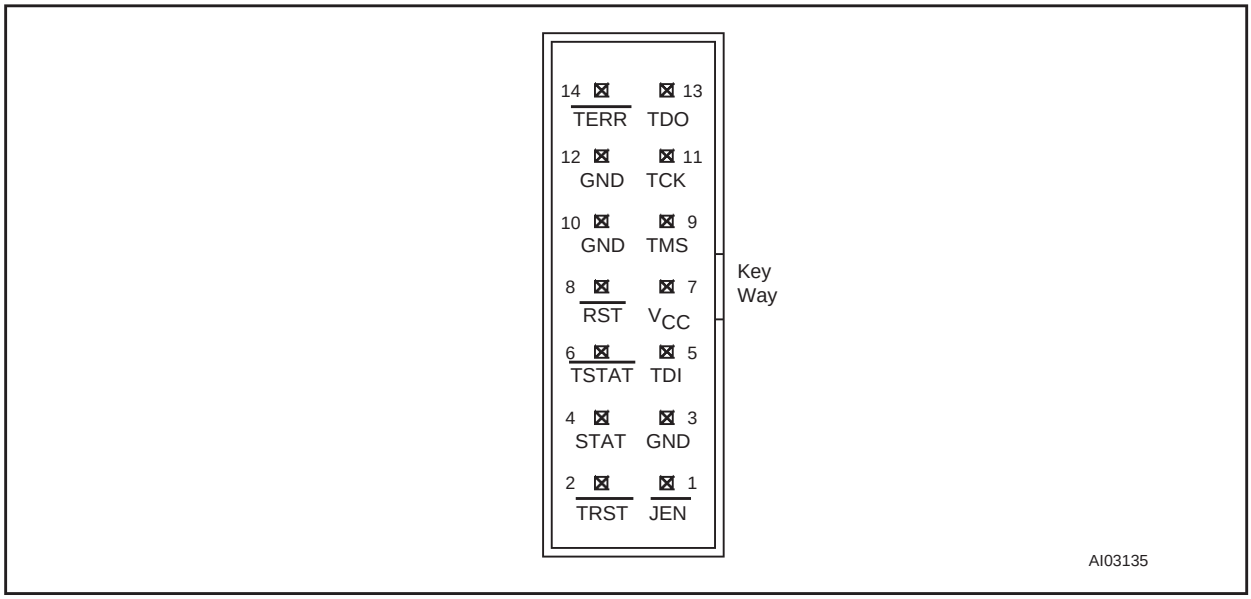
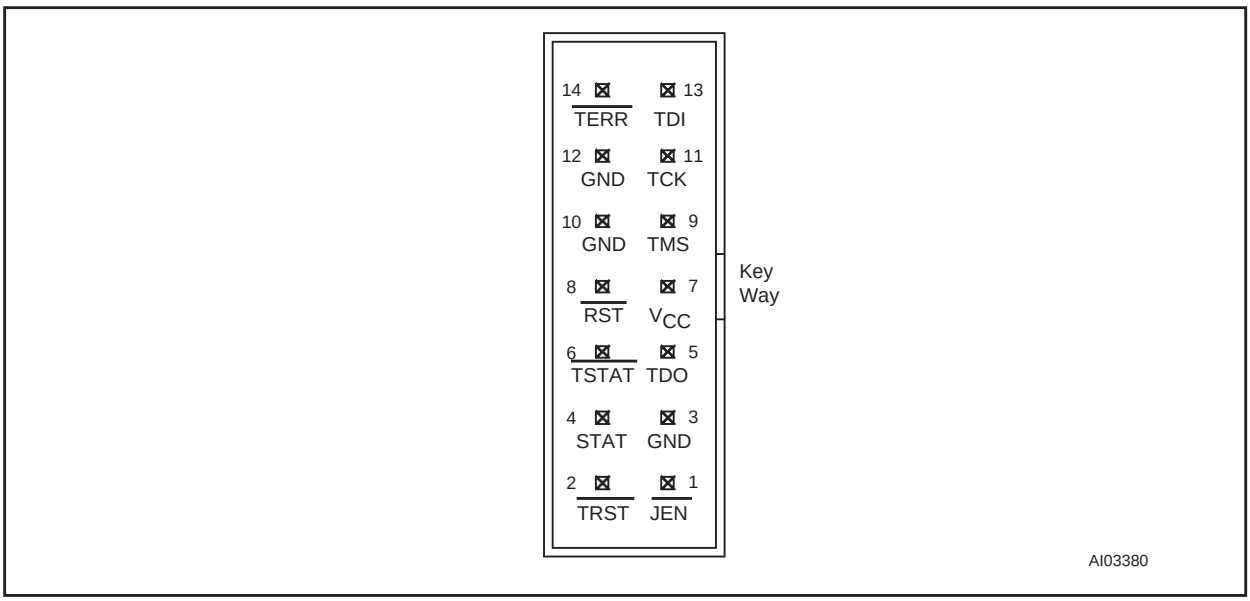


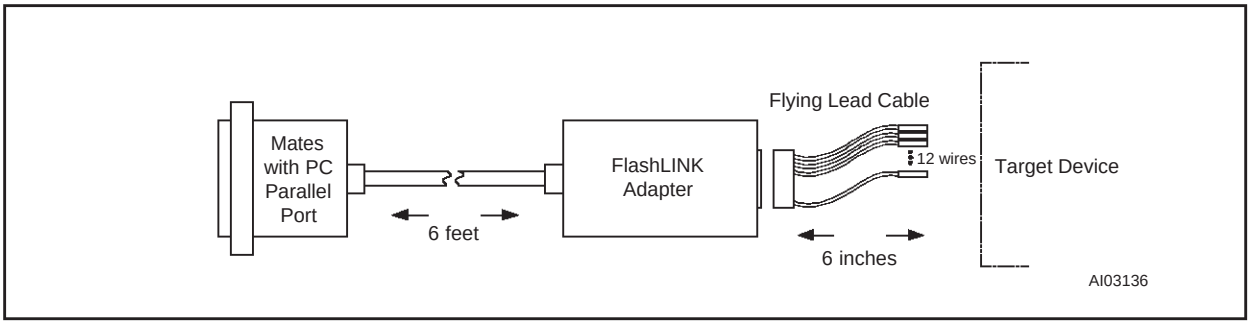
Figure 4 shows the view looking into the face of the shrouded male connectors (which are 0.025-inch posts on 0.1-inch centers). The connector reference is: Molex 70247-1401. The recommended ribbon cables for quick connection of the FlashLINK adapter to the end product are: Samtec HCSD-07-D-06.00-01-S-N and Digikey M3CCK-14065-ND. The user should ensure that the target pin-out, on the end product, is as shown in Figure 5.

Figure 5. JTAG Connector Recommended Target Pin-out (receiver)



Each FlashLINK is sold with a six-inch “flying lead” cable, for maximum flexibility (as opposed to a ribbon cable, which would have assumed the use of a specific connector for the target assembly). This flying lead cable, shown in Figure 6, connects to the FlashLINK adapter at one end, and has loose sockets at the other end (to slide on to 0.025-inch square posts on the target assembly).

Figure 6. FlashLINK Cable Assembly as Sold



The signals are as defined in Table 1.

Table 1. Pin descriptions for FlashLINK adapter assembly

Pin Number	Signal Name	Description JTAG = IEEE 1149.1 EJTAG = ST ENHANCED JTAG	Type	At the FlashLINK
1	$\overline{JEN}$	Enables JTAG pins on FLASH+PSD (optional)	Open Collector	Source
2	$\overline{TRST}$ [3]	JTAG reset on target (optional per 1149.1)	Open Collector	Source
3	GND [1,2]	Signal ground		
4	STAT [3]	Generic signal, user defined		Destination
5	TDI [1]	JTAG serial data input		Destination
6	$\overline{TSTAT}$	EJTAG programming status		Destination
7	V_{CC} [1]	V_{DC} Source from target [4]		
8	$\overline{RST}$	Target system reset (optional)	Open Collector	Source
9	TMS [1]	JTAG mode select		Source
10	GND [2]	Signal ground		
11	TCK [1]	JTAG clock		Source
12	GND [2]	Signal ground		
13	TDO [1]	JTAG serial data output		Source
14	$\overline{TERR}$	EJTAG programming error		Destination

Notes: 1. These signals are required connections, the others are optional.
2. All signal grounds are connected inside the FlashLINK adapter
3. Not initially supported by PSDsoft.
4. The target device must supply V_{CC} to the FlashLINK Adapter (2.7 to 5.5 V_{DC}, 15 mA (max.) at 5.5V).

Not all of the 14 signals are necessarily needed for any given application. They are as follows:

- There are six core signals that must be connected: **TDI, TDO, TMS, TCK, V_{CC}, GND**
- Two signals are optional, for enhanced ISP (as in the Option 3 flow control): **$\overline{TSTAT}$, $\overline{TERR}$**
- One signal is optional, to control multiplexing of the JTAG signals: **$\overline{JEN}$**
- One signal is optional, to allow FlashLINK to reset target system after ISP: **$\overline{RST}$**
- One signal is optional, under IEEE-1149.1, for JTAG chain reset: **$\overline{TRST}$**
- One signal is optional, for generic control from FlashLINK to target system: **STAT**
- Two additional ground lines help reduce EMI if a ribbon cable is used. These ground lines “sandwich” the TCK signal in the ribbon cable. These lines are not needed for use with the flying lead cable, which is why the flying lead cable only has 12 of 14 wires.

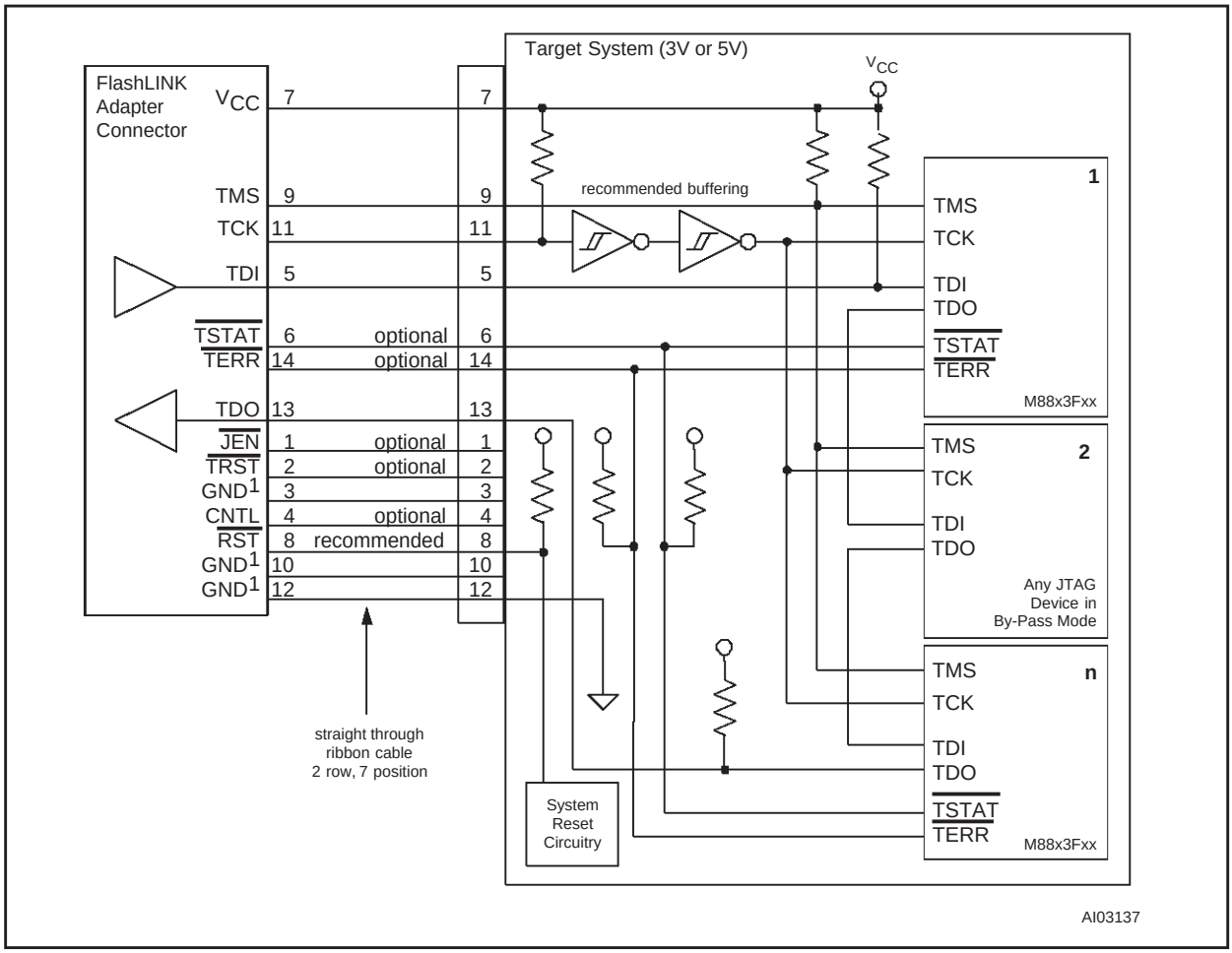
JTAG CHAINING

Multiple FLASH+PSD devices may be placed in a JTAG chain configuration. An example of this configuration is shown in Figure 7, which also shows that FLASH+PSDs can reside in a JTAG chain with non-PSD devices. However, the non-PSD devices cannot be programmed using PSDsoft. These devices are placed by PSDsoft in BYPASS mode while the JTAG operations are occurring on PSD devices.

PSDsoft performs operations on only one FLASH+PSD device at a time. This means that while one FLASH+PSD device is being programmed or erased, the other FLASH+PSDs are in BYPASS mode. Future versions of PSDsoft will support concurrent programming of several PSD devices in the JTAG chain.

As shown in Figure 7, the enhanced JTAG signals $\overline{\text{TSTAT}}$ and $\overline{\text{TERR}}$ are Wire-Ored together (and are configured as open-drain outputs). The FLASH+PSD devices that are in BYPASS mode do not assert $\overline{\text{TSTAT}}$ and $\overline{\text{TERR}}$; only the FLASH+PSD that is performing JTAG operations asserts these signals.

Figure 7. JTAG Chaining Example (with M88x3Fxx and other JTAG-compatible devices)



Notes: 1. All ground pins are connected together inside the FlashLINK assembly

Finally, it should be noted that all sections of the M88x3Fxx are programmable via the JTAG interface, except the 64 byte “OTP row” of EEPROM in the M88x3F1x.

For current information on FLASH+PSD products, please consult our pages on the world wide web:
www.st.com/flashpsd

If you have any questions or suggestions concerning the matters raised in this document, please send them to the following electronic mail addresses:

apps.flashpsd@st.com (for application support)
ask.memory@st.com (for general enquiries)

Please remember to include your name, company, location, telephone number and fax number.