QRSR9401
QUALIFICATION REPORT

ZEROPOWER and TIMEKEEPER SRAM
Surface Mounted SNAPHAT Package

This document was previously known as *QR103*. Its purpose is to present the summary of the reliability tests performed to qualify the SNAPHAT housing used for ZEROPOWER and TIMEKEEPER devices from STMicroelectronics.

Table 1. Process and Packaging

	Process	Package
ZEROPOWER and TIMEKEEPER devices	SNAPHAT	SOIC with SNAPHAT

ST is dedicated to the philosophy that the quality of a product must be built-in during the design, material procurement, manufacturing and testing phases, and that the reliability must be demonstrated before the product is released to full mass production. The qualification of new products and the certification of new processes is a rigorous task undertaken by Quality and Reliability professionals, to ensure stable products and processes capable of fully meeting customer requirements.

A key step of this activity is the Design Review where we assure that:

– adequate and realistic product specifications have been developed

– design and layout rules, as documented in the Design Rules Manual, have been respected

– critical performance parameters and process variables have been identified

– previously untested design techniques or manufacturing processes are recognized

– manufacturability concerns are identified

– comprehensive and efficient qualification programs are defined.

Product Qualification is made on all new products and new packages. Qualification is also remade on existing products when there are major changes to the design or manufacturing process. The tests performed are tailored to the parameters affected by the major change or the combinations of new die or new package to be evaluated.

The results of the tests for the SNAPHAT housing for ZEROPOWER and TIMEKEEPER devices are listed on the attached pages of this Qualification Report.

Director of Memory Products Group
Quality Control & Reliability

Attilio PANCHIERI

QUALIFICATION OVERVIEW

The qualification plan included stressing the SNAPHAT housing and SOIC package separately as well as assembled in module form. This allowed evaluation of all possible failure modes. The test vehicle chosen was the M48T08. Each component has different reliability and manufacturing concerns that were addressed in qualification. These are summarized in Table 2.

Table 2. Reliability Concerns – Failure versus Stress Matrix

Component	Potential Failure Mechanism	Stress Used to Verify Reliability
SOIC Package	"Popcorn" failures	Resistance to Surface Mount
	Bonding failures	Temperature Cycling: –40°C to 125°C
	Moisture-induced failures	Autoclave and HAST
	Female pin corrosion	Autoclave and HAST
SNAPHAT Housing	Battery and crystal welds	100°C, 125°C, 140°C Storage, Temperature Cycling, Welding Characterisation, Pull Strengths
	Poor battery lifetime	100°C, 125°C, 140°C Storage, Temperature Cycling
	Male pin plating peeling, cracking	100°C, 125°C, 140°C Storage, Temperature Cycling
Module: SOIC and SNAPHAT	Operational life failures	Accelerated Life at 125°C
	Moisture-induced failures	Temperature and Humidity
	Loss of memory with V_{CC}=0V	85°C Storage, Temperature Cycling, both with patterns
	Male or Female pin corrosion	Temperature and Humidity, Post Stress Visual Inspection

Based on this analysis, the qualification test plan, described in Table 3, Table 4 and Table 5, was used to qualify the ZEROPOWER SNAPHAT package. Specific details of the test methods are given in the section entitled "Device Description" on page 4. Samples for stress were taken from four back-end production lots and were divided equally between the stresses. The results of the stressing are described in the section entitled "Qualification Test Results" on page 7.

Table 3. Qualification Test Plan – Module

Stress	Condition	Duration	Samples
Temperature and Humidity	T_A=85°C, RH=85%, V_{CC}=5.5V	959 hours	70
Temperature Cycling (with Stored Patterns)	–40°C to 125°C	1000 cycles	78
High Temperature Storage (with Stored Patterns)	T_A=85°C	1000 hours	78

Table 4. Qualification Test Plan – SOIC Package

Stress	Condition	Duration	Samples
Operational Life	V_{CC}=7V, T_A=125°C	1000 hours	276
Temperature Cycling	–40°C to 125°C	1000 cycles	102
HAST	T_A=131°C, RH=85%, V_{CC}=5.5V	196 hours	44
Autoclave	T_A=121°C, RH=100%, unbiased	240 hours	45
Resistance to Surface Mounting	See Table 6	215°C IR Reflow after T&H soak	10

Table 5. Qualification Test Plan – SNAPHAT Housing

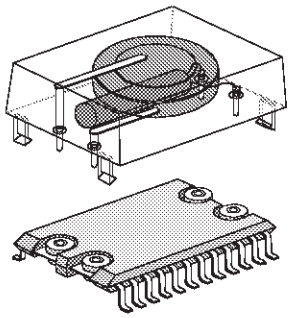
Stress	Condition	Duration	Samples
High Temperature Storage	100°C	OCV – 3.σ < 2.0 V	98
High Temperature Storage	125°C	OCV – 3.σ < 2.0 V	98
High Temperature Storage	140°C	OCV – 3.σ < 2.0 V	98

DEVICE DESCRIPTION

Since their introduction in 1984, by STMicroelectronics, ZEROPOWER self contained battery backed-up static memories, have offered the system designer a non-volatile memory with excellent performance characteristics. Prior to ST's further innovation, though, all battery-based non-volatile SRAMs had been offered in some form of a 600 mil dual-in-line package. The non-volatile technology has not evolved into surface mount configurations for the primary reason that the energy cell cannot survive the ultra high temperatures needed for solder reflow. The new SNAPHAT package from ST overcomes this obstacle and offers the industry's first integrated battery backed SRAM that can be surface mounted. This revolutionary surface mount design combines the company's patented monolithic memory and battery control circuitry with a unique battery housing and small outline package to form a highly compact SMT solution.

The SNAPHAT® package consists of two parts: a standard 330 mil Small Outline Integrated Circuit package (SOIC) and the attachable battery housing, as shown in Figure 1. The SOIC package has two conventional press fitted sockets at both ends. Once the SOIC and other surface mount components are attached to the printed circuit board, the battery housing, with its interconnect pins, mechanically locks to the SOIC package to provide energy backup in the event of system power loss.

Figure 1. SOIC and SNAPHAT Packaging



ST designed the SNAPHAT package with long term reliability in mind. Critical contact points at the socket and battery package pins are gold plated to resist oxidation. Internally, each socket contains six independent contact fingers to form redundant connections between the two components. These sockets were designed to provide high point contact force to scrape away potential contamination from the user's assembly process. Furthermore, the battery package has two flexible snap clips at both ends to secure the housing firmly to the SOIC package.

In addition to the ZEROPOWER® RAM, a TIMEKEEPER® RAM, which incorporates a built-in real time clock, is also offered in the SNAPHAT package. This device includes a crystal in the attachable housing which allows the time-keeping function to continue in the absence of system power. When assembled, the SNAPHAT ZEROPOWER RAM and TIMEKEEPER RAM offer a non-volatile memory and real time clock solution with the smallest footprint and form factor on the market today.

DESCRIPTION OF QUALIFICATION TESTS

The qualification devices for this program were sampled from three separate assembly lots. All samples were processed through the standard production flow including Final Test as described in Table 3, Table 4 and Table 5. These units were subjected to the reliability tests described as follows.

High Temperature Operational Life

High Temperature Operating Life (H.T.O.L) testing was performed to accelerate failure mechanisms which are thermally activated through the application of extreme temperatures and biased operating conditions. H.T.O.L. testing was performed at 125°C and 7.0 volts. The high voltage stress increases electric field strength across the gate and inter-level oxides well beyond the level any device will encounter during application, thereby providing maximum acceleration for potential dielectric breakdown failures. This stress also increases the active currents and power dissipation, thereby increasing the acceleration for electro-migration failures. The devices were exercised by sequentially addressing all cells in the memory array and alternately writing and reading complementing data.

Temperature and Humidity Biased Test

Temperature Humidity Bias (T.H.B.) testing was performed to assess the moisture resistance of plastic encapsulated devices. Failure mechanisms expected are primarily corrosion of the external leads and connections, and the aluminum traces within the integrated circuits. The test samples were stressed at 85°C and 85% RH, and statically biased to achieve minimum power dissipation and junction heating. Input pins were alternately biased to V_{CC} and V_{SS} in order to maximize the number of biased gaps and accelerate electrolytic corrosion of the metallization. This stress was performed for 959 hours. Extreme care was taken to prevent dry-out of the packages during the period when the devices were removed from stress for the electrical readouts by storing them in a 25°C, 85% RH wet-box. The initial and final electrical tests were performed at 70°C; however, all interim tests were performed at 25°C to prevent baking the moisture out of the devices during test.

Temperature Cycling

Temperature cycle testing accelerates the effects of the thermal expansion coefficient mismatch among the different components within any given die and packaging system. This stress was performed in accordance with MIL-STD-883C, Method 1010. Qualification components were stressed from –40°C to 125°C for a minimum of 1000 cycles. Modules were tested with a “final pattern” written into the memory array. As read-points occurred, the memory was read to see if this pattern remained in the memory. Failure to read the proper data is taken as evidence of stress failure.

High Temperature Storage - SNAPHAT

This stress accelerates the evaporation of the liquid electrolyte within the battery, as indicated by the decreasing battery voltage over time. Three temperatures 140°C, 125°C, 100°C are used to determine an acceleration factor for the evaporation. The resultant data is compared to historical values when stressing is completed. The effects of high temperature stressing on the physical joints through aging and expansion of dissimilar materials is also assessed.

High Temperature Storage with Patterns - Module

To determine the module’s ability to retain patterns at high storage temperatures, a test pattern was written into the memory of a completed SNAPHAT module. V_{CC} was then removed and the unbiased units were stored in an oven at 85°C. The first test at each read-point is the verification of this pattern, and a failure is revealed if it is corrupted or missing.

Resistance to Surface Mounting

The effects of surface mounting the SOIC package were determined by using a series of preconditions, stresses, and evaluations. The flow is listed in Table 6. Devices were baked dry, then exposed to 10 cycles of –40°C to 60°C temperature cycle, which stresses the leadframe-to-plastic interface in order later to maximize moisture uptake. The units were then put into an 85°C, 35% relative humidity chamber for 168 hours, which gave the units a moisture content of approximately 1400 ppm by weight. This was immediately followed by exposure to an infrared radiation source, which produced a maximum body temperature of 215°C, as measured with a thermocouple. Post stress testing included 30x external visual inspection for cracks, electrical test for die cracks, and internal cross-sectioning for diepad-to-leadframe cracks.

Table 6. Resistance to Surface Mounting Stress Flow

Stress	Condition	Duration
Storage	T_A=125°C	24 hours
Temperature Cycling	–40°C to 60°C	10 cycles
Moisture Exposure	T_A=85°C, RH=35%	168 hours
Infrared Exposure	215°C (max.)	45 seconds
Visual Inspection	External (for cracks)	—
Electrical Test	Final test	—
Cross Section	Internal (for cracks)	—

QUALIFICATION TEST RESULTS

This section contains the results of the stressing as described in section entitled “Qualification Overview“ on page 2. Four back-end lots were assembled and submitted for reliability testing. The stresses used, along with the results at each read-point, have been compiled in Table 7, Table 8 and Table 9.

Module Stressing Results

Biased Temperature and Humidity stressing produced no failures through 2000 hours of stress. A sample of units were deprocessed at this read-point for evidence of internal metal corrosion and gold contact deterioration including cracking, peeling, and corrosion. No degradation of any kind was detected.

Also on Temperature Cycling and 85°C storage with patterns, no data corruption failures occurred indicating the SNAPHAT housing to SOIC package connections remained intact throughout the stress. Post stress inspection of both the male and female connection pieces after 1000 cycles indicate no corrosion or other physical deformation.

SNAPHAT Housing Stressing Results

The 100°C, 125°C, and 140°C high temperature storage tests have exhibited battery lifetimes comparable to the standard CAPHAT package. Stressing will continue until battery end of life. Brand Permanency, Physical Dimension, and X-ray all indicated good construction and dimensional characteristics.

Table 7. Qualification Test Results – Module

Stress	Condition	Read-point	Samples	Failures
Temperature and Humidity	T_A=85°C, RH=85%, V_{CC}=5.5V	548 hours 959 hours 1500 hours	70 70 70	0 0 0
Temperature Cycling (with Stored Patterns)	–40°C to 125°C	100 cycles 300 cycles 1000 cycles 2000 cycles	77 77 77 77	0 0 0 0
High Temperature Storage (with Stored Patterns)	T_A=85°C	168 hours 500 hours 1000 hours	78 78 78	0 0 0

Table 8. Qualification Test Results – SNAPHAT Housing

Stress	Condition	Read-point	Samples	Failures
High Temperature Storage	140°C	1000 hours[1]	98	mean – 3.σ < 2.0 V
High Temperature Storage	125°C	1500 hours[1]	98	mean – 3.σ < 2.0 V
High Temperature Storage	100°C	2000 hours[1]	98	0
Brand Permanency	—	—	16	0
Physical Dimension	—	—	5	0
X-Ray	—	—	20	0

Notes: 1. Read-point indicates the last time that the units did not fail the failure criterion.

SOIC Stressing Results

Operational Life stressing did not produce failures. The M48T08 device used in this qualification is a mature, well documented product. The technology to manufacture this die was not the focus of this qualification. However interactions with the minor process changes from standard SOIC package manufacturing and the die were examined.

The temperature cycle test performed on the SOIC samples increased the sample size for this stress and allowed the measurement of parameters not tested in the module form such as Battery Current (I_{BAT}). No failures occurred in this stress.

HAST and autoclave were the critical tests to understand if the gold plated connectors would corrode and how resistant to moisture the package and die would be. Post stress, 30x examination of the female pins, which are attached to the SOIC package, resulted in neither corrosion, cracking, nor peeling of the gold plating.

With the determination of no electrical failures during stress and no evidence of post stress corrosion, the connection and package system chosen have been established to be very reliable.

In addition to qualification testing, a Failure Mode and Effects Analysis (FMEA) was documented. A process FMEA is used as a means to assure that, to the extent possible, potential manufacturing concerns have been considered and addressed. In its most rigorous form, an FMEA is a summary of the development of a process. This includes an analysis of experiences and past concerns. It then develops a list of potential failure modes ranked according to their effects on the final product, thus establishing a priority system for corrective action considerations. The FMEA is then reviewed and the risk factors reassessed as the corrective actions and controls are implemented and the process matures.

Table 9. Qualification Test Results – SOIC Package

Stress	Condition	Read-point	Samples	Failures
Operational Life	V_{CC}=7V, T_A=125°C	168 hours 500 hours 1000 hours	276 276 276	0 0 0
Temperature Cycling	–40°C to 125°C	300 cycles 600 cycles 1000 cycles 1300 cycles	102 102 102 102	0 0 0 0
HAST	T_A=131°C, RH=85%, V_{CC}=5.5V	92 hours 196 hours	44 44	0 0
Autoclave	T_A=121°C, RH=100%, unbiased	96 hours 240 hours	45 45	0 0
Resistance to Surface Mounting	See Table 6	215°C IR Reflow after T&H soak	10	0

FAILURE RATE CALCULATIONS

While adequate models for derating the accelerated test data for the various environmental stresses (T.H.B., Temperature Cycle, HAST) to actual use conditions are not available, the SOIC package 125°C Operating Life Test data has been derated to 55°C as shown in Table 10.

Table 10. Failure Rate Calculation

Test	Number Tested	Stress Device-hours	0.7eV Equiv. 55°C Device-hrs	Number of Failures	Failure Rate
Operational Life	276	276,000	21.3M	0	< 1 FIT

The stress hours were derated from 125°C to 55°C using the Arrhenius Model by assuming a 0.7 eV activation energy. This gives an estimated device failure rate at 55°C (Tj) of <1 FITs assuming:

- Arrhenius temperature acceleration of device hours from 125°C to 55°C = 77.4 for 0.7eV.
- Voltage Acceleration from V_{CC} = 7V to 5.5V = 90 using the Berman model for the oxide failures.
- Chi-Squared Failure Distribution, 60% UCL

SUMMARY AND CONCLUSIONS

After reviewing all of the qualification data, manufacturing support documentation, and corrective actions that are currently in place, the surface mount ZEROPOWER package has been released to manufacturing.

During the first three months of production, this product was sampled monthly by the ST Product Monitoring Program in order to assure continual product quality. Samples are now monitored quarterly. The data is published in the quarterly PMP Report published by the Carrollton Quality and Reliability group.

Table 11. Technical Description – Assembly

SOIC PACKAGE		
Small Outline Package Type	28 Pin (MH) 330 mil SOIC Package (JEDEC MO-059)	
Assembly Location	Carrollton, Texas	
Female pins	Shell finish:	200-400 microinches Tin over 100-150 microinches Nickel
	Contact finish:	30-35 microinches Gold over 50-100 microinches Nickel
Die Attach Adhesive	Ablestik 84-1 LMIS R4 Epoxy	
Leadframe	Copper with spot silver, Pad Size: 260 mils x460 mils	
Wire Bonding	1.0 mil Gold Thermosonic Bonding	
Molding Compound	Sumikon EME 6300HG	
Cure Conditions	175°C, 6 hours	
Lead Finish	Solder-plate, 85% tin, 15% lead	
SNAPHAT HOUSING		
Shell	General Electric Valox 420 SEO Thermoplastic	
Encapsulant	Hysol XES-0491	
Male pins	Brass Alloy 360, 1/2 hard with a plating finish of 30-35 microinches of Gold over and 50-100 microinches of Nickel.	

Table 12. Technical Description – Test

Test & Finishing Location	Carrollton, Texas
SOIC PACKAGE	
Preburn	100% 80°C AC-DC-Functional Test, Teradyne 386
Burn-in	24 hours, 125°C V_{CC} = 7V
Final Test 1	100% 80°C AC-DC-Functional Test, Teradyne 386
Final Test 2	100% 25°C AC-DC-Functional Test, Teradyne 386
Final QA Electrical	0.1% AQL; n=125, c=0 per lot 25°C, AC-DC-Functional Test
Final QA Visual	0.25% AQL; n=50, c=0 per lot
SNAPHAT HOUSING	
Final Test	Battery Voltage and Crystal impedance, 80°C, PC based tester using Lab View software.

Table 13. Revision History

Date	Description
Apr-1994	Document written
07-Dec-1999	Conversion to the new document template, and updated to the present tense

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apps.nvram@st.com (for application support)
ask.memory@st.com (for general enquiries)

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