74VCXH162373

LOW VOLTAGE 16-BIT D-TYPE LATCH (3-STATE) WITH 3.6V TOLERANT INPUTS AND OUTPUTS

PRELIMINARY DATA

- 3.6V TOLERANT INPUTS AND OUTPUTS
- HIGH SPEED:
  t_{PD} = 3.3 ns (MAX.) at V_{CC} = 3.0 to 3.6V
  t_{PD} = 4.5 ns (MAX.) at V_{CC} = 2.3 to 2.7V
- POWER-DOWN PROTECTION ON INPUTS AND OUTPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:
  $|I_{OH}| = I_{OL}$ = 12 mA (MIN) at V_{CC} = 3.0V
  $|I_{OH}| = I_{OL}$ = 8 mA (MIN) at V_{CC} = 2.3V
- 26Ω SERIE RESISTORS IN OUTPUTS
- OPERATING VOLTAGE RANGE:
  V_{CC} (OPR) = 1.8V to 3.6V
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 16373
- LATCH-UP PERFORMANCE EXCEEDS 300mA
- ESD PERFORMANCE:
  HBM >2000V; MM > 200V

T
(TSSOP48 Package)

ORDER CODES :
74VCXH162373T

DESCRIPTION

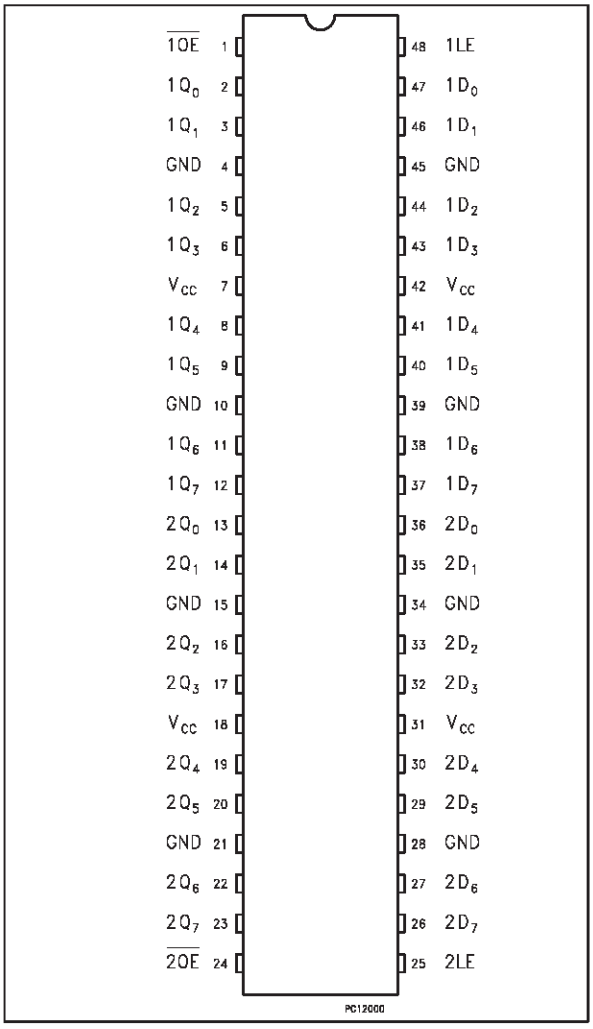
The VCXH162373 is a low voltage CMOS 16-BIT D-TYPE LATCH with 3 STATE OUTPUTS NON INVERTING fabricated with sub-micron silicon gate and five-layer metal wiring C2MOS technology. It is ideal for low power and very high speed 2.3 to 3.6V applications; it can be interfaced to 3.6V signal enviroment for both inputs and outputs.

These 16 bit D-Type latchs are byte controlled by two latch enable inputs (nLE) and two output enable inputs (OE). While the nLE input is held at a high level, the nQ outputs will follow the data input precisely. When the nLE is taken low, the nQ outputs will be latched precisely at the logic level of D input data. While the (nOE) input is low, the nQ outputs will be in a normal logic state (high or low logic level) and while high level the outputs will be in a high impedance state. This device is designed to be used with 3 state memory address drivers, etc.

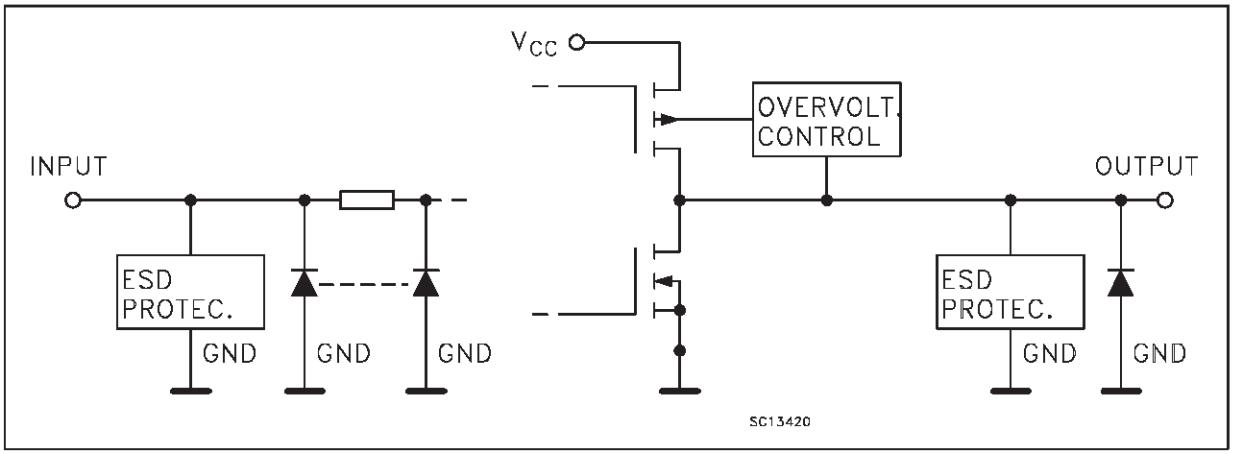
The device circuits is including 26Ω series resistance in the outputs. These resistors permit to reduce line noise in high speed applications.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

PIN CONNECTION



INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

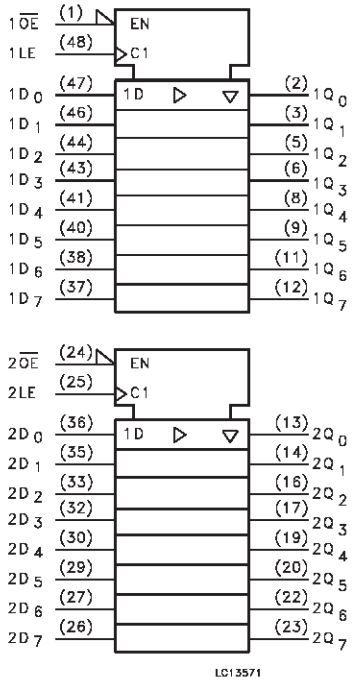
PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{1OE}$	3 State Output Enable Input (Active LOW)
2, 3, 5, 6, 8, 9, 11, 12	1Q0 to 1Q7	3 State Outputs
13, 14, 16, 17, 19, 20, 22, 23	2Q0 to 2Q7	3 State Outputs
24	$\overline{2OE}$	3 State Output Enable Input (Active LOW)
25	2LE	Latch Enable Input
36, 35, 33, 32, 30, 29, 27, 26	2D0 to 2D7	Data Inputs
47, 46, 44, 43, 41, 40, 38, 37	1D0 to 1D7	Data Inputs
48	1LE	Latch Enable Input
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive Supply Voltage

TRUTH TABLE

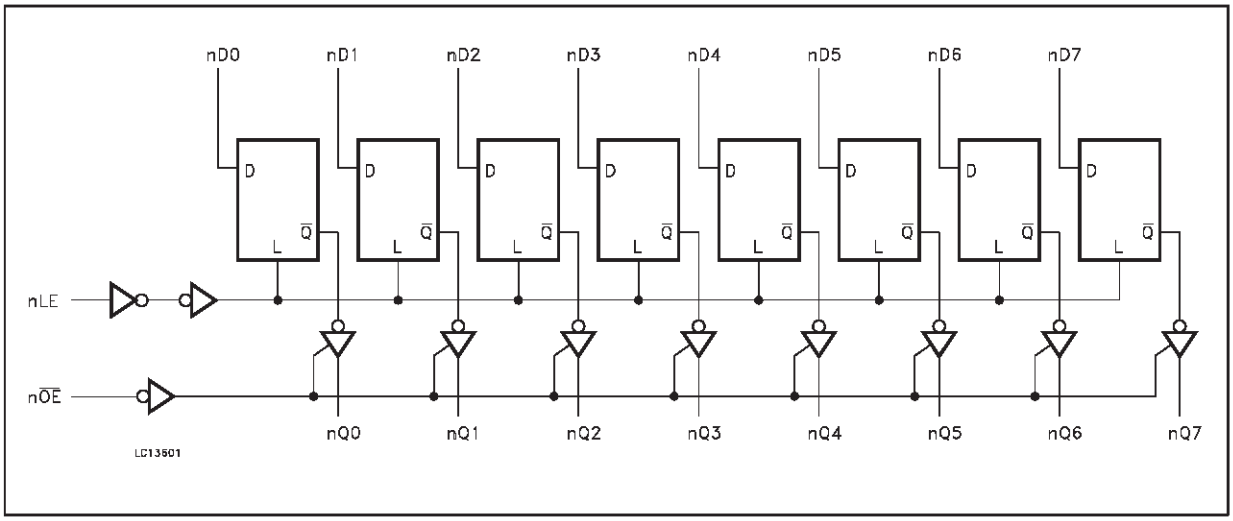
INPUTS			OUTPUTS
$\overline{OE}$	LE	D	Q
H	X	X	Z
L	L	X	NO CHANGE *
L	H	L	L
L	H	H	H

X: Don't care
Z: High impedance
* Q output are latched at the time when the LE input is taken low level.

IEC LOGIC SYMBOLS



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to + 4.6	V
V_I	DC Input Voltage	-0.5 to + 4.6	V
V_O	DC Output Voltage (OFF state)	-0.5 to + 4.6	V
V_O	DC Output Voltage (High or Low State) (note1)	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	- 50	mA
I_{OK}	DC Output Diode Current (note2)	± 50	mA
I_O	DC Output Source/Sink Current	± 50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current Per Supply Pin	± 100	mA
P_D	Power Dissipation	400	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
1) I_O absolute maximum rating must be observed
2) $V_O < GND$, $V_O > V_{CC}$

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2.3 to 3.6	V
V_I	Input Voltage	-0.3 to 3.6	V
V_O	Output Voltage (OFF state)	0 to 3.6	V
V_O	Output Voltage (High or Low State)	0 to V_{CC}	V
I_{OH}, I_{OL}	High or Low Level Output Current (V_{CC} = 3.0 to 3.6V)	± 12	mA
I_{OH}, I_{OL}	High or Low Level Output Current (V_{CC} = 2.3 to 2.7V)	± 8	mA
T_{op}	Operating Temperature:	-40 to +85	°C
dt/dv	Input Transition Rise or Fall Rate (V_{CC} = 3.0V) (note 1)	0 to 10	ns/V

1) V_{IN} from 0.8V to 2.0V, V_{CC} = 3.0V

DC SPECIFICATIONS (2.7V < V_{CC} ≤ 3.6V unless otherwise specified)

Symbol	Parameter	Test Conditions			Value		Unit
		V_{CC} (V)			-40 to 85 °C		
					Min.	Max.	
V_{IH}	High Level Input Voltage	2.7 to 3.6			2.0		V
V_{IL}	Low Level Input Voltage					0.8	V
V_{OH}	High Level Output Voltage	2.7 to 3.6	$V_I = V_{IH}$ or V_{IL}	I_O=-100 µA	V_{CC}-0.2		V
		2.7		I_O=-6 mA	2.2		
		3.0		I_O=-8 mA	2.4		
		3.0		I_O=-12 mA	2.2		
V_{OL}	Low Level Output Voltage	2.7 to 3.6	$V_I = V_{IH}$ or V_{IL}	I_O=100 µA		0.2	V
		2.7		I_O= 6 mA		0.4	
		3.0		I_O= 8 mA		0.55	
		3.0		I_O=12 mA		0.8	
I_I	Input Leakage Current	2.7 to 3.6	$V_I = V_{CC}$ or GND			±5	µA
$I_{I(HOLD)}$	Input Hold Current	3	V_I = 0.8 V		75		µA
			V_I = 2 V		-75		
		3.6	V_I = 0 to 3.6 V			±500	
I_{OZ}	3 State Output Leakage Current	2.7 to 3.6	$V_I = V_{IH}$ or V_{IL} V_O = 0 to 3.6V			±10	µA
I_{off}	Power Off Leakage Current	0	V_I or V_O = 0 to 3.6V			10	µA
I_{CC}	Quiescent Supply Current	2.7 to 3.6	$V_I = V_{CC}$ or GND			20	µA
			V_I or $V_O = V_{CC}$ to 3.6 V			±20	
ΔI_{CC}	ICC incr. per input	2.7 to 3.6	$V_{IH} = V_{CC}$ -0.6V			750	µA

DC SPECIFICATIONS (2.3V < V_{CC} ≤ 2.7V unless otherwise specified)

Symbol	Parameter	Test Conditions			Value		Unit
		V_{CC} (V)			-40 to 85 °C		
					Min.	Max.	
V_{IH}	High Level Input Voltage	2.3 to 2.7			1.6		V
V_{IL}	Low Level Input Voltage					0.7	V
V_{OH}	High Level Output Voltage	2.3 to 2.7	$V_I = V_{IH}$ or V_{IL}	I_O=-100 µA	V_{CC}-0.2		V
		2.3		I_O=-4 mA	2.0		
		2.3		I_O=-6 mA	1.8		
		2.3		I_O=-8 mA	1.7		
V_{OL}	Low Level Output Voltage	2.3 to 2.7	$V_I = V_{IH}$ or V_{IL}	I_O=100 µA		0.2	V
		2.3		I_O=6 mA		0.4	
		2.3		I_O=8 mA		0.6	
I_I	Input Leakage Current	2.3 to 2.7	$V_I = V_{CC}$ or GND			±5	µA
$I_{I(HOLD)}$	Input Hold Current	2.3	V_I = 0.7 V		45		µA
			V_I = 1.7 V		-45		
I_{OZ}	3 State Output Leakage Current	2.3 to 2.7	$V_I = V_{IH}$ or V_{IL} V_O = 0 to 3.6V			±10	µA
I_{off}	Power Off Leakage Current	0	V_I or V_O = 0 to 3.6V			10	µA
I_{CC}	Quiescent Supply Current	2.3 to 2.7	$V_I = V_{CC}$ or GND			20	µA
			V_I or $V_O = V_{CC}$ to 3.6 V			±20	

DYNAMIC SWITCHING CHARACTERISTICS ($T_a = 25^oC$, Input $t_r = t_f = 2.0ns$, $C_L = 30pF$, $R_L = 500\Omega$)

Symbol	Parameter	Test Conditions		Value			Unit
		V_{CC} (V)		$T_A = 25\ ^oC$			
				Min.	Typ.	Max.	
V_{OLP}	Dynamic Low Voltage Quiet Output (note 1, 3)	2.5	$V_{IL} = 0\ V$ $V_{IH} = V_{CC}$		0.25		V
		3.3			0.35		
V_{OLV}	Dynamic Low Voltage Quiet Output (note 1, 3)	2.5	$V_{IL} = 0\ V$ $V_{IH} = V_{CC}$		-0.25		V
		3.3			-0.35		
V_{OHV}	Dynamic High Voltage Quiet Output (note 2, 3)	2.5	$V_{IL} = 0\ V$ $V_{IH} = V_{CC}$		2.05		V
		3.3			2.65		

1) Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH to LOW or LOW to HIGH. The remaining output is measured in the LOW state.
2) Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH to LOW or LOW to HIGH. The remaining output is measured in the HIGH state.
3) Parameters guaranteed by design.

AC ELECTRICAL CHARACTERISTICS ($C_L = 30$ pF, $R_L = 500\ \Omega$, Input $t_r = t_f = 2.0$ ns)

Symbol	Parameter	Test Condition		Value		Unit
		V_{CC} (V)	Waveform	-40 to 85 °C		
				Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time Dn to Qn	2.3 to 2.7	3	1.0	4.5	ns
		3.0 to 3.6		0.8	3.3	
t_{PLH} t_{PHL}	Propagation Delay Time LE to Qn	2.3 to 2.7	1	1.0	4.9	ns
		3.0 to 3.6		0.8	3.6	
t_{PZL} t_{PZH}	Output Enable Time	2.3 to 2.7	2	1.0	5.4	ns
		3.0 to 3.6		0.8	3.9	
t_{PLZ} t_{PHZ}	Output Disable Time	2.3 to 2.7	2	1.0	4.4	ns
		3.0 to 3.6		0.8	4.0	
t_s	Setup Time, HIGH or LOW level Dn to LE	2.3 to 2.7	1	1.0		ns
		3.0 to 3.6		1.0		
t_h	Hold Time, HIGH or LOW level Dn to LE	2.3 to 2.7	1	1.0		ns
		3.0 to 3.6		1.0		
t_w	LE Pulse Width, HIGH	2.3 to 2.7	1	1.5		ns
		3.0 to 3.6		1.5		
t_{OSLH} t_{OSHL}	Output to Output Skew Time (note 1, 2)	2.3 to 2.7			0.5	ns
		3.0 to 3.6			0.5	

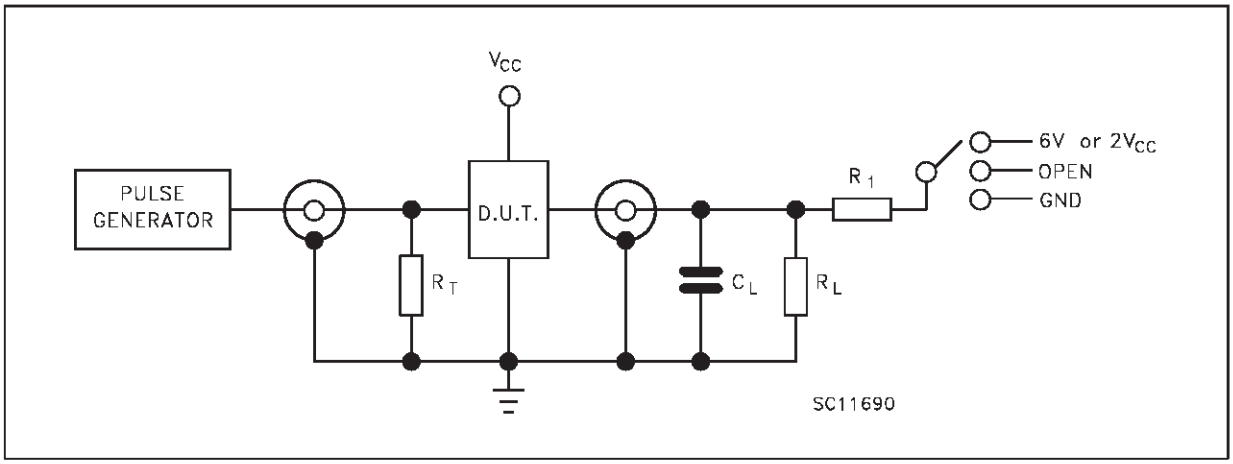
1) Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW ($t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$)
2) Parameter guaranteed by design

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions		Value			Unit
		V_{CC} (V)		$T_A = 25\ ^oC$			
				Min.	Typ.	Max.	
C_{IN}	Input Capacitance	2.5 or 3.3	$V_{IN} = 0V$ or V_{CC}		6		pF
C_{OUT}	Output Capacitance	2.5 or 3.3	$V_{IN} = 0V$ or V_{CC}		7		pF
C_{PD}	Power Dissipation Capacitance (note 1)	2.5 or 3.3	$f_{IN} = 10MHz$ $V_{IN} = 0V$ or V_{CC}		20		pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \bullet V_{CC} \bullet f_{IN} + I_{CC}/16$ (per circuit)

TEST CIRCUIT



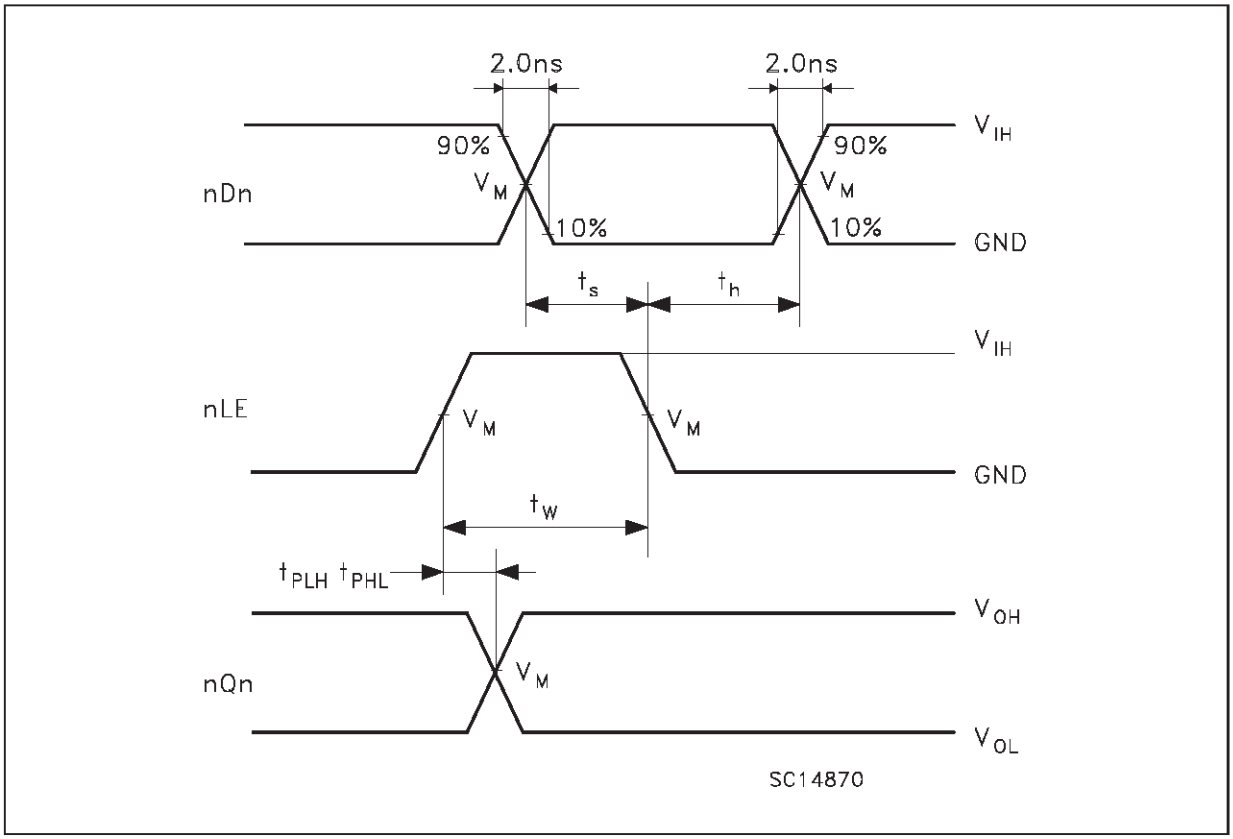
TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ} (V_{CC} = 3.0 to 3.6V)	6V
t_{PZL}, t_{PLZ} (V_{CC} = 2.3 to 2.7V)	$2V_{CC}$
t_{PZH}, t_{PHZ}	GND

C_L = 30 pF or equivalent (includes jig and probe capacitance)
$R_L = R_1$ = 500Ω or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

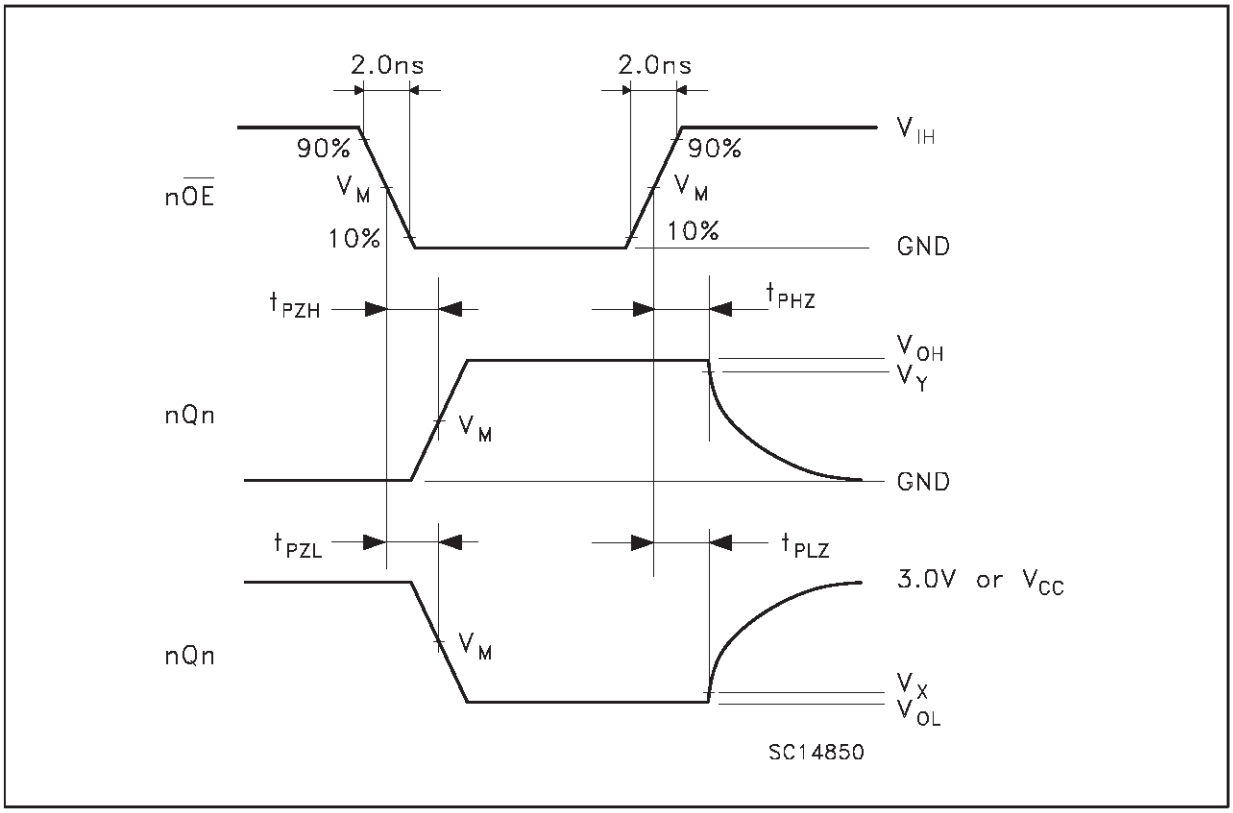
WAVEFORM SYMBOL VALUES

Symbol	V_{CC}	
	3.0 to 3.6V	2.3 to 2.7V
V_{IH}	2.7V	V_{CC}
V_M	1.5V	$V_{CC}/2$
V_X	V_{OL} + 0.3V	V_{OL} + 0.15V
V_Y	V_{OH} - 0.3V	V_{OH} - 0.15V

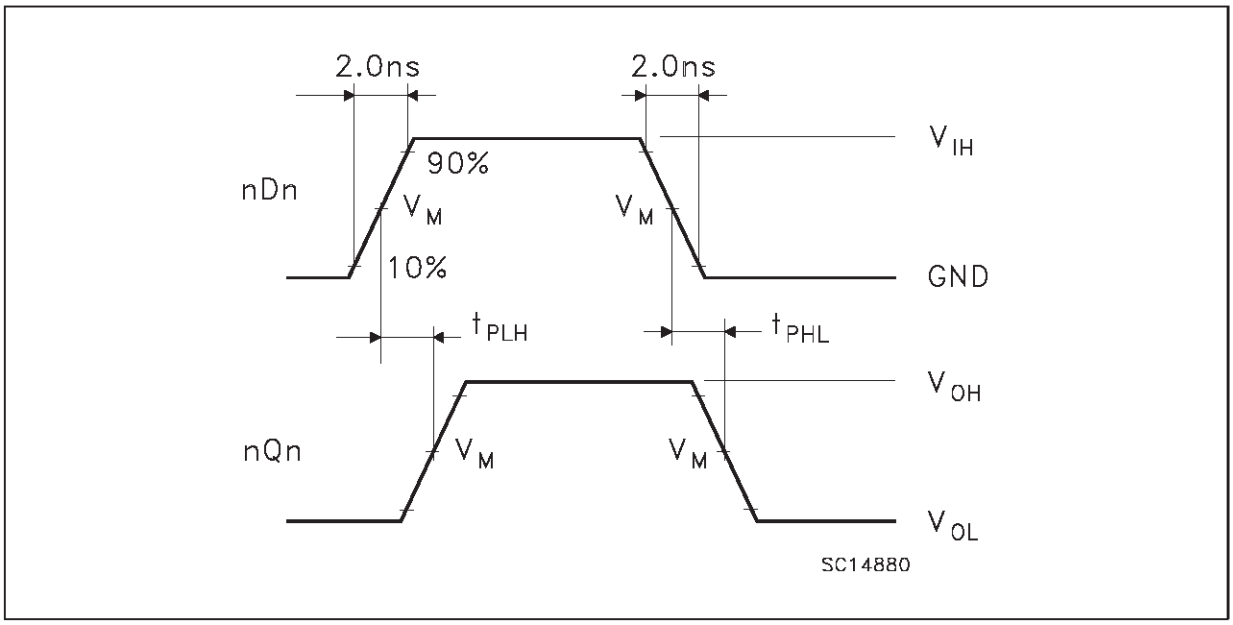
WAVEFORM 1: LE TO Qn PROPAGATION DELAYS, LE MINIMUM PULSE WIDTH, Dn TO LE SETUP AND HOLD TIMES (f=1MHz; 50% duty cycle)



WAVEFORM 2: OUTPUT ENABLE AND DISABLE TIMES (f=1MHz; 50% duty cycle)



WAVEFORM 3: PROPAGATION DELAY TIME (f=1MHz; 50% duty cycle)



TSSOP48 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.1			0.433
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.85	0.9	0.95	0.335	0.354	0.374
b	0.17		0.27	0.0067		0.011
c	0.09		0.20	0.0035		0.0079
D	12.4	12.5	12.6	0.408	0.492	0.496
E	7.95	8.1	8.25	0.313	0.319	0.325
E1	6.0	6.1	6.2	0.236	0.240	0.244
e		0.5 BSC			0.0197 BSC	
K	0^o	4^o	8^o	0^o	4^o	8^o
L	0.50	0.60	0.70	0.020	0.024	0.028