APPLICATION NOTE

USING THE ST62T6XC/5XC SPI IN MASTER MODE

by Microcontroller Application Team

1 INTRODUCTION

To avoid problems when switching from Rev B to Rev C devices, special attention must be paid to the programming of the I/O port Data Direction Register when using the SPI in master mode.

In Rev B devices, the SPI functions in master mode without depending on whether the DDR bit for the I/O port pin (PC4) used for the SCK is set or reset (programmed as input or output).

In Rev C devices, the DDR bit has to be programmed as INPUT (left at the reset value).

2 FUNCTIONAL DESCRIPTION

When the SPI is used in master mode, the SCK pin (PC4) and Sout pin (PC3) work in output mode and Sin pin (in input mode).

To enable the SPI in master mode, the SPCLK bit of the SPI mode control register has to be set.

By setting this bit, the SCK pin (PC4) is automatically configured in output push pull mode and the clock appears according to the base/bit clock selection.

The dedicated bit of the port C data direction register HAS TO REMAIN IN ITS RESET STATE (input mode); its configuration doesn't have to be changed.

The output of the SPI data register (Sout/PC3) is also automatically configured in output push pull by setting bit 0 of the MISCR register. The input of the SPI data register (Sin/PC2) can be configured in input with or without pull-up.

3 EXAMPLE

The following is a software example for SPI in master mode:

```
.org 080h

reset   clr X
clr A
ldi wdr,watchtim     ; Load the watchdog.
ldi ocr, 00h         ; set oscillator division to 1

ldi ddrc,00h
ldi orc,00h
ldi drc,00h          ; reset state

ldi drc,004h         ; pc2 in input without p-u ldi misc,001h
                     ; pc3 in output push pull

ldi spidiv,048h      ; 9 bits
ldi spimod,03Eh      ; pc4 in out p/p cpol=0 cpha=1 spin=0 ldi spidr,0aah
set 7,spimod         ; spirun

loop    jrs 7,spimod,loop ; poll end of transmission
```