APPLICATION NOTE
Upgrading From MK5027 to MK50H27

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The MK50H27 is a pin for pin replacement for the MK5027 with additional features and performance enhancements. Options such as TTC JT-Q703 protocol operation, Receive Signal Unit Timer, and on-chip watch dog timers are available by programming previously unused status register and Initialization block bits. It is important to note that even with the added options, the functionality and pin out of the MK5027 and MK50H27 are identical and the designer should not experience any difficulty or change of software substituting the MK50H27 for any revision of MK5027. Changes to software or hardware should only be required if some of the new features of the MK50H27 are to be used.

The following is the information regarding the changes made to the MK5027 to produce the new MK50H27 A02 device with optional TTC JT-Q703 protocol operation. The key points and items added are documented as follows:

1. JSS7E bit defined in CSR2 <08> to enable TTC JT-Q703 compliant operation of the device. With this bit set the MK50H27 will use only SIEs and T4e timer for alignment, and will conform to the JT-Q703 SS7 specifications for protocol actions. For TTC JT-Q703 compliant operation it is necessary to disable 2/3 FIB/BSN Error monitoring. The 2/3 FIB/BSN Error monitoring function can be disabled on the exiting MK5027 and on the MK50H27 by clearing bit 07 (2/3EN) in the Protocol Options field (IADR+26). When 2/3 FIB/BSN Error monitoring is disabled, an MSU will be discarded if its FIB does not match the BIB of the last sent SU.

2. JT-Q703 timers were added to the previously reserved section of the MK027 Init Block starting at IADR+144, as follows: IADR+144 - Tf, FISU Sending Interval IADR+146 - Ts, SIOS Sending Interval IADR+148 - To, SIO Sending Interval IADR+150 - Ta, SIE Sending Interval All of these timers are fully programmable 16-bit timers which are represented as two's complement numbers just like all of the existing MK5027 timers. These timers are scaled by the Pre-Scaler just like all of the other MK5027 timers such as the T5 timer (IADR+16) which controls the transmit frequency for SIB LSSUs.

3. An ESEN bit was implemented in CSR2<14> to enable use of a 16-bit Extended Scaler at IADR+24 rather than the existing 8-bit Scaler at IADR+02. This is done to allow programming of times longer than 27 seconds when using the MK50H27 with a SYSCLK of 25 MHz.

4. The MK50H27 has two additional User Primitives, UPRIM=17 to stop the sending of SIOS LSSUs during Out of Serivce, and UPRIM=16 to re-enable the sending of SIOS during Out of Serivce. The typical use of these primitives when operating in a TTC compliant mode would be to issue UPRIM 17 three seconds after deactivation and then issue UPRIM 16 prior to issuing UPRIM 7 to start initial alignment. Normally the MK50H27 will immediately start sending continuous SIOS when UPRIM 1 (Power On) is issued after the device is initialized.

5. On the 1984 and 1994 JT-Q703 specs that the maximum number of MSUs that can be transmitted without waiting for positive acknowledgement is 40. On the MK5027 this is a fixed value of 127 for ITU Q.703. So for the MK50H27 was added a TWS (Transmit Window Size) 7-bit field in the upper byte of IADR+44. The lower byte of IADR+44 continues to contain SBA<23:16> (upper byte of Status Buffer Address) as it does on the MK5027. The purpose of the TWS field is to limit the maximum number of outstanding MSUs that can be transmitted without acknowledgement. TTC JT-Q703 requires this limit be set to 40, but the MK50H27 will allow it to be fully programmable from 1-127. If TWS is set to 0x00 then its operation will be disabled for compatibility with code written for the MK5027 in which the upper byte of IADR+44 was reserved as all 0's.

6. Also, the 1984 and 1994 JT-Q703 specifies the use of Priority Indication Bits in the upper 2 bits of the LI octet. So Priority Indication bits were added to the RMD0 and TMD0 entries
of the Rx and Tx descriptor rings. The Priority Indication bits PrIn, RMD0<11:10> reflect the content of the Priority Indication bits of the received frame to which the RMD0 corresponds. The Priority Indication bits PrIn, TMD0<11:10> determine the content of the Priority Indication bits of the transmitted frame to which the TMD0 corresponds. According to JT-Q703 it is possible to transmit MSUs without indicating priority, in which case these bits would be fixed at 00. For non-TTC applications these bits are reserved as 0's as they are for the existing MK5027.

7. A feature added to the MK50H27, due to past experience of not being able to easily detect when a cable is disconnected, is a Receive Signal Unit Timer. This timer can be enabled or disabled and it is designed to expire after an extended period of time (32 x TP - Poll Timer) in which no SU's are received. In going from MK50H27 A01 to A02 revision, the Receive Signal Unit Timer (RSUT) was modified to allow operation during Processor Outage.

8. Because the MK50H27 is built on the MK50H2x family platform it also has the Watchdog Timers for TCLK and RCLK as on the MK50H25.

A. SUMMARY OF OPTION BITS ADDED TO MK50H27 A02

1. ARA - Auto Re-Align option - Bit 09 in CSR2 When this bit is 0 the MK50H27 A02 will automatically re-align upon receiving any out of service condition (other than a Stop primitive), as defined in JT-Q703. When this bit is 1, the MK50H27 A02 will require the issuance of a Start primitive in order to re-align after receipt of any out of service condition, but the protocol will still obey all JT-Q703 operation if JSS7E=1. This bit has no effect if JSS7E=0.

2. JOSRA - Japanese Out of Service Re-Align - Bit 10 in CSR2 When this bit is 1, the MK50H27 A02 upon receiving any out of service condition (including a Stop primitive), will actually go to an Out of Service state/phase in which SIOS will be transmitted. This is essentially the ITU Q.703 required behaviour upon receiving any out of service condition. When JOSRA=0 the out of service operation will behave according to JT-Q703 if JSS7E=1 (see item 6).

3. ANSIT6/T7 - ANSI Compliant T6 & T7 Timer Operation - Bit 09 of PROTOCOL OPTIONS (located at IADR + 26). When this bit is 1 the MK50H27 A02 T6 & T7 timer operation will comply with the ANSI T1.111.3 specifications. When this bit is 0 the MK50H27 A02 T6 &
T7 timer operation will comply with the ITU / CCITT Q.703 specifications.

B. SUMMARY OF FIRMWARE CHANGES (Items 1-7 are for JSS7E=1 and JOSRA=0 unless otherwise indicated)

1. If JSS7E=1, the MK50H27 A02 upon receiving a SIE or SIO while in the "IN SERVICE" state will cause the device to give a Out Of Service indication to MTP3 and change state to "Initial_alignment Aligned". Then, depending upon the setting of a ARA (Auto Re-Alignment) option bit, the device will either automatically attempt to align (by sending SIE), or it will wait for a Re-Align Primitive to be given in order for it to attempt to re-align by sending SIE.

2. If JSS7E=1, the MK50H27 A02 upon receiving a SIO while in "PROVING" or "PROVED" states will cause the device to change state to "Initial_alignment Aligned". Then the device will either automatically attempt to re-align (by sending SIE).

3. If JSS7E=1, the MK50H27 A02 upon receiving a SIOS, excessive errors, or a T6 or T7 Time Out while "IN SERVICE" will cause the device to give a Out Of Service indication to MTP3 and change state to "Initial_alignment Not Aligned". Then, depending upon the setting of a ARA (Auto Re-Alignment) option bit, the device will either automatically attempt to align (by sending SIO), or it will wait for a Re-Align Primitive to be given in order for it to attempt to re-align by sending SIO.

4. If JSS7E=1, the MK50H27 A02 upon receiving a SIOS, or excessive errors while in "PROVING" or "PROVED" states (or T3 timeout in "Initial_alignment Aligned" state) will cause the device to give a Alignment Out Of Service indication to MTP3 and change state to "Initial_alignment Not Aligned". Then, depending upon the setting of ARA (Auto Re-Alignment) option bit, the device will either automatically attempt to align (by sending SIO), or it will wait for a Re-Align Primitive to be given in order for it to attempt to re-align by sending SIO.

Note: *In all of the above cases 1 - 4, the BIB, BSN, FIB, and FSN values will remain as they were prior to the out of service condition (they will NOT be reset to FIB/BIB=1 and FSN/BSN=127). In these cases, if JSS7E=1, the MK50H27 A02 will use the values of FIB and FSN from the first received SIE in the re-alignment as the BIB and BSN values for the remaining SIE to be transmitted. The only time the BIB, BSN, FIB, and FSN values will will be reset to FIB/BIB=1 and FSN/BSN=127, is when aligning after a Stop and/or Power Off primitive has been issued to the MK50H27.*

5. If JSS7E=1, the only time that SIOS will be transmitted is upon initial power on (after Power On primitive has been issued) or after a Stop primitive has been issued to the MK50H27 A02.
6. If JSS7E=1, the MK50H27 A02 will allow the issuance of the "Retrieve BSNT" and "Retreival Request and FSNC" primitives in all states not only in "OUT-OF-SERVICE" state. If the retreival process is attempted while not Out Of Service, the MK50H27 will clear the RXON bit (CSR0 bit 10) when the "Retrieve BSNT" primitive is issued, and it will not set it back to 1 until the "Retreival Request and FSNC" primitive has completed the retreival process. In this manner the RXON bit will essentially serve as the "Link_switching" flag. It should be noted that while the MK50H27 is In Service and RXON=0, the MK50H27 will not receive any MSUs and will send SIB in response to any incomming MSU.

7. A JOSRA option bit has been added to the the MK50H27 A02 to cause the following behaviour when

JSS7E=1 and JOSRA=1.

a. Receiving a SIE or SIO while in the ”IN SERVICE” state will cause the device to: I - Send Out Of Service indication to MTP3 (PPRIM 9 will be used). II - Perform exactly the same procedure as if a ”stop” were received from MTPL3. (Fig. 13-2/JT-Q703(4/4) Link State Control). This involves sending ”Stop” to SUERM, sending ”Stop” to RC, C:=0, Start Ts, sending ”Send SIOS” to TXC, and changing state to ”OUT-OF-SERVICE”. III- The device will remain in this state until a Start Primitve is received, which will cause the device to re-align by sending SIO.

b. Receiving a SIO while in ”PROVING” or ”PROVED” states will cause the device to change state to ”Initial_alignment Aligned” and to automatically attempt to align (by sending SIE), without sending any signal to MTPL3.

c. Receiving a SIOS, excessive errors or a T6 or T7 Time Out while ”IN SERVICE” will cause the device to :

I - Send Out Of Service indication to MTP3 (PPRIM 9 will be used).
II - Perform exactly the same procedure as if a ”stop” were received from MTPL3. (Fig. 13-2/JT-Q703(4/4) Link State Control. This involves sending ”Stop” to SUERM, sending ”Stop” to RC, C:=0, Start Ts, sending ”Send SIOS” to TXC, and changing state to ”OUT-OF-SERVICE”.

III- The device will remain in this state until a Start Primitve is received, which will cause the device to re-align by sending SIO.

d. Receiving an SIOS or excessive errors while in ”PROVING” or ”PROVED” states , or T3 timeout in ”Initial_alignment Aligned” state will cause the device to: I - Give a Alignment Out Of Service indication to MTP3 (PPRIM 6 ”JT-Q703 Alignment Out of Service Indication” will be used) II - Change state to ”Initial_alignment Not Aligned”. III- Depending upon the setting of a ARA (Auto Re-Alignment) option bit, the device will either automatically attempt to align (by sending SIO), or it will wait for a Re-Align Primitive to be given in order for it to attempt to realign by sending SIO.

e. For JOSRA=1, in the cases a - d, the BIB, BSN, FIB, and FSN values will be reset to FIB/BIB=1 and FSN/BSN=127 upon issuance of the Start primitive from MTP3. During alignment procedure, the MK50H27 A02 will use the values of FIB and FSN from the first received SIE in the re-alignment as the BIB and BSN values for the remaining SIE to be transmitted. FIB and FSN, however, will keep their reset values during and after alignment.

f. For JOSRA=1 option, SIOS is send if and only if: I - ”Stop” is received from MTPL3 in any state (including ”IN SERVICE”). II - SIOS, SIO, SIE, excessive error, T7 time out or T6 time out is received in the state ”IN SERVICE”.

g. If JSS7E=1, the MK50H27 A02 will allow the issuance of the ”Retrieve BSNT” and ”Retreival

Request and FSNC" primitives in all states not only in "OUT-OF-SERVICE" state. If the retreival process is attempted while not Out Of Service, the MK50H27 will clear the RXON bit (CSR0 bit 10) when the "Retrieve BSNT" primitive is issued, and it will not set it back to 1 until the "Retreival Request and FSNC" primitive has completed the retreival process. In this manner the RXON bit will essentially serve as the "Link_switching" flag. It should be noted that while the MK50H27 is In Service and RXON=0, the MK50H27 will not receive any MSUs and will send SIB in response to any incomming MSU.

9. To comply with TTC JT-Q703, AERM was modified when JSS7E=1 so that T4 timer is not immediately restarted upon receiving a SU Error condition. T4 is instead restarted after a T4 time period has elapsed in which a SU Error was received. Also Alignment Failure due to AERM is not indicated (by a PPRIM) until after L (same as M parameter in MK50H27 Init Block) consecutive aborted proving periods.

The MK50H27 is designed to allow users of the MK5027 A09 device to be able to upgrade to the MK50H27 without any change in their code or hardware, unless they want to use some of the many additional features offered by the MK50H27.

SUMMARY OF MK50H27 A02 TO A03 CHANGES

The MK50H27 A03 incorporates the following changes as compared to the MK50H27 A02 device:

1. The firmware controlling the Poll Timer, TP, was modified to provide more reliable operation of TP in Transparent Mode. Its operation in SS7 protocol operation remains unaffected.

2. An option bit bas added to CSR2 (bit 11) to allow the device to ignore 2 byte LSSUs. When bit 11 of CSR2 is set, 2 byte LSSUs will be ignored by the MK50H27 A03 device. When JSS7E=1, the setting of CSR2 bit 11 will also cause MSUs received with bad BSN to be ignored. (This is an option that can be useful to pass certain TTC JT-Q703 compliance tests).

3. Received signal units larger than m (Maximum Frame Length, IADR+34) will be treated as bad and cause the SUERM to be incremented, even if Octet Counting is disabled, as is the case when operating in TTC JT-Q703 mode (CSR2, JSS7E=1). The MK50H27 A02 ignored SUs larger than m if Octet Counting was disabled. This change has no effect on the operation of the MK50H27 A03 for normal CCITT SS7.

4. For Japanese SS7 mode of operation (CSR2, JSS7E=1), the MK50H27 A03 will NACK duplicate MSUs (MSUs received with the same FSN) according to TTC JT-Q703. (This change was needed to pass certain TTC JT-Q703 compliance tests).

The changes made in going from MK50H27 revision A02 to A03 were mainly done to allow the device to more fully comply with TTC JT-Q703 compliance tests, and should have no effect on the use of the device for normal CCITT SS7 operation.

MK50H27 A02 users who do not use the device in Japanese SS7 applications should see no difference between the operation of the MK50H27 A02 and A03 devices.