QRR9902
QUALITY & RELIABILITY REPORT

July 1998 to June 1999 - EPROM, Flash Memory, EEPROM and NVRAM Products

INTRODUCTION

STMicroelectronics manufactures a wide range of memory types which include:

Non-volatile memories: Flash memory, UV EPROM, OTP EPROM and EEPROMs. EPROM products are manufactured in both 1.5µm NMOS and 0.8µm to 0.35µm CMOS technology; Flash memories in 0.8µm to 0.35µm CMOS technology; OTP EPROMs in 0.8µm to 0.35µm and EEPROMs in 1.2µm to 0.6µm CMOS technology.

Packages for non-volatile memories include both ceramic FDIP and plastic PDIP, PLCC, SO and TSOP.

Non-volatile RAM: ZEROPOWER and TIMEKEEPER ranges are manufactured in 1.2-0.7µm HCMOS technology.

Packages for ZEROPOWER and TIMEKEEPER products use a modified PDIP or SO with an additional "top hat" assembly mounted above and containing a Lithium battery and optionally a quartz crystal. The battery and crystal are sealed in the plastic cap with a plastic resin.

The results presented in this quarterly report cover the tests made from July 1998 to June 1999. Regular reports are issued each quarter with the last years cumulative results.

Director of
Memory Products Group
Quality Control & Reliability

Attilio PANCHIERI

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CONTENT

Table 1. Final Average Outgoing Quality (AOQ)
July 1998 to June 1999

Process	Electrical ppm				Visual ppm			
	3Q98	4Q98	1Q99	2Q99	3Q98	4Q98	1Q99	2Q99
UV EPROM								
CMOS	7	4	6	5	12	9	8	8
NMOS	0	0	0	0	20	0	0	0
OTP EPROM								
CMOS	19	14	20	19	6	5	13	9
FLASH								
CMOS	9	8	3	2	5	12	12	10
NVRAM								
CMOS	0	0	0	0	0	0	5	0
EEPROM								
CMOS	7	3	2	5	2	7	11	5

Table 2. Failure Rate Predictions (Fit)
July 1998 to June 1999

Process	Actual Device hrs		Temperature Activation Energy (eV)	Voltage Acceleration Factor	Equivalent hrs 55 °C (x 10^6)	Life Test Failure	Failure Rate (Fit) Confidence Level	
	Dev. hrs (x 10^6)	Temp. (°C)					60%	90%
UV EPROM								
CMOS E5 -35%	1.037	140	0.6	4.0	285	0	3.2	8.1
CMOS E6 -10%	3.787	140	0.6	4.0	1,039	0	0.9	2.2
OTP EPROM								
CMOS E5 -35%	2.000	140	0.6	4.0	518	0	1.8	4.4
CMOS E6 -10%	2.400	140	0.6	4.0	622	0	1.5	3.7
FLASH								
CMOS T5 -20%	2.338	140	0.6	4.0	606	0	1.5	3.8
CMOS T6	21.260	140	0.6	4.6	6,336	0	0.14	0.36
CMOS T6X -35%	4.327	140	0.6	4.6	1,290	0	0.7	1.8
EEPROM								
CMOS F4S	2.542	140	0.6	3.0	598	0	1.5	3.8
CMOS F6SP	3.645	140	0.6	4.6	1,315	0	0.7	1.8
NVRAM								
HCMOS S3	1.470	100	0.7	64	1,882	0	0.5	1.2
HCMOS 4DZ	0.877	125	0.7	6.0	405	1	4.9	9.5

Table 3. NMOS E3/1.5µm Process UV EPROM Reliability Data, Die Related Tests
July 1998 to June 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M2764A		M27128		M27256		M27512	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,								
		– 48 hrs	735	0	80	0	-	-	520	0
		– 168 hrs	610	0	80	0	-	-	80	0
		– 500 hrs	610	0	80	0	-	-	80	0
		– 1000 hrs	610	0	80	0	-	-	-	-
Retention Bake	1008	250°C,								
		– 48 hrs	610	0	80	0	-	-	80	0
		– 168 hrs	610	0	80	0	-	-	80	0
		– 500 hrs	610	0	80	0	-	-	80	0

Table 4. CMOS E5/0.8µm Process UV EPROM Reliability Data, Die Related Tests
July 1998 to June 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C64A	
			Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz, – 48 hrs – 168 hrs – 500 hrs – 1000 hrs	 77 - - -	 0 - - -
Retention Bake	1008	250°C, – 48 hrs – 168 hrs – 500 hrs	 - - -	 - - -

Table 5. CMOS E5/0.6µm Process (–35% upgrade) UV EPROM Reliability Data, Die Related Tests
July 1998 to June 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C256 (D) M87C257 (D)		M27C512 (D)		M27C801 (D)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,						
		– 48 hrs	4,343	0	5,706	0	80	0
		– 168 hrs	390	0	470	0	80	0
		– 500 hrs	390	0	470	0	80	0
		– 1000 hrs	390	0	470	0	80	0
Retention Bake	1008	250°C,						
		– 48 hrs	390	0	470	0	80	0
		– 168 hrs	390	0	470	0	80	0
		– 500 hrs	390	0	470	0	80	0

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 6. CMOS E6/0.6µm Process (–10% upgrade) UV EPROM Reliability Data, Die Related Tests
July 1998 to June 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C1001 (F)		M27C1024 (F)		M27C2001 (F)		M27C4001 (F)		M27C4002 (F)		M27C801 (F)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,												
		– 48 hrs	1,454	0	377	0	784	0	941	0	790	0	11,192	0
		– 168 hrs	530	0	300	0	630	0	710	0	790	0	790	0
		– 500 hrs	530	0	300	0	630	0	710	0	630	0	790	0
		– 1000 hrs	530	0	300	0	630	0	710	0	630	0	790	0
Retention Bake	1008	250°C,												
		– 48 hrs	530	0	300	0	630	0	710	0	790	0	790	0
		– 168 hrs	530	0	300	0	630	0	710	0	790	0	790	0
		– 500 hrs	530	0	300	0	630	0	710	0	630	0	790	0

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 7. CMOS E6DM/0.6µm Process UV EPROM Reliability Data, Die Related Tests
July 1998 to June 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C4001 (F)		M27C800 (F)		M27C160 (F)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,						
		– 48 hrs	-	-	1,822	0	2,765	0
		– 168 hrs	-	-	80	0	120	0
		– 500 hrs	-	-	80	0	120	0
		– 1000 hrs	-	-	80	0	120	0
Retention Bake	1008	250°C,						
		– 48 hrs	-	-	80	0	120	0
		– 168 hrs	-	-	80	0	120	0
		– 500 hrs	-	-	80	0	120	0

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 8. CMOS E6DM/0.5µm Process (-15% upgrade) UV EPROM Reliability Data, Die Related Tests
July 1998 to June 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C160 (F)	
			Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz, – 48 hrs – 168 hrs – 500 hrs – 1000 hrs	 3,596 240 240 160	 0 0 0 0
Retention Bake	1008	250°C, – 48 hrs – 168 hrs – 500 hrs	 240 240 240	 0 0 0

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 9. CMOS E6/0.35µm Process (-30% upgrade) UV EPROM Reliability Data, Die Related Tests
July 1998 to June 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C256 (F)		M27C801 (F)		M27C320 (F)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,						
		– 48 hrs	282	0	1,704	0	5,477	0
		– 168 hrs	80	0	80	0	80	0
		– 500 hrs	80	0	-	-	80	0
		– 1000 hrs	-	-	-	-	-	-
Retention Bake	1008	250°C,						
		– 48 hrs	80	0	80	0	80	0
		– 168 hrs	80	0	80	0	80	0
		– 500 hrs	80	0	-	-	-	-

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 10. UV EPROM Reliability Data, Package Related Tests (Ceramic Frit-Seal)
July 1998 to June 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	Samp.	Fail
Temperature Cycling	1010	–65 to 150°C, – 100 cycles – 500 cycles – 1000 cycles	 3,705 3,655 3,275	 0 0 0
– Fine Leak – Gross Leak	1014 1014	Test Condition A1 Test Condition C1		
Solderability	2003	245°C, 5sec, Precondition Steam, 1hr	1,110	0
Resistance to Solvents	2015	4 Solvent Solutions	248	0
Lead Integrity	2004	Test Condition B2 (lead fatigue)	184	0
– Fine Leak – Gross Leak	1014 1014	Test Condition A1 Test Condition C1		

Table 11A. CMOS E5/0.6µm Process (–35% upgrade) OTP EPROM Reliability Data, Die Related Tests
July 1998 to June 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C256 (D) M87C257 (D)		M27C512 (D)		M27C516 (D)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,						
		– 168 hrs	450	0	810	0	240	0
		– 500 hrs	450	0	810	0	240	0
		– 1000 hrs	450	0	690	0	240	0
Retention Bake	1008	150°C,						
		– 168 hrs	450	0	790	0	240	0
		– 500 hrs	450	0	790	0	240	0
		– 1000 hrs	450	0	750	0	240	0

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 11B. CMOS E5/0.6µm Process (–35% upgrade) OTP EPROM Reliability Data, Die Related Tests
July 1998 to June 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C1001 (D)		M27C1024 (D)		M27C2001 (D)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,						
		– 168 hrs	180	0	180	0	230	0
		– 500 hrs	180	0	180	0	230	0
		– 1000 hrs	180	0	120	0	230	0
Retention Bake	1008	150°C,						
		– 168 hrs	180	0	120	0	230	0
		– 500 hrs	180	0	120	0	230	0
		– 1000 hrs	180	0	120	0	230	0

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 12A. CMOS E5/0.6µm Process (–35% upgrade) OTP EPROM Reliability Data, Package Related Tests
July 1998 to June 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C256 (D) M87C257 (D)		M27C512 (D)		M27C516 (D)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,						
		– 168 hrs	450	0	730	0	240	0
		– 500 hrs	450	0	730	0	240	0
		– 1000 hrs	450	0	690	0	240	0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,						
		– 48 hrs	185	0	310	0	100	0
		– 96 hrs	185	0	310	0	100	0
		– 168 hrs	185	0	310	0	100	0
		– 240 hrs	40	0	65	0	75	0
Pressure Pot		121°C, 2Atm,						
		– 48 hrs	450	0	750	0	240	0
		– 96 hrs	450	0	750	0	240	0
		– 168 hrs	450	0	750	0	240	0
		– 240 hrs	450	0	750	0	240	0
Temperature Cycling	1010	–65 to 150°C,						
		– 100 cycles	340	0	580	0	240	0
		– 500 cycles	340	0	580	0	240	0
		– 1000 cycles	340	0	580	0	240	0
Solderability								
– PLCC/TSOP Packages	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	(See cumulative data on Table 12B)					
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	(See cumulative data on Table 12B)					

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 12B. CMOS E5/0.6µm Process (–35% upgrade) OTP EPROM Reliability Data, Package Related Tests
July 1998 to June 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C1001 (D)		M27C1024 (D)		M27C2001 (D)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,						
		– 168 hrs	180	0	120	0	230	0
		– 500 hrs	180	0	120	0	230	0
		– 1000 hrs	180	0	120	0	230	0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,						
		– 48 hrs	75	0	50	0	95	0
		– 96 hrs	75	0	50	0	95	0
		– 168 hrs	75	0	50	0	95	0
		– 240 hrs	25	0	25	0	70	0
Pressure Pot		121°C, 2Atm,						
		– 48 hrs	180	0	120	0	230	0
		– 96 hrs	180	0	120	0	230	0
		– 168 hrs	180	0	120	0	230	0
		– 240 hrs	180	0	120	0	230	0
Temperature Cycling	1010	–65 to 150°C,						
		– 100 cycles	180	0	120	0	230	0
		– 500 cycles	180	0	120	0	230	0
		– 1000 cycles	180	0	120	0	230	0
Solderability								
– PLCC/TSOP Packages	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	Cumulative Sample/Fail = 770/0					
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	Cumulative Sample/Fail = 90/0					

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 13. CMOS E6/0.6µm Process (–10% upgrade) OTP EPROM Reliability Data, Die Related Tests
July 1998 to June 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C1001 (F)		M27C1024 (F)		M27C2001 (F)		M27C4001 (F)		M27C4002 (F)		M27C801 (F)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,												
		– 168 hrs	990	0	390	0	170	0	470	0	400	0	120	0
		– 500 hrs	990	0	390	0	110	0	470	0	400	0	120	0
		– 1000 hrs	870	0	390	0	110	0	410	0	400	0	120	0
Retention Bake	1008	150°C,												
		– 168 hrs	990	0	390	0	180	0	470	0	400	0	120	0
		– 500 hrs	990	0	390	0	120	0	470	0	400	0	120	0
		– 1000 hrs	870	0	390	0	120	0	410	0	400	0	120	0

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 14A. CMOS E6/0.6µm Process (–10% upgrade) OTP EPROM Reliability Data, Package Related Tests
July 1998 to June 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C1001 (F)		M27C1024 (F)		M27C2001 (F)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,						
		– 168 hrs	990	0	390	0	180	0
		– 500 hrs	990	0	390	0	120	0
		– 1000 hrs	870	0	390	0	120	0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,						
		– 48 hrs	410	0	160	0	70	0
		– 96 hrs	410	0	160	0	70	0
		– 168 hrs	410	0	160	0	70	0
		– 240 hrs	70	0	40	0	-	-
Pressure Pot		121°C, 2Atm,						
		– 48 hrs	990	0	390	0	110	0
		– 96 hrs	990	0	390	0	110	0
		– 168 hrs	990	0	390	0	110	0
		– 240 hrs	930	0	390	0	110	0
Temperature Cycling	1010	–65 to 150°C,						
		– 100 cycles	990	0	390	0	170	0
		– 500 cycles	990	0	390	0	110	0
		– 1000 cycles	810	0	390	0	110	0
Solderability								
– PLCC Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	(See cumulative data on Table 14B)					
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs						

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 14B. CMOS E6/0.6µm Process (–10% upgrade) OTP EPROM Reliability Data, Package Related Tests
July 1998 to June 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C4001 (F)		M27C4002 (F)		M27C801 (F)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,						
		– 168 hrs	470	0	400	0	120	0
		– 500 hrs	470	0	400	0	120	0
		– 1000 hrs	410	0	400	0	120	0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,						
		– 48 hrs	195	0	165	0	50	0
		– 96 hrs	195	0	165	0	50	0
		– 168 hrs	195	0	165	0	50	0
		– 240 hrs	25	0	65	0	-	-
Pressure Pot		121°C, 2Atm,						
		– 48 hrs	470	0	400	0	120	0
		– 96 hrs	470	0	400	0	120	0
		– 168 hrs	470	0	400	0	120	0
		– 240 hrs	470	0	400	0	120	0
Temperature Cycling	1010	–65 to 150°C,						
		– 100 cycles	410	0	400	0	120	0
		– 500 cycles	410	0	400	0	120	0
		– 1000 cycles	350	0	400	0	120	0
Solderability								
– PLCC Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	Cumulative Sample/Fail = 268/0					
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs						

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 15. CMOS E6DM/0.6µm Process OTP EPROM Reliability Data, Die Related Tests
July 1998 to June 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C4001 (F)		M27C800 (F)		M27C160 (F)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,						
		– 168 hrs	60	0	-	-	120	0
		– 500 hrs	60	0	-	-	120	0
		– 1000 hrs	60	0	-	-	120	0
Retention Bake	1008	150°C,						
		– 168 hrs	60	0	-	-	120	0
		– 500 hrs	60	0	-	-	120	0
		– 1000 hrs	60	0	-	-	120	0

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 16. CMOS E6DM/0.6µm Process OTP EPROM Reliability Data, Package Related Tests
July 1998 to June 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C4001 (F)		M27C800 (F)		M27C160 (F)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,						
		– 168 hrs	60	0	-	-	120	0
		– 500 hrs	60	0	-	-	120	0
		– 1000 hrs	60	0	-	-	120	0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,						
		– 48 hrs	25	0	-	-	50	0
		– 96 hrs	25	0	-	-	50	0
		– 168 hrs	25	0	-	-	50	0
		– 240 hrs	25	0	-	-	50	0
Pressure Pot		121°C, 2Atm,						
		– 48 hrs	60	0	-	-	120	0
		– 96 hrs	60	0	-	-	120	0
		– 168 hrs	60	0	-	-	120	0
		– 240 hrs	60	0	-	-	120	0
Temperature Cycling	1010	–65 to 150°C,						
		– 100 cycles	60	0	-	-	120	0
		– 500 cycles	60	0	-	-	120	0
		– 1000 cycles	60	0	-	-	120	0
Solderability								
– PLCC/TSOP Packages	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	Cumulative Sample/Fail = 92/0					
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	Cumulative Sample/Fail = 36/0					

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 17. CMOS E6DM/0.5µm Process (-15% upgrade) OTP EPROM Reliability Data, Die Related Tests
July 1998 to June 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C160 (F)	
			Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz, – 168 hrs – 500 hrs – 1000 hrs	 120 60 -	 0 0 -
Retention Bake	1008	150°C, – 168 hrs – 500 hrs – 1000 hrs	 120 60 -	 0 0 -

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 18. CMOS E6DM/0.5µm Process (-15% upgrade) OTP EPROM Reliability Data, Package Related Tests
July 1998 to June 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C160 (F)	
			Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs	 - - -	 - - -
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V, – 48 hrs – 96 hrs – 168 hrs – 240 hrs	 - - - -	 - - - -
Pressure Pot		121°C, 2Atm, – 48 hrs – 96 hrs – 168 hrs – 240 hrs	 120 120 120 120	 0 0 0 0
Temperature Cycling	1010	–65 to 150°C, – 100 cycles – 500 cycles – 1000 cycles	 60 60 60	 0 0 0
Solderability				
– PLCC/TSOP Packages	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	(See cumulative data on Table 14B)	
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	(See cumulative data on Table 14B)	

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 19. CMOS T5/0.8µm Process (–20% upgrade) Flash Memory Reliability Data, Die Related Tests
July 1998 to June 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F256 (B)		M28F512 (B)		M28F101 (B)		M28F102 (B)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test (1)	1005	140°C, V_{CC} = 6V,f = 500kHz,								
		– 24 hrs	-	-	1,557	0	7,842	0	7,362	0
		– 168 hrs	-	-	895	0	1,700	0	1,220	0
		– 500 hrs	-	-	640	0	700	0	470	0
		– 1000 hrs	-	-	640	0	520	0	410	0
Retention Bake (1)	1008	150°C,								
		– 168 hrs	-	-	760	0	610	0	410	0
		– 500 hrs	-	-	700	0	610	0	410	0
		– 1000 hrs	-	-	640	0	490	0	410	0
Retention Bake	1008	250°C,								
		– 168 hrs	-	-	-	-	376	0	60	0
		– 500 hrs	-	-	-	-	376	0	60	0
		– 1000 hrs	-	-	-	-	376	0	-	-
Write/Erase Cycling		1,000 cycles	128	0	3,798	0	4,512	0	7,099	0
		10,000 cycles	-	-	-	-	608	0	-	-
Retention Bake	1008	150°C, 36 hrs	128	0	3,798	0	3,904	0	7,099	0

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.
1. A quarter of sample size was subjected to 10,000 Write/Erase cycles before operating life test and retention bake.

Table 20. CMOS T5/0.8µm Process (–20% upgrade) Flash Memory Reliability Data, Package Related Tests
July 1998 to June 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F256 (B)		M28F512 (B)		M28F101 (B)		M28F102 (B)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,								
		– 168 hrs	-	-	700	0	700	0	470	0
		– 500 hrs	-	-	700	0	700	0	470	0
		– 1000 hrs	-	-	640	0	580	0	410	0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,								
		– 48 hrs	-	-	290	0	295	0	195	0
		– 96 hrs	-	-	290	0	295	0	195	0
		– 168 hrs	-	-	290	0	295	0	195	0
		– 240 hrs	-	-	290	0	215	0	170	0
Pressure Pot		121°C, 2Atm,								
		– 48 hrs	-	-	600	0	580	0	410	0
		– 96 hrs	-	-	600	0	580	0	410	0
		– 168 hrs	-	-	600	0	580	0	410	0
		– 240 hrs	-	-	600	0	580	0	410	0
Temperature Cycling	1010	–65 to 150°C,								
		– 100 cycles	-	-	640	0	550	0	470	0
		– 500 cycles	-	-	640	0	550	0	410	0
		– 1000 cycles	-	-	640	0	430	0	410	0
Thermal Shock	1011	–55 to 125°C,								
		– 100 cycles	-	-	-	-	-	-	-	-
		– 500 cycles	-	-	-	-	-	-	-	-
Solderability										
– TSOP/PLCC Packages	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	Cumulative Sample/Fail = 395/0							
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	Cumulative Sample/Fail = 80/0							

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 21A. CMOS T6/0.55µm Process Flash Memory Reliability Data, Die Related Tests
July 1998 to June 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F201 (B)		M28F210 (C) M28F211 (C) M28F220 (C)		M28F411 (C) M28F410 (C) M28F420 (C)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test (1)	1005	140°C, V_{CC} = 6V,f = 500kHz,						
		– 24 hrs	12,285	0	118,956	0	9,217	0
		– 168 hrs	-	-	470	0	-	-
		– 500 hrs	-	-	410	0	-	-
		– 1000 hrs	-	-	350	0	-	-
Retention Bake (1)	1008	150°C,						
		– 168 hrs	-	-	470	0	-	-
		– 500 hrs	-	-	410	0	-	-
		– 1000 hrs	-	-	350	0	-	-
Retention Bake	1008	250°C,						
		– 168 hrs	361	0	-	-	180	0
		– 500 hrs	361	0	-	-	180	0
		– 1000 hrs	361	0	-	-	180	0
Write/Erase Cycling		1,000 cycles	1,376	0	13,612	0	960	0
		10,000 cycles	-	-	-	-	-	-
		100,000 cycles	-	-	-	-	-	-
		200,000 cycles	-	-	-	-	-	-
Retention Bake	1008	150°C, 36 hrs	1,376	0	13,612	0	960	0

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.
1. A quarter of sample size was subjected to 10,000 Write/Erase cycles before operating life test and retention bake.

Table 21B. CMOS T6/0.55µm Process Flash Memory Reliability Data, Die Related Tests
July 1998 to June 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M29F102 M29F105		M29F002		M29F200 M29F100		M29F040 (C) M29W040		M29F400 M29W400	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test (1)	1005	140°C, V_{CC} = 6V,f = 500kHz,										
		– 24 hrs	329,027	0	90,371	0	22,220	0	79,309	0	102,287	0
		– 168 hrs	1,050	0	470	0	170	0	680	0	470	0
		– 500 hrs	1,050	0	410	0	110	0	680	0	470	0
		– 1000 hrs	990	0	350	0	110	0	620	0	410	0
Retention Bake (1)	1008	150°C,										
		– 168 hrs	990	0	470	0	170	0	505	0	470	0
		– 500 hrs	990	0	410	0	110	0	505	0	470	0
		– 1000 hrs	930	0	350	0	110	0	445	0	410	0
Retention Bake	1008	250°C,										
		– 168 hrs	120	0	126	0	51	0	617	0	162	0
		– 500 hrs	120	0	126	0	51	0	617	0	162	0
		– 1000 hrs	120	0	66	0	51	0	617	0	162	0
Write/Erase Cycling		1,000 cycles	37,773	0	10,326	0	2,336	0	9,659	0	11,861	0
		10,000 cycles	831	0	64	0	-	-	960	0	703	0
		100,000 cycles	63	0	64	0	-	-	512	0	351	0
		200,000 cycles	-	-	-	-	-	-	63	0	60	0
		1,000,000 cycles	-	-	-	-	-	-	-	-	60	0
Retention Bake	1008	150°C, 36 hrs	36,942	0	10,262	0	2,336	0	8,754	0	11,158	0

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.
1. A quarter of sample size was subjected to 10,000 Write/Erase cycles before operating life test and retention bake.

Table 22A. CMOS T6/0.55µm Process Flash Memory Reliability Data, Package Related Tests
July 1998 to June 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F201 (B)		M28F211 (C) M28F210 (C) M28F220 (C)		M28F411 (C) M28F410 (C) M28F420 (C)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,						
		– 168 hrs	-	-	470	0	-	-
		– 500 hrs	-	-	410	0	-	-
		– 1000 hrs	-	-	350	0	-	-
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,						
		– 48 hrs	-	-	195	0	-	-
		– 96 hrs	-	-	195	0	-	-
		– 168 hrs	-	-	195	0	-	-
		– 240 hrs	-	-	170	0	-	-
Pressure Pot		121°C, 2Atm,						
		– 48 hrs	-	-	350	0	-	-
		– 96 hrs	-	-	350	0	-	-
		– 168 hrs	-	-	350	0	-	-
		– 240 hrs	-	-	350	0	-	-
Temperature Cycling	1010	–65 to 150°C,						
		– 100 cycles	-	-	470	0	-	-
		– 500 cycles	-	-	410	0	-	-
		– 1000 cycles	-	-	350	0	-	-
Thermal Shock	1011	–55 to 125°C,						
		– 100 cycles	-	-	-	-	-	-
		– 500 cycles	-	-	-	-	-	-
Solderability								
– TSOP/SO Packages	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	(See cumulative data on Table 22B)					

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 22B. CMOS T6/0.55µm Process Flash Memory Reliability Data, Package Related Tests
July 1998 to June 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M29F102 M29F105		M29F002		M29F200 M29F100		M29F040 (C) M29W040		M29F400 M29W400	
			Fail	Fail	Samp.	Fail	Samp.	Samp.	Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,										
		– 168 hrs	1,050	0	470	0	170	0	680	0	470	0
		– 500 hrs	1,050	0	410	0	110	0	680	0	470	0
		– 1000 hrs	990	0	350	0	110	0	620	0	410	0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,										
		– 48 hrs	434	0	195	0	70	0	285	0	195	0
		– 96 hrs	434	0	195	0	70	0	285	0	195	0
		– 168 hrs	434	0	195	0	45	0	285	0	170	0
		– 240 hrs	409	0	170	0	45	0	255	0	170	0
Pressure Pot		121°C, 2Atm,										
		– 48 hrs	990	0	315	0	110	0	360	0	410	0
		– 96 hrs	990	0	315	0	110	0	360	0	410	0
		– 168 hrs	990	0	315	0	110	0	360	0	410	0
		– 240 hrs	990	0	315	0	110	0	360	0	410	0
Temperature Cycling	1010	–65 to 150°C,										
		– 100 cycles	930	0	470	0	110	0	680	0	470	0
		– 500 cycles	930	0	410	0	110	0	680	0	410	0
		– 1000 cycles	870	0	350	0	110	0	560	0	410	0
Thermal Shock	1011	–55 to 125°C,										
		– 100 cycles	-	-	-	-	-	-	-	-	-	-
		– 500 cycles	-	-	-	-	-	-	-	-	-	-
Solderability												
– TSOP/SO Packages	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs										
			Cumulative Sample/Fail = 545/0									

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 23. CMOS T6X/0.35µm Process Flash Memory Reliability Data
July 1998 to June 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M29W800 M29W008		M29F102	
			Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V,f = 500kHz,				
		– 24 hrs	160,781	0	2,580	0
		– 168 hrs	540	0	60	0
		– 500 hrs	420	0	-	-
		– 1000 hrs	300	0	-	-
Retention Bake	1008	150°C,				
		– 168 hrs	540	0	60	0
		– 500 hrs	420	0	-	-
		– 1000 hrs	300	0	-	-
Retention Bake	1008	250°C,				
		– 168 hrs	278	0	-	-
		– 500 hrs	278	0	-	-
		– 1000 hrs	278	0	-	-
Write/Erase Cycling		1,000 cycles	16,866	0	338	0
		10,000 cycles	428	0	50	0
		100,000 cycles	150	0	50	0
		300,000 cycles	50	0	50	0
		1,000,000 cycles	-	-	50	0
Retention Bake	1008	150°C, 36 hrs	16,411	0	288	0

Table 24. CMOS T6X/0.35µm Process Flash Memory Reliability Data, Die Related Tests
July 1998 to June 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M29W800 M29W008		M29F102	
			Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85% V_{CC} = 5V				
		– 168 hrs	540	0	60	0
		– 500 hrs	420	0	-	-
		– 1000 hrs	300	0	-	-
		– 2000 hrs	-	-	-	-
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V				
		– 48 hrs	50	0	25	0
		– 96 hrs	50	0	25	0
		– 168 hrs	50	0	-	-
		– 240 hrs	50	0	-	-
Pressure Pot		121°C, 2Atm,				
		– 48 hrs	312	0	-	-
		– 96 hrs	312	0	-	-
		– 168 hrs	312	0	-	-
		– 240 hrs	312	0	-	-
Temperature Cycling	1010	65°C to 150°C,				
		– 100 cycles	240	0	60	0
		– 500 cycles	240	0	-	-
		– 1000 cycles	240	0	-	-

Table 25. CMOS F4/1.2µm Process EEPROM Reliability Data, Die Related Tests
July 1998 to June 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST93Cxxx	
			Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V,		
		– 24 hrs	4,720	0
		– 168 hrs	720	0
		– 500 hrs	720	0
		– 1000 hrs	-	-
Retention Bake	1008	150°C,		
		– 168 hrs	450	0
		– 500 hrs	450	0
		– 1000 hrs	450	0
Write/Erase Cycling		100,000 cycles	2,216	0
		1,000,000 cycles	545	0
Retention Bake	1008	150°C, 168 hrs	-	-

Table 26. CMOS F4/1.2µm Process EEPROM Reliability Data, Package Related Tests
July 1998 to June 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST93Cxxx	
			Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs	 560 560 560	 0 0 0
Pressure Pot		121°C, 2Atm, – 48 hrs – 96 hrs – 168 hrs – 240 hrs	 1,800 1,800 1,800 900	 0 0 0 0
Temperature Cycling	1010	–65 to 150°C, – 100 cycles – 200 cycles –40 to 150°C, – 500 cycles – 1000 cycles	 1,800 900 - -	 0 0 - -
Soderability – PDIP Package – SO Package	 2003 CECC 90,000	 245°C, 5sec, Precondition Steam, 8hrs 215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	 (See cumulative data on Table 30B) (See cumulative data on Table 30B)	
Resistance to Surface Mount: – SO Package			 (See cumulative data on Table 30B)	

Table 27A. CMOS F4S/1.0µm Process EEPROM Reliability Data, Die Related Tests
July 1998 to June 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST24C01 ST24W01		ST24C02 ST24W02		ST24C04 ST24W04		ST24C08		ST24C16 ST25C16		ST24LC21	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V,												
		– 24 hrs	480	0	3,280	0	3,760	0	-	-	1,440	0	-	-
		– 168 hrs	80	0	480	0	560	0	-	-	240	0	-	-
		– 500 hrs	80	0	480	0	560	0	-	-	240	0	-	-
		– 1000 hrs	-	-	-	-	-	-	-	-	-	-	-	-
Retention Bake	1008	150°C,												
		– 168 hrs	50	0	300	0	350	0	-	-	330	0	-	-
		– 500 hrs	50	0	300	0	350	0	-	-	330	0	-	-
		– 1000 hrs	50	0	300	0	350	0	-	-	330	0	-	-
Write/Erase Cycling		100,000 cycles	1,636	0	5,362	2 (a)	7,266	3 (a)	2,317	1 (a)	8,028	7 (a)	1,665	1 (a)
		1,000,000 cycles	-	-	1980	0	2,881	3 (a)	1,067	1 (a)	1,140	0	675	0
Retention Bake	1008	150°C, 168 hrs	-	-	-	-	-	-	-	-	-	-	-	-

Note: a. Single bit fail.
Oxide quality improvements are addressed in two directions:
– Continuous quality improvement by fab task force.
– “Build in” robustness through product and process design.

Table 27B. CMOS F4S/1.0µm Process EEPROM Reliability Data, Die Related Tests
July 1998 to June 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M93C06		M93C46		M93C56		M93C66		M28C16		M28C64D M28C64	
			Samp	Fail	Samp	Fail	Samp	Fail	Samp	Fail	Samp	Fail	Samp	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V,												
		– 24 hrs	-	-	1,960	0	480	0	480	0	240	0	2,290	0
		– 168 hrs	-	-	320	0	80	0	80	0	240	0	2,290	0
		– 500 hrs	-	-	320	0	80	0	80	0	240	0	1,600	0
		– 1000 hrs	-	-	-	-	-	-	-	-	80	0	610	0
Retention Bake	1008	150°C,												
		– 168 hrs	-	-	200	0	50	0	50	0	-	-	50	0
		– 500 hrs	-	-	200	0	50	0	50	0	-	-	50	0
		– 1000 hrs	-	-	200	0	50	0	50	0	-	-	50	0
Write/Erase Cycling		100,000 cycles	-	-	722	0	1,577	2 (a)	1,396	0	-	-	-	-
		1,000,000 cycles	-	-	-	-	473	0	473	0	-	-	-	-
Retention Bake	1008	150°C, 168 hrs	-	-	-	-	-	-	-	-	-	-	-	-

Note: a. Single bit fail.
Oxide quality improvements are addressed in two directions:
– Continuous quality improvement by fab task force.
– “Build in” robustness through product and process design.

Table 28A. CMOS F4S/1.0µm Process EEPROM Reliability Data, Package Related Tests
July 1998 to June 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST24C01 ST24W01		ST24C02 ST24W02		ST24C04 ST24W04		ST24C08	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,								
		– 168 hrs	160	0	160	0	200	0	160	0
		– 500 hrs	160	0	160	0	200	0	160	0
		– 1000 hrs	160	0	160	0	200	0	160	0
Pressure Pot		121°C, 2Atm,								
		– 48 hrs	400	0	700	0	500	0	400	0
		– 96 hrs	400	0	700	0	500	0	400	0
		– 168 hrs	400	0	700	0	500	0	400	0
		– 240 hrs	200	0	350	0	250	0	200	0
Temperature Cycling	1010	–65 to 150°C,								
		– 100 cycles	400	0	700	0	500	0	400	0
		– 200 cycles	200	0	350	0	250	0	200	0
		–40 to 150°C,								
		– 500 cycles	-	-	-	-	-	-	-	-
		– 1000 cycles	-	-	-	-	-	-	-	-
Solderability										
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	(See cumulative data on Table 30B)							
– SO Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	(See cumulative data on Table 30B)							
Resistance to Surface Mount:										
– SO Package			(See cumulative data on Table 30B)							

Table 28B. CMOS F4S/1.0µm Process EEPROM Reliability Data, Package Related Tests
July 1998 to June 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST24C16 ST25C16		M93C46	
			Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,				
		– 168 hrs	299	0	80	0
		– 500 hrs	299	0	80	0
		– 1000 hrs	299	0	80	0
Pressure Pot		121°C, 2Atm,				
		– 48 hrs	880	0	550	0
		– 96 hrs	880	0	550	0
		– 168 hrs	880	0	550	0
		– 240 hrs	530	0	100	0
Temperature Cycling	1010	–65 to 150°C,				
		– 100 cycles	530	0	500	0
		– 200 cycles	530	0	100	0
		– 500 cycles	180	0	-	-
		– 1000 cycles	180	0	-	-
		–40 to 150°C,				
		– 500 cycles	-	-	-	-
		– 1000 cycles	-	-	-	-
Solderability						
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	(See cumulative data on Table 30B)			
– SO Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	(See cumulative data on Table 30B)			
Resistance to Surface Mount:						
– SO Package			(See cumulative data on Table 30B)			

Table 28C. CMOS F4S/1.0µm Process EEPROM Reliability Data, Package Related Tests
July 1998 to June 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M93C56		M93C66		M28C16F		M28C64 M28C64D	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,								
		– 168 hrs	40	0	40	0	150	0	510	0
		– 500 hrs	40	0	40	0	150	0	510	0
		– 1000 hrs	40	0	40	0	50	0	460	0
Pressure Pot		121°C, 2Atm,								
		– 48 hrs	100	0	100	0	150	0	1,030	0
		– 96 hrs	100	0	100	0	150	0	1,030	0
		– 168 hrs	100	0	100	0	150	0	1,030	0
		– 240 hrs	50	0	50	0	50	0	1,030	0
Temperature Cycling	1010	–65 to 150°C,								
		– 100 cycles	100	0	100	0	100	0	630	0
		– 200 cycles	50	0	50	0	100	0	630	0
		– 500 cycles	-	-	-	-	100	0	450	0
		–1000 cycles	-	-	-	-	100	0	400	0
		–40 to 150°C,								
		– 500 cycles	-	-	-	-	-	-	-	-
		– 1000 cycles	-	-	-	-	-	-	-	-
Solderability										
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	(See cumulative data on Table 30B)							
– SO Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	(See cumulative data on Table 30B)							
– PLCC Package			(See cumulative data on Table 30B)							
– TSOP Package			(See cumulative data on Table 30B)							
Resistance to Surface Mount:										
– SO Package			(See cumulative data on Table 30B)							
– TSOP Package			(See cumulative data on Table 30B)							
– PLCC Package			(See cumulative data on Table 30B)							

Table 29A. CMOS F6 0,6µm Process EEPROM Reliability Data, Die Related Tests
July 1998 to June 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M24C01		M24C02		M24C04		M24C08	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V,								
		– 24 hrs	2,400	0	2,040	0	4,240	0	2,400	0
		– 168 hrs	400	0	400	0	640	0	400	0
		– 500 hrs	400	0	400	0	640	0	400	0
		– 1000 hrs	-	-	-	-	-	-	-	-
Retention Bake	1008	150°C,								
		– 168 hrs	250	0	250	0	400	0	250	0
		– 500 hrs	250	0	250	0	400	0	250	0
		– 1000 hrs	250	0	250	0	400	0	250	0
Write/Erase Cycling		100,000 cycles	7,679	0	11,273	2 (a)	9,657	2 (a)	12,271	6 (a)
		1,000,000 cycles	2,303	0	2,303	0	2,303	0	2,100	0
Retention Bake	1008	150°C, 168 hrs	-	-	-	-	-	-	-	-

Note: a. Single bit fail.
Oxide quality improvements are addressed in two directions:
– Continuous quality improvement by fab task force.
– “Build in” robustness through product and process design.

Table 29B. CMOS F6 0,6µm Process EEPROM Reliability Data, Die Related Tests
July 1998 to June 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M24C16 M25C16		M24C32		M24C64		M28C64	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V,								
		– 24 hrs	3,360	0	3,280	0	1,440	0	2,370	0
		– 168 hrs	560	0	480	0	240	0	2,370	0
		– 500 hrs	560	0	480	0	240	0	2,370	0
		– 1000 hrs	-	-	-	-	-	-	1,030	0
Retention Bake	1008	150°C,								
		– 168 hrs	480	0	300	0	150	0	-	-
		– 500 hrs	480	0	300	0	150	0	-	-
		– 1000 hrs	480	0	300	0	150	0	-	-
Write/Erase Cycling		100,000 cycles	8,192	4 (a)	15,479	17 (a)	6,390	4 (a)	-	-
		1,000,000 cycles	2,100	1 (a)	2,828	0	-	-	-	-
Retention Bake	1008	150°C, 168 hrs	-	-	-	-	-	-	-	-

Note: a. Single bit fail.
Oxide quality improvements are addressed in two directions:
– Continuous quality improvement by fab task force.
– “Build in” robustness through product and process design.

Table 30A. CMOS F6 0,6µm Process EEPROM Reliability Data, Package Related Tests
July 1998 to June 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M24C01		M24C02		M24C04		M24C08	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,								
		– 168 hrs	80	0	200	0	120	0	320	0
		– 500 hrs	80	0	200	0	120	0	320	0
		– 1000 hrs	80	0	200	0	120	0	320	0
Pressure Pot		121°C, 2Atm,								
		– 48 hrs	650	0	1,550	0	1,200	0	1,450	0
		– 96 hrs	650	0	1,550	0	1,200	0	1,450	0
		– 168 hrs	650	0	1,550	0	1,200	0	1,450	0
		– 240 hrs	150	0	500	0	250	0	400	0
Temperature Cycling	1010	–65 to 150°C,								
		– 100 cycles	750	0	1,600	0	1,200	0	1,300	0
		– 200 cycles	150	0	500	0	250	0	400	0
		–40 to 150°C,								
		– 500 cycles	-	-	-	-	-	-	-	-
		– 1000 cycles	-	-	-	-	-	-	-	-
Soderability										
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	(See cumulative data on Table 30B)							
– SO Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	(See cumulative data on Table 30B)							
Resistance to Surface Mount:										
– SO Package			(See cumulative data on Table 30B)							

Table 30B. CMOS F6 0,6µm Process EEPROM Reliability Data, Package Related Tests
July 1998 to June 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M24C16 M25C16		M24C32		M24C64		M28C64	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,								
		– 168 hrs	337	0	120	0	-	-	890	0
		– 500 hrs	337	0	120	0	-	-	890	0
		– 1000 hrs	337	0	120	0	-	-	890	0
Pressure Pot		121°C, 2Atm,								
		– 48 hrs	960	0	300	0	400	0	1,090	0
		– 96 hrs	960	0	300	0	400	0	1,090	0
		– 168 hrs	960	0	300	0	400	0	1,090	0
		– 240 hrs	430	0	150	0	200	0	690	0
Temperature Cycling	1010	–65 to 150°C,								
		– 100 cycles	1,190	0	300	0	400	0	950	0
		– 200 cycles	410	0	150	0	200	0	950	0
		– 500 cycles	410	0	-	-	-	-	950	0
		– 1000 cycles	180	0	-	-	-	-	450	0
		–40 to 150°C,								
		– 500 cycles	-	-	-	-	-	-	-	-
		– 1000 cycles	-	-	-	-	-	-	-	-
Solderability										
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	Cumulative Sample/Fail = 25/0							
– SO Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	Cumulative Sample/Fail = 216/0							
– PLCC Package			Cumulative Sample/Fail = 25/0							
– TSOP Package			Cumulative Sample/Fail = 25/0							
Resistance to Surface Mount:										
– PDIP Package			Cumulative Sample/Fail = 40/0							
– SO Package			Cumulative Sample/Fail = 17,560/0							
– TSOP Package			Cumulative Sample/Fail = 2,360/0							
– PLCC Package			Cumulative Sample/Fail = 1,460/0							

Table 31. HCMOS S3/1.2µm Process ZEROPOWER NVRAM Reliability Data, Die Related Tests
July 1998 to June 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M48T08 M48T18	
			Samp.	Fail
Operating Life Test	1005	125°C, V_{CC} = 7V, f = 1MHz, – 168 hrs – 500 hrs – 1000 hrs	 1,778 1,415 1,405	 0 0 0

Table 32. HCMOS S3/1.2µm Process ZEROPOWER NVRAM Reliability Data, Package Related Tests
July 1998 to June 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M48T08 M48T18	
			Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs	 847 845 691	 0 0 0
Temperature Cycling Caphat	1010	–40 to 100°C, – 100 cycles – 500 cycles – 1000 cycles	 880 80 80	 0 0 0

Table 33. HCMOS 4DZ/0.8µm Process ZEROPOWER NVRAM Reliability Data, Die Related Tests
July 1998 to June 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M48T58 M48T58Y M48T559Y	
			Samp.	Fail
Operating Life Test	1005	125°C, V_{CC} = 6V, f = 1MHz, – 168 hrs – 500 hrs – 1000 hrs	 716 537 527	 0 0 0

Table 34. HCMOS 4DZ/0.8µm Process ZEROPOWER NVRAM Reliability Data, Package Related Tests
July 1998 to June 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M48T58 M48T58Y M48T559Y	
			Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs	 308 231 231	 0 0 0
Hast	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V, – 96 hrs – 168 hrs – 240 hrs	 - - -	 - - -
Temperature Cycling	1010	–65 to 150°C, – 100 cycles – 500 cycles – 1000 cycles	 400 240 160	 0 0 0

Table 35. HCMOS 4DZ/0.7µm Process ZEROPOWER HYBRID MODULE Reliability Data, Die Related Tests
July 1998 to June 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M48T37Y (5V)	
			Samp.	Fail
Operating Life Test	1005	125°C, V_{CC} = 6V, f = 1MHz, – 168 hrs – 500 hrs – 1000 hrs	 442 346 252	 1 (a) 0 0

Note: a. Single bit Failure

Table 36. HCMOS 4DZ/0.7µm Process ZEROPOWER HYBRID MODULE Reliability Data, Package Related Tests
July 1998 to June 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M48T37Y (5V)	
			Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs	 80 76 36	 0 0 0
	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V, – 96 hrs – 168 hrs – 240 hrs	 - - -	 - - -
Temperature Cycling	1010	–40 to 100°C, – 100 cycles – 500 cycles – 1000 cycles	 200 159 119	 0 0 0

Table 37. HCMOS 4PZ/0.6µm PROCESS ZEROPOWER SRAM Reliability Data, Die Related Tests
July 1998 to June 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M48Z35	
			Samp.	Fail
Operating Life Test	1005	125°C, V_{CC} = 6V, f = 1MHz, – 168 hrs – 500 hrs – 1000 hrs	 1,800 598 598	 1 (a) 0 0

Note: a. A particle-induced gate-oxide breakdown in an n-channel gate of the control decode circuitry causing elevated current.

Table 38. HCMOS 4PZ/0.6µm PROCESS ZEROPOWER SRAM Reliability Data, Package Related Tests
July 1998 to June 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M48Z35	
			Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs	 - - -	 - - -
Hast	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V, – 96 hrs – 168 hrs – 240 hrs	 66 66 -	 0 0 -
Temperature Cycling	1010	–40 to 100°C, – 100 cycles – 500 cycles – 1000 cycles	 99 99 99	 0 0 0

Table 39. ZEROPOWER HYBRID MODULE Reliability Data, Die Related Tests
July 1998 to June 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M48Z128 M48Z30	
			Samp.	Fail
Operating Life Test	1005	125°C, V_{CC} = 6V, f = 1MHz, – 168 hrs – 500 hrs – 1000 hrs	 315 269 220	 0 0 0

Table 40. ZEROPOWER HYBRID MODULE Reliability Data, Package Related Tests
July 1998 to June 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M48Z128 M48Z30	
			Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs	 147 124 99	 0 0 0
Hast	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V, – 96 hrs – 168 hrs – 240 hrs	 - - -	 - - -
Temperature Cycling	1010	–40 to 100°C, – 100 cycles – 500 cycles – 1000 cycles	 314 221 134	 0 0 0

Table 41. Statistical Process Control: CMOS E5/0.6µm Process (–35% upgrade) UV EPROM and OTP EPROM, Agrate - Italy F8 Diffusion Line

Key Process Parameters	3Q98	4Q98	1Q99	2Q99
	CPK	CPK	CPK	CPK
Pad Oxide Thickness	(*)	(*)	2.12	2.20
Silicon Nitride Thickness	(*)	(*)	1.9	2.13
Field Oxide Thickness	(*)	(*)	2.13	1.98
Gate Oxide Thickness	(*)	(*)	1.62	1.72
Interpoly Oxide Thickness	(*)	(*)	1.76	2.00
Intermediate Dielectric Thickness	(*)	(*)	1.73	1.74
Polysilicon 1 Thickness	(*)	(*)	2.54	2.41
Active Area Critical Dimensions	(*)	(*)	2.58	1.42
Policide Critical Dimensions	(*)	(*)	2.13	1.68

Key Electrical Parameters	3Q98	4Q98	1Q99	2Q99
	CPK	CPK	CPK	CPK
VT N-Channel Square Tr.	(*)	(*)	2.31	1.40
VT P-Channel Square Tr.	(*)	(*)	2.22	1.40
VT Natural Square Tr.	(*)	(*)	2.88	3.86
VT Memory Cell	(*)	(*)	1.8	2.26
I_{DON} N-Channel	(*)	(*)	2.79	2.30
N+ Active Area Contact Chain	(*)	(*)	8.1	8.71
AL-W Silicide Contact Chain Resistance	(*)	(*)	2.46	4.32

Note: (*) No production data during 3Q98, 4Q98.

Table 42. Statistical Process Control: CMOS E6DM/0.5µm Process (–15% upgrade) UV EPROM and OTP EPROM, Catania - Italy M5 Diffusion Line

Key Process Parameters	3Q98	4Q98	1Q99	2Q99
	CPK	CPK	CPK	CPK
Pad Oxide Thickness	(*)	(*)	2.06	3.05
Silicon Nitride Thickness	(*)	(*)	1.81	1.49
Field Oxide Thickness	(*)	(*)	1.62	1.60
Gate Oxide Thickness	(*)	(*)	2.3	1.81
Interpoly Oxide Thickness	(*)	(*)	2.04	2.5
Intermediate Dielectric Thickness	(*)	(*)	1.89	1.92
Polysilicon 1 Thickness	(*)	(*)	1.63	1.33
Active Area Critical Dimensions	(*)	(*)	1.36	1.61
Policide Critical Dimensions	(*)	(*)	1.84	1.33

Key Electrical Parameters	3Q98	4Q98	1Q99	2Q99
	CPK	CPK	CPK	CPK
VT N-Channel Square Tr.	(*)	(*)	2.11	1.42
VT P-Channel Square Tr.	(*)	(*)	1.71	2.01
VT Natural Square Tr.	(*)	(*)	3.06	3.60
VT Memory Cell	(*)	(*)	1.56	1.37
I_{DON} N-Channel	(*)	(*)	5.01	3.46
N+ Active Area Contact Chain	(*)	(*)	10.7	5.60
AL-W Silicide Contact Chain Resistance	(*)	(*)	4.68	4.83

Note: (*) No production data during 3Q98, 4Q98.

Table 43. Statistical Process Control: CMOS E6/0.6µm Process (–10% upgrade) UV EPROM and OTP EPROM, Agrate - Italy F8 Diffusion Line

Key Process Parameters	3Q98	4Q98	1Q99	2Q99
	CPK	CPK	CPK	CPK
Pad Oxide Thickness	2.22	2.17	2.12	2.23
Silicon Nitride Thickness	1.94	1.59	1.57	1.38
Field Oxide Thickness	3.12	3.70	3.66	4.75
Gate Oxide Thickness	1.72	1.99	1.62	1.72
Interpoly Oxide Thickness	2.37	2.03	1.76	2.00
Intermediate Dielectric Thickness	1.62	1.59	1.73	1.72
Polysilicon 1 Thickness	1.97	2.46	2.54	2.39
Active Area Critical Dimensions	2.26	3.68	2.63	1.56
Policide Critical Dimensions	2.03	1.59	1.74	1.58

Key Electrical Parameters	3Q98	4Q98	1Q99	2Q99
	CPK	CPK	CPK	CPK
VT N-Channel 10 x 10µm	4.35	3.89	2.20	3.38
VT P-Channel 10 x 10µm	2.08	3.27	2.47	2.45
VT Natural 10 x 10µm	2.31	1.93	2.53	2.58
VT Memory Cell 0.65 x 0.65µm	1.51	1.56	1.55	1.63
I_{DON} N-Channel 10 x 10µm	3.15	2.04	2.91	2.74
N+ Active Area Contact Chain	2.87	4.01	4.89	4.92
AL-W Silicide Contact Chain Resistance	2.05	1.87	3.32	4.16

Table 44. Statistical Process Control: CMOS E6/0.6µm Process (–10% upgrade) UV EPROM and OTP EPROM, Catania - Italy M5 Diffusion Line

Key Process Parameters	3Q98	4Q98	1Q99	2Q99
	CPK	CPK	CPK	CPK
Pad Oxide Thickness	1.55	1.62	1.51	1.52
Silicon Nitride Thickness	1.38	1.42	1.38	1.49
Field Oxide Thickness	2.87	2.59	1.64	1.60
Gate Oxide Thickness	2.08	1.81	2.3	1.81
Interpoly Oxide Thickness	1.48	1.57	1.73	1.60
N-Well Oxidation	3.53	3.74	3.24	4.23
Polysilicon 1 Thickness	1.68	1.51	1.81	1.97
Active Area Critical Dimensions	2.98	2.95	1.36	3.16
Policide Critical Dimensions	1.95	1.94	1.84	2.17

Key Electrical Parameters	3Q98	4Q98	1Q99	2Q99
	CPK	CPK	CPK	CPK
VT N-Channel Square Tr.	1.73	2.91	5.06	3.67
VT P-Channel Square Tr.	2.72	3.10	2.49	3.04
VT Natural Square Tr.	1.52	2.08	2.62	2.48
VT Memory Cell	1.44	1.34	1.42	1.59
I_{DON} N-Channel	2.62	2.60	3.16	3.48
N+ Active Area Contact Chain	6.01	6.20	7.87	5.70
AL-W Silicide Contact Chain Resistance	1.72	2.97	2.3	2.70

Table 45. Statistical Process Control: CMOS E6/0.35µm Process (–30% upgrade) UV EPROM and OTP EPROM, Catania - Italy M5 Diffusion Line

Key Process Parameters	3Q98	4Q98	1Q99	2Q99
	CPK	CPK	CPK	CPK
Pad Oxide Thickness	-	-	-	1.76
Silicon Nitride Thickness	-	-	-	2.33
Field Oxide Thickness	-	-	-	1.61
Gate Oxide Thickness	-	-	-	1.97
Interpoly Oxide Thickness	-	-	-	1.6
N-Well Oxidation	-	-	-	4.2
Polysilicon 1 Thickness	-	-	-	1.76
Active Area Critical Dimensions	-	-	-	1.34
Policide Critical Dimensions				2.27

Key Electrical Parameters	3Q98	4Q98	1Q99	2Q99
	-	CPK	CPK	CPK
VT N-Channel Square Tr.	-	-	-	2.58
VT P-Channel Square Tr.	-	-	-	3.10
VT Natural Square Tr.	-	-	-	8.10
VT Memory Cell	-	-	-	0.8 (1)
I_{DON} N-Channel	-	-	-	6.74
N+ Active Area Contact Chain	-	-	-	9.93
AL-W Silicide Contact Chain Resistance		-	-	3.7

Note: 1. Fine tuning of the target.

Table 46. Statistical Process Control: CMOS T5/0.8µm Process (–20% upgrade) Flash Memory, Agrate - Italy F8 Diffusion Line

Key Process Parameters	3Q98	4Q98	1Q99	2Q99
	CPK	CPK	CPK	CPK
Field Oxide Thickness	2.23	2.83	2.61	2.59
Polysilicon 1 Thickness	2.81	4.37	2.75	2.52
Gate Oxide Thickness	1.88	2.01	1.93	1.73
Tunnel Oxide Thickness	2.65	2.60	2.70	2.41
ONO Bottom Oxide Thickness	1.80	2.12	2.52	2.08
ONO Nitride Thickness	1.67	2.19	1.34	1.76
ONO Top Oxide Thickness	2.21	2.58	2.12	3.36
Active Area Critical Dimensions	2.26	1.67	1.80	1.65
Polysilicon 2 Critical Dimensions	2.49	1.82	1.55	2.48

Key Electrical Parameters	3Q98	4Q98	1Q99	2Q99
	CPK	CPK	CPK	CPK
VT N-Channel 25 x 25 µm	1.55	2.19	2.27	1.78
VT P-Channel 25 x 25 µm	1.80	2.33	2.46	2.81
BV N-Channel 25 x 0.8 µm	1.60	1.37	1.86	1.74
BV P-Channel 25 x 0.9 µm	4.10	3.66	3.55	3.57
VT Memory Cell 0.8 x 0.8 µm	2.24	1.59	3.02	2.50
I_{DON} N-Channel 25 x 0.8 µm	2.63	2.56	1.49	1.68
Al+N+ Contact Chain	4.18	4.53	4.55	4.49
AL-W Silicide Contact Chain Resistance	3.81	3.05	2.28	5.94

Table 47A. Statistical Process Control: CMOS T6/0.55µm Process Flash Memory, Agrate - Italy R1 Diffusion Line

Key Process Parameters	3Q98	4Q98	1Q99	2Q99
	CPK	CPK	CPK	CPK
Field Oxide Thickness	2.07	2.23	1.95	(*)
First Poly Thickness	2.05	1.97	2.61	(*)
Gate Oxide HV Thickness	3.05	2.94	2.58	(*)
Tunnel Oxide Thickness	2.17	1.66	2.01	(*)
Gate Oxide LV Thickness	2.22	1.83	2.24	(*)
ONO Bottom Oxide Thickness	1.81	1.34	1.37	(*)
ONO Nitride Thickness	1.89	2.15	2.27	(*)
ONO Top Oxide Thickness	1.96	1.83	2.09	(*)
Active Area CD	1.15 (1)	1.39	1.39	(*)
Second Poly CD	1.22 (2)	1.05 (3)	2.29	(*)

Note: 1. New resist and new equipment under evaluation.
2. Change in exposure energy according to new target.
3. Fine tuning ongoing to align different production island.
(*) No data due to low production during 2Q99

Table 47B. Statistical Process Control: CMOS T6/0.55µm Process Flash Memory, Agrate - Italy R1 Diffusion Line

Key Electrical Parameters	3Q98	4Q98	1Q99	2Q99
	CPK	CPK	CPK	CPK
LV-NCh LVS (10 x 0.8) Saturation Current	4.46	4.79	4.55	(*)
LV-PCh LVS (10 x 0.9) BV	5.4	3.39	2.17	(*)
LV-PCh LVS (10 x 0.9) Saturation Current	2.32	3.90	4.52	(*)
LV-PCh SQ. VTh	1.79	2.23	1.51	(*)
HV-NCh SQ. VTh	1.82	2.09	1.97	(*)
HV-NCh (10 x 1.2) LVS Saturation Current	12.2	14.4	10.2	(*)
HV-PCh (10 x 1.3) BV	3.14	3.31	3.65	(*)
HV-PCh (10 x 1.3) Saturation Current	4.96	5.32	5.00	(*)
HV-PCh SQ. VTh	1.46	1.47	1.35	(*)
UV Erased Cell VTh	1.40	1.49	2.12	(*)
N+ Contact Chain	6.33	7.73	8.73	(*)
Silicide Contact Chain	3.11	3.65	2.97	(*)
LV-NCh (10 x 0.8) BV	4.34	4.92	8.53	(*)

Note: (*) No data due to low production during 2Q99

Table 48A. Statistical Process Control: CMOS T6/0.55µm Process Flash Memory, Catania - Italy M5 Diffusion Line

Key Electrical Parameters	3Q98	4Q98	1Q99	2Q99
	CPK	CPK	CPK	CPK
Field Oxide Thickness	2.82	2.28	2.5	2.12
First Poly Thickness	1.45	1.39	1.43	1.53
Gate Oxide HV Thickness	1.61	1.48	1.35	1.41
Tunnel Oxide Thickness	1.51	1.75	1.6	2.06
Gate Oxide LV Thickness	1.66	1.45	1.56	1.78
ONO Bottom Oxide Thickness	1.44	1.33	1.33	1.34
ONO Nitride Thickness	1.52	1.34	1.34	1.69
ONO Top Oxide Thickness	1.83	2.35	2.07	2.64
Active Area CD	2.65	1.88	1.98	2.13
Second Poly CD	2.25	1.41	1.61	1.36

Table 48B. Statistical Process Control: CMOS T6/0.55µm Process Flash Memory, Catania - Italy M5 Diffusion Line

Key Electrical Parameters	3Q98	4Q98	1Q99	2Q99
	CPK	CPK	CPK	CPK
LV-NCh LVS (10 x 0.8) Saturation Current	1.70	2.91	3.12	3.21
LV-PCh LVS (10 x 0.9) BV	2.29	2.41	2.98	3.28
LV-PCh LVS (10 x 0.9) Saturation Current	1.37	1.87	1.74	1.35
LV-PCh SQ. VTh	1.58	1.97	2.00	1.59
HV-NCh (10 x 1.2) LVS BV	1.99	1.6	2.24	1.68
HV-NCh SQ. VTh	1.53	1.63	1.77	1.63
HV-NCh (10 x 1.2) LVS Saturation Current	3.3	2.8	3.13	2.90
HV-PCh (10 x 1.3) BV	2.44	2.73	3.56	2.53
HV-PCh (10 x 1.3) Saturation Current	2.6	2.3	3.71	3.70
HV-PCh SQ. VTh	1.39	1.36	1.81	1.33
UV Erased Cell VTh	1.88	1.82	1.73	1.51
N+ Contact Chain	3.28	4.51	5.63	4.00
Silicide Contact Chain	1.35	2.55	2.36	1.39
LV-NCh (10 x 0.8) BV	2.08	3.69	3.35	2.02

Table 49A. Statistical Process Control: CMOS T6XU35/0.35µm Process Flash Memory, Agrate - Italy R1 Diffusion Line

Key Process Parameters	3Q98	4Q98	1Q99	2Q99
	CPK	CPK	CPK	CPK
Field Oxide Thickness	-	3.16	3.40	5.20
First Poly Thickness Gate	-	1.33	1.93	2.51
Gate Oxide HV Thickness	-	2.44	2.10	2.82
Tunnel Oxide Thickness	-	2.22	1.83	2.43
Gate Oxide LV Thickness	-	2.09	2.31	2.78
ONO Nitride Thickness	-	1.03 (1)	1.73	1.68
ONO Top Oxide Thickness	-	1.01 (1)	1.34	1.53
Active Area CD	-	1.33	1.77	1.33
Second Poly CD	-	1.37	2.03	2.26

Note: 1. Process optimization to improve thickness uniformity.

Table 49B. Statistical Process Control: CMOS T6XU35/0.35µm Process Flash Memory, Agrate - Italy R1 Diffusion Line

Key Electrical Parameters	3Q98	4Q98	1Q99	2Q99
	CPK	CPK	CPK	CPK
LV-NCh LVS Saturation Current	-	1.88	2.13	2.45
LV-PCh LVS BV	-	1.65	2.61	2.46
LV-PCh LVS Saturation Current	-	1.44	4.92	4.12
LV-PCh SQ. VTh	-	1.63	3.15	3.12
HV-NCh SQ. VTh	-	2.56	2.17	1.90
HV-NCh LVS Saturation Current	-	2.21	3.39	3.22
HV-PCh BV	-	4.55	4.19	3.15
HV-PCh Saturation Current	-	3.82	5.05	4.96
HV-NCh LVS BV	-	3.51	6.73	5.57
LV-NCh LVS BV	-	3.20	6.69	3.95
LV-NCh SQ. VTh	-	4.41	3.65	2.57
HV-PCh SQ. VTh	-	1.39	2.13	1.72
Word Line Resistant	-	1.48	1.55	1.45
UV Erased Cell VTh	-	0.65 (1)	1.98	3.70
N+ Contact Chain	-	1.69	4.11	1.70

Note: 1. Test structure problem suspected. Further investigation in progress.

Table 50A. Statistical Process Control: CMOS T6XU35/0.35µm Process Flash Memory, Catania - Italy M5 Diffusion Line

Key Process Parameters	3Q98	4Q98	1Q99	2Q99
	CPK	CPK	CPK	CPK
Field Oxide Thickness	(*)	(*)	1.42	1.70
First Poly Thickness Gate	(*)	(*)	1.67	1.52
Gate Oxide HV Thickness	(*)	(*)	1.84	1.34
Tunnel Oxide Thickness	(*)	(*)	1.36	2.28
Gate Oxide LV Thickness	(*)	(*)	1.40	2.18
ONO Nitride Thickness	(*)	(*)	2.97	2.33
ONO Top Oxide Thickness	(*)	(*)	1.67	1.36
Active Area CD	(*)	(*)	0.98 (1)	1.33
Second Poly CD	(*)	(*)	1.33	0.83 (1)

Note: (*).No production data.New process.
1. Fine tuning of measurement equipment software in progress.

Table 50B. Statistical Process Control: CMOS T6XU35/0.35µm Process Flash Memory, Catania - Italy M5 Diffusion Line

Key Electrical Parameters	3Q98	4Q98	1Q99	2Q99
	CPK	CPK	CPK	CPK
LV-NCh LVS Saturation Current	-	-	2.14	2.20
LV-PCh LVS BV	-	-	1.36	1.33
LV-PCh LVS Saturation Current	-	-	1.72	1.58
LV-PCh SQ. VTh	-	-	2.81	3.65
HV-NCh SQ. VTh	-	-	3.34	3.40
HV-NCh LVS Saturation Current	-	-	2.15	2.01
HV-PCh BV	-	-	3.97	3.86
HV-PCh Saturation Current	-	-	3.26	3.10
HV-NCh LVS BV	-	-	3.11	3.74
LV-NCh LVS BV	-	-	2.14	2.84
LV-NCh SQ. VTh	-	-	2.14	2.84
HV-PCh SQ. VTh	-	-	2.57	2.05
Word Line Resistant	-	-	1.33	1.35
UV Erased Cell VTh	-	-	1.55	3.93
N+ Contact Chain	-	-	1.72	1.65

Table 51. Statistical Process Control: CMOS F6 0.6µm Process EEPROM Memory, Agrate - Italy F8 Diffusion Line

Key Process Parameters	3Q98	4Q98	1Q99	2Q99
	CPK	CPK	CPK	CPK
Pad Oxide Thickness	2.22	2.17	2.12	2.12
Silicon Nitride Thickness	1.90	1.86	1.58	1.58
Field Oxide Thickness	2.23	2.83	2.61	2.61
Gate Oxide 1 Thickness	1.86	2.23	2.08	2.08
Gate Oxide 2 Thickness	2.34	1.81	2.35	2.35
Tunnel Oxide Thickness	2.50	2.62	2.73	2.73
Dialectric Thickness	1.73	2.20	1.99	1.99
Active Area Critical Dimensions	1.70	1.81	1.53	1.53
Policide Critical Dimensions	2.08	1.89	1.89	1.89
Poly Front Deposition Thickness	1.87	2.21	1.98	1.98
Contacts Critical Dimension	1.59	1.65	1.79	1.79

Key Electrical Parameters	3Q98	4Q98	1Q99	2Q99
	CPK	CPK	CPK	CPK
VT N-Channel 10 x 10µm	1.99	2.26	2.20	2.20
VT P-Channel 10 x 10µm	2.48	2.31	2.55	2.55
VT Natural 10 x 10µm	1.79	3.56	2.37	2.37
BV N-Channel 10 x 10µm	2.77	2.26	2.51	2.51
BV P-Channel 10 x 10µm	2.14	1.42	1.57	1.57
EBD-LVN	5.43	4.67	3.38	3.38
N+ Active Area Contact Chain	2.89	3.46	3.86	3.86
EBD-TUN	1.87	2.92	1.86	1.86

Table 52A. Statistical Process Control: CMOS M4S40-F-DLM/0.7µm Process Smartcard Product, Rousset - France Diffusion Line

Key Process Parameters	3Q98	4Q98	1Q99	2Q99
	CPK	CPK	CPK	CPK
Field Oxide Thickness	-	-	3.13	4.27
Gate Oxide Thickness	-	-	1.64	1.79
Tunnel Oxide Thickness	-	-	1.83	1.67
Polysilicium	-	-	1.67	3.56
Poly for Logic	-	-	3.13	3.41
Vapox	-	-	2.34	3.49
TEOS IMD1	-	-	2.34	2.37
USG IMD1	-	-	3.02	3.09

Table 52B. Statistical Process Control: CMOS M4S40-F-DLM/0.7µm Process Smartcard Product, Rousset - France Diffusion Line

Key Electrical Parameters	3Q98	4Q98	1Q99	2Q99
	CPK	CPK	CPK	CPK
Resist N+	-	-	2.93	1.55
Resist P+	-	-	3.3	2.22
Contact AL/N+	-	-	4.19	3.04
Contact AL/P+	-	-	3.2	3.04
Contact AL/POLY	-	-	13.08	4.38
VT En (25x25)	-	-	2.7	2.12
VT Ep (25x25)	-	-	1.68	1.54
VT Mc Erase	-	-	2.41	1.48
VT Mc Write	-	-	4.27	3.13
BV Diode N+/P-	-	-	4.08	3.34
BV Diode P+/N-	-	-	9.68	3.54
IDS En (25x0.8)	-	-	1.89	1.54
IDS Ep (25x0.8)	-	-	1.74	1.37
QBD Tunnel	-	-	2.24	1.52

Table 53. Statistical Process Control: UV EPROM Ceramic Frit-Seal Package Assembly Line, Singapore

Key Process Parameters	3Q98	4Q98	1Q99	2Q99
	CPK	CPK	CPK	CPK
Shear Test (D.A.)	4.5	6.9	6.8	7.11
Stud Pull	1.5	1.6	1.9	1.78
Bond Strength (W.B.)	5.5	6.4	6.7	6.95
SN Thickness (Tin Plate)	1.7	1.8	1.6	1.66

Table 54. Statistical Process Control: TSOP Package Assembly Line, Singapore

Key Process Parameters	3Q98	4Q98	1Q99	2Q99
	CPK	CPK	CPK	CPK
Shear Test (D.A.)	2.06	2.33	2.3	2.59
Ball Shear (W.B.)	3.42	3.43	3.9	4.09
Bond Strength (W.B.)	1.67	2.00	2.0	2.32
Coplanarity	2.82	5.47	5.2	3.94
Plating Thickness	2.30	2.03	1.8	2.39

Table 55. Statistical Process Control: PLCC Package Assembly Line, Singapore

Key Process Parameters	3Q98	4Q98	1Q99	2Q99
	CPK	CPK	CPK	CPK
Shear Test (D.A.)	3.5	4.1	3.2	3.58
Ball Shear (W.B.)	2.9	3.2	3.3	3.83
Bond Strength (W.B.)	1.8	1.9	1.8	1.88
Plating Thickness	1.9	1.9	6.5	8.43
Coplanarity	6.6	5.7	1.8	2.08

If you have any questions or suggestion concerning the matters raised in this document please send them to the following electronic mail address:

ask.memory@st.com (for general enquiries)

Please remember to include your name, company, location, telephone number and fax number