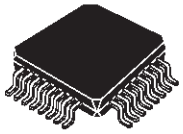
L5994
L5994A

ADJUSTABLE TRIPLE OUTPUT POWER SUPPLY CONTROLLER

PRODUCT PREVIEW

FEATURE

- DUAL PWM CONTROLLERS ADJUSTABLE
  1.9V to 5.3V(Section1)
  1.6V to 3.5V(Section2)
- AUXILIARY DRIVER FOR LINEAR REGULATOR
- CURRENT MODE CONTROL USING A LOW SENSE RESISTOR
- DUAL SYNC RECTIFIERS DRIVERS
- ”ONE SHOT” FEATURE (L5994A only)
- 96% EFFICIENCY ACHIEVABLE
- 50µA@12V STAND BY CONSUMPTION
- 4.75V TO 25V OPERATING SUPPLY VOLTAGE
- EXCELLENT LOAD TRANSIENT RESPONSE
- ”PULSE SKIPPING” FUNCTION
- OUTPUT UNDER VOLTAGE SHUTDOWN
- ADAPTATIVE ANTI SHOOT-THROUGH CONTROL
- OVER/UNDER VOLTAGE DETECTION
- POWER GOOD SIGNALS
- SEPARATED DISABLE
- THERMAL SHUTDOWN



TQFP32
ORDERING NUMBERS: L5994
L5994A

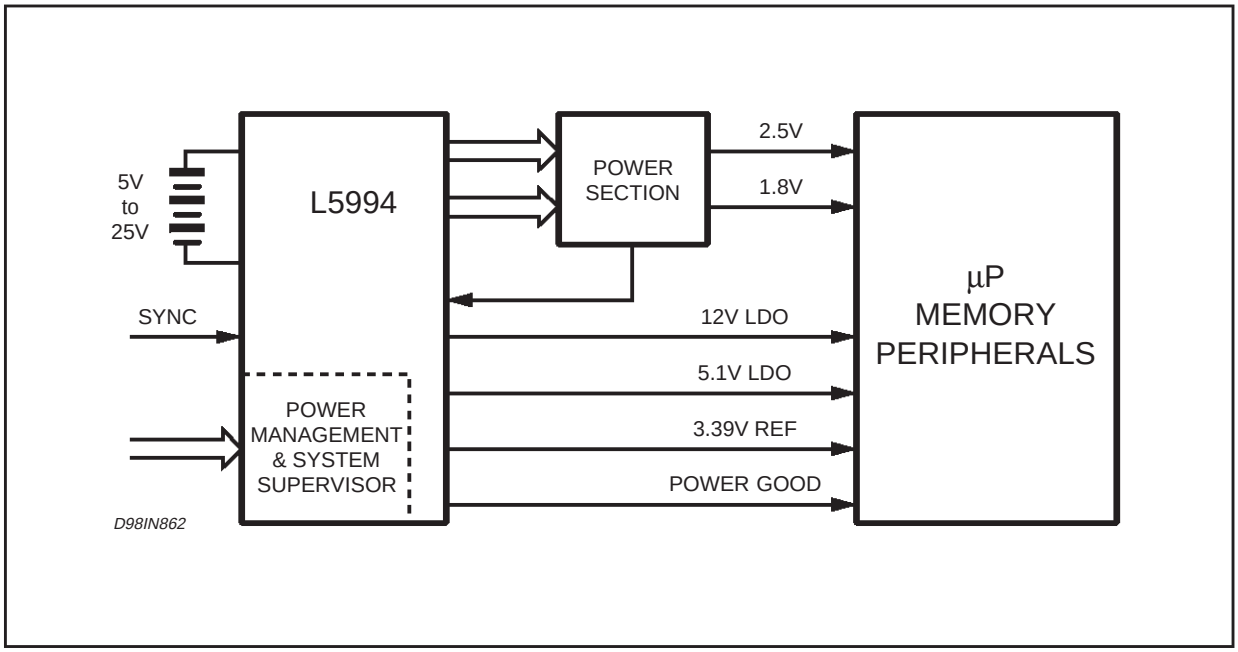
APPLICATIONS

- NOTEBOOK AND SUB NOTEBOOK COMPUTERS
- 1.8V AND 2.5V I/O SUPPLY
- WORDPAD
- INTERNET APPLIANCE

DESCRIPTION

The device provides a dual PWM controller and a linear driver controller that can support the complete power management in mobile equipment with high efficiency.

Figure 1. System Block Diagram



DESCRIPTION (continued)

The device produces an adjustable regulated voltage in both sections and a linear regulated voltage with an external bipolar such as for PCMCIA applications.
The auxiliary linear driver is able to source up to 1A for 12V bus and is also possible to use it for the regulation of 2.5V from 5V bus.
Synchronous rectification and pulse skipping mode for the buck sections optimise the overall efficiency over a wide load current range.
The two high performance PWM output sections are monitored for over voltage, under voltage and over current conditions.
A POWER GOOD signal is provided for each section.
On detection of a fault, the relevant POWER GOOD signal is generated and a specific shutdown procedure takes place to prevent physical damage and data corruption.
A disable function allows to manage the output power sections separately, optimising the quiescent consumption of the IC in stand-by conditions.
The internal architecture is a current mode that allows to have fast transient response without compromise the efficiency due to the ultra low sense resistor.
Under voltage shutdown is forced in case of short circuit in one of the two sections.
The drivers are provided of an adaptative anti cross conduction system for high output current application

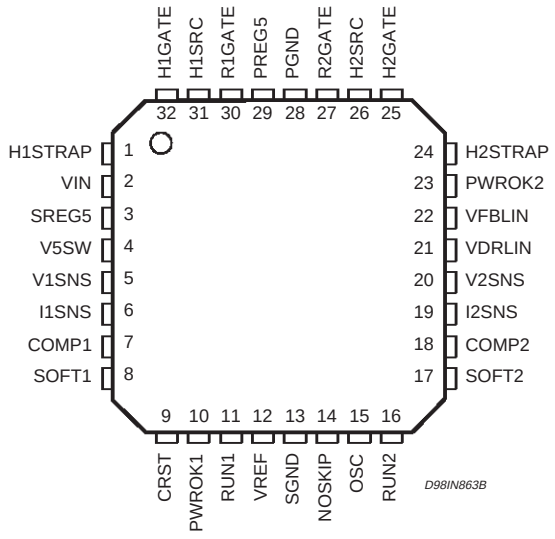
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameters	Value	Unit
V_{in}	Power Supply Voltage	0 to 27	V
V_i	Maximum pin voltage to pins 1,24,25,32	-0.3 to (V_{in} + 0.3)	V

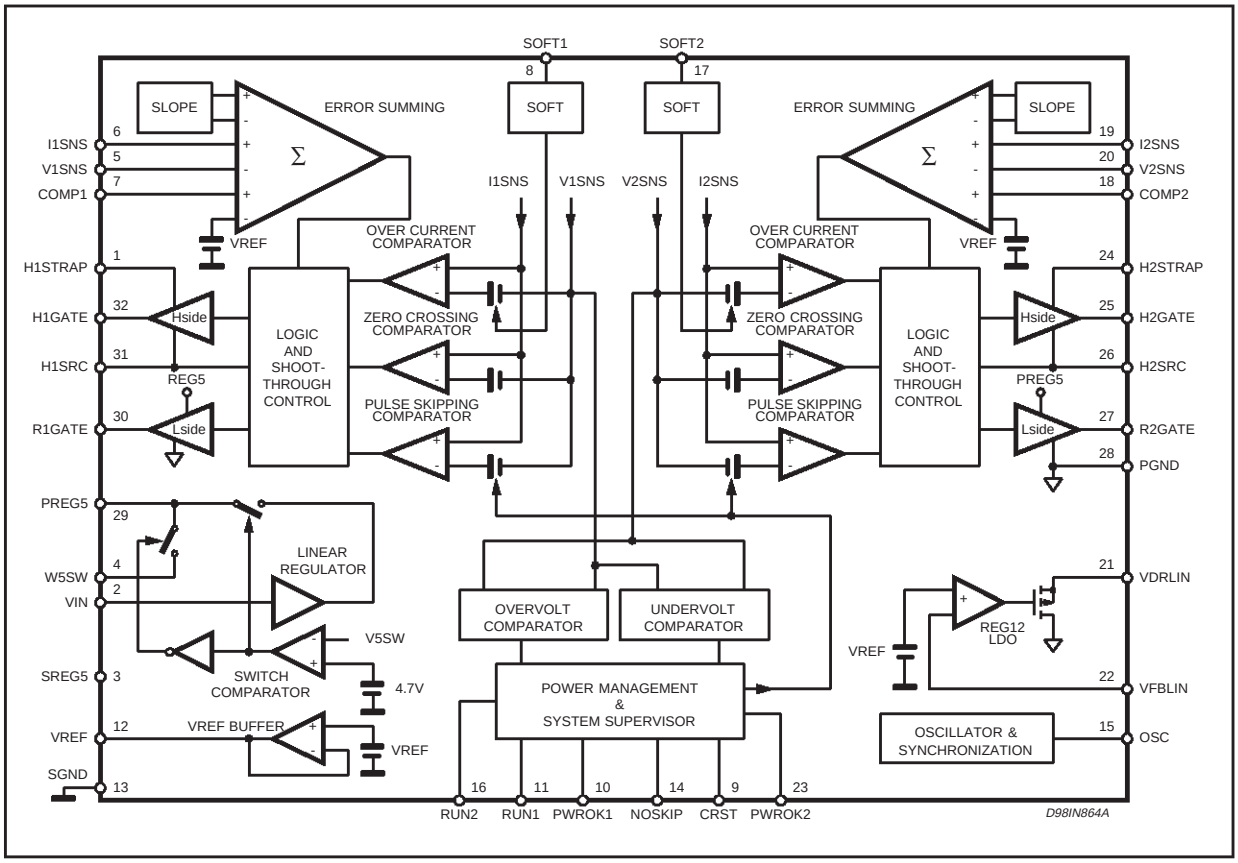
THERMAL DATA

Symbol	Parameters	Value	Unit
$R_{TH\ j\text{-}amb}$	Thermal Resistance Junction to Ambient	60	°C/W
T_j	Operative Junction Temperature Range	-40 to 140	°C

PIN CONNECTIONS (Top views)



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (V_{in} = 12V; T_j = 25°C; V_{osc} = GND; unless otherwise specified.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
DC CHARACTERISTIC						
V_{in}	Input supply voltage	V1out,4V	4.75		25	V
I_2	Operating quiescent current	R1GATE= R2GATE = OPEN H1GATE = H2GATE = OPEN RUN1= RUN2 = SREG5 (DRIVERS OFF)			1.4	mA
I_2	Stand by current	RUNQ=RUN2=GND NOSKIP=GND Vin=12V Vin=20V		 50 60	 100 120	 µA µA
SECTION 1 PWM CONTROLLER						
V_{1out}	V1SNS feedback voltage	V_{in} = 5V to 20V NOSKIP = REG5 V_{i1sns}-V_{v1sns} = 0 to 40mA	1.81	1.89	1.97	V
V_6-V_5	Overcurrent Threshold current	VSOFT1 = 3.1V	40	50	60	mV
V_6-V_5	Pulse skipping mode threshold voltage	V_{in} > 6.8V V_{in} < 5.8V		13 6.5		mV mV

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_5	Over voltage threshold ON V1SNS		2.09	2.15	2.21	V
	Under voltage threshold ON V1SNS		1.66	1.71	1.76	V
SECTION 2 PWM CONTROLLER						
V_{2out}	V2SNS feedback voltage	Vin = 5V to 20V NOSKIP = REG5 V_{i2sns}-V_{v2sns} = 0 to 40mA	1.566	1.64	1.714	V
V_{19}-V_{20}	Overcurrent Threshold current	V_{SOFT2} = 3.1V	40	50	60	mV
V_{19}-V_{20}	Pulse skipping mode threshold voltage	V_{in} > 6.8V		13		mV
V_{20}	Over voltage threshold ON V2SNS		1.843	1.9	1.957	V
	Under voltage threshold ON V2SNS		1.451	1.496	1.541	V
PWM CONTROLLERS CHARACTERISTICS						
f_{OSC}	Switching frequency accuracy	OSC = 2.5V OSC = GND OR 5V	255 170	300 200	345 230	KHz
V_{15}	Voltage range for 300KHz operation		2.4		2.6	V
T_d	Dead time	HS rise LS rise		50 30		ns
T_{ov}	Over voltage propagation time	V1SNS to PWROK or V2SNS to PWROK			1.25	µs
Tuv	Under voltage propagation time	V1SNS to PWROK or V2SNS to PWROK			1.5	µs
V_5,V_{20}	Output UVLO threshold latched	Respect output voltage	65	70	75	%
I_8,I_{17}	Soft start current		3.2	4	4.8	µA
V_8,V_{17}	Soft start clamp voltage			3.1		V
HIGH AND LOW SIDE GATE DRIVER (BOTH SECTIONS)						
I_{25},I_{27} I_{32},I_{30}	Source output peak current	C_{load} = 3.3nF		1		A
	Sink output peak current	C_{load} = 3.3nF		1		A
R_H	Rds_{ON} resistance	Driver out high		2.1	4	Ohm
R_L	Rds_{ON} resistance	Driver out low		1.5	3	Ohm
V_{OH}	Output high voltage	HSTRAP = PREG5 I_{source} = 10mA; HSOURCE = GND	4.4	5.3	5.61	V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{OL}	Output low voltage	HSTRAP = PREG5 I_{source} = 10mA; HSOURCE = GND			0.5	V
LINEAR REGULATOR DRIVER SECTION						
I_{max}	Driver current	VFBLIN < 2.5V			30	mA
V_{ref}	VFBLIN threshold	VDRLIN = 15V		2.5		V
V_{DRLIN}	Input voltage range		4.5		20	V
V_{CP}	Input voltage clamp	I_{clamp} = 100µA	16			V
	"One Shot" activation threshold (L5994A only)	VDRLIN falling	12.88	13.7	14.52	V
	"One Shot" Pulse (L5994A only)				1.5	µs
INTERNAL REGULATOR DRIVER SECTION						
V_{29}	VREG5 output voltage	V_{in} = 7 to 25V	5.0	5.3	5.5	V
I_{29}	Totale current capability	V_{PREG5} = 5.3V V_{in} = 7V	25 70			mA
V_{5SW}	Swith-over threshold voltage	V_{in} > 7V, V_{5SW} fall	4.3	4.53	4.7	V
V_{12}	Reference voltage	I_{load} = 1mA V_{in} = 5 to 20V I_{load} = 1 to 5mA	2.45 2.425	2.5 2.5	2.55 2.575	V
I_{12}	Source current at reference voltage	V_{12} = Vref-0.3V			15	mA
POWER GOOD AND ENABLE FUNCTION						
V_{16},V_{11}	RUN1, RUN2, enable voltage	High level	2.4			V
V_{16},V_{11}	RUN1, RUN2, disable voltage	Low level			0.8	V
T_{10}	Power good delay	CRST=100nF	115	147	180	ns
T_{27},T_{30}	Shutdown delay time before LS activation (except for over voltage fault)	CRST=100nF	115	147	180	ns
	CRST timing rate	V_{12} = Vref-0.3V		1.47		ms/nF
	Power good high level	$I_{POWEROK}$ = 40µA	4.1			V
	Power good low level	$I_{POWEROK}$ = 320µA			0.4	V
SYNCHRONIZATION						
V_{15}	Synchronization pulse width	Fsw = MHz	400			ns
	Synchronization input voltage (falling edge)	$I_{POWEROK}$ = 320µA	5			V

PIN DESCRIPTION

N°	Name	Function
1	H1STRAP	Section 1 bootstrap capacitor connection. A bootstrap capacitor must be connected between this pin and pin H1SRC to supply the H1GATE driver.
2	Vin	Device supply voltage.
3	SREG5	Internal logic supply. It must be connected to PREG5 pin through a R-C low-pass filter.
4	V5SW	Alternative supply voltage for the internal 5V regulator. If its voltage is greater than 4.5V, the internal regulator is supplied via this pin. If left floating, the regulator is supplied through the Vin pin.
5	V1SNS	This pin connects the (-) input of section 1 current sense comparator. It must be connected downstream the external R_{SENSE} resistor.
6	I1SNS	This pin connects the (+) input of section 1 current sense comparator. It must be connected upstream the external R_{SENSE} resistor.
7	COMP1	Feedback input for section 1. It must be connected directly or through a resistor divider to the output of the section 1.
8	SOFT1	Soft start connection for section 1. The soft start time is programmed by an external capacitor connected between this pin and SGND. Approximatively 0.7ms/nF.
9	CRST	Used for start-up and shut-down timing. A capacitor must be connected between this pin and SGND defining a time of 1.47ms/nF.
10	PWROK1	Power Good open drain diagnostic signal. This output is in high inpedence when sect. 1 is enabled and running properly after a delay defined by the CRST capacitor. When not used may be left floating.
11	RUN1	Control input to enable / disable the section 1. A high logic level (>2.4V) enables this section, a low level (<0.8V) shuts it down.
12	Vref	Internal 2.5V high accuracy voltage generator. It can source 5mA to external load. Bypass to SGND with a 4.7uF electrolytic capacitor to reduce noise.
13	SGND	Signal ground. Reference for internal logic circuitry. It must be routed separately from high current returns.
14	NOSKIP	Pulse skipping mode control. A high logic level (>2.4V) disables pulse skipping at low load current, a low level (<0.8V) enables it.
15	OSC	Oscillator frequency control: connect to 2.5V to select 300kHz operation, connect to ground or to 5V for 200kHz operation. A proper external signal can synchronise the oscillator
16	RUN2	Control input to enable / disable the section 2. A high logic level (>2.4V) enables this section, a low level (<0.8V) shuts it down.
17	SOFT2	Soft start connection for section 2. The soft start time is programmed by an external capacitor connected between this pin and SGND. Approximatively 0.7ms/nF.
18	COMP2	Feedback input for section 2. It must be connected directly or through a resistor divider to the output of the section 2.
19	I2SNS	This pin connects the (+) input of section 2 current sense comparator. It must be connected upstream the external R_{SENSE} resistor.
20	V2SNS	This pin connects the (-) input of section 2 current sense comparator. It must be connected downstream the external R_{SENSE} resistor.

PIN DESCRIPTION (continued)

N°	Name	Function
21	VDRLIN	Linear regulator driver connection. It must be connected to the base pin of an external PNP transistor and, through a resistor, to its emitter in order to supply the internal driver. If no linear regulation is implemented, it may be left floating.
22	VFBLIN	Feedback input for the linear regulator. It must be connected directly, or through a resistor divider, to the linear regulated output. If no linear regulation is implemented, it may be left floating
23	PWROK2	Power Good open drain diagnostic signal. This output is in high inpedence when sect. 2 is enabled and running properly after a delay defined by the CRST capacitor. When not used may be left floating.
24	H2STRAP	Section 2 bootstrap capacitor connection. A bootstrap capacitor must be connected between this pin and pin H2SRC to supply the H2GATE driver.
25	H2GATE	Gate driver for the section 2, high side NMOS
26	H2SRC	Section 2 High side NMOS source connection.
27	R2GATE	Gate driver for the section 2, low side NMOS (synchronuos rectifier)
28	PGND	Current return for power mosfet driver for both sections. Connect to the low side mosfet sources pin. It must be routed separately from signal current returns
29	PREG5	5V internal regulator output. Used mainly to supply the bootstrap capacitors and the internal circuitry connected to SREG5 via a low-pass filter.
30	R1GATE	Gate driver for the section 1, low side NMOS (synchronuos rectifier)
31	H1SRC	Section 1 High side NMOS source connection.
32	H1GATE	Gate driver for the section 1, high side NMOS

Detailed Functional Description

In the device block diagram six fundamental functional blocks can be identified:

- 1.9V to 5.1V step-down PWM switching regulator (section 1, pins 1, 4 to 8, 30 to 32);
- 1.66V to 3.3V step-down PWM switching regulator (section 2, pins 17 to 20, 24 to 27);
- Linear regulator driver for an external PNP transistor (pins 21,22);
- 5V low drop-out linear regulator (pin 29);
- 2.5V reference voltage generator (pin 12);
- Power Management section (pins 9 to 11, 14,16).

The chip is supplied through pin Vin (2), typically by a battery pack or the output of an AC-DC adapter, with a voltage that can range from 5V to 25V. The return of the bias current of the device is the signal ground pin SGND (13), which references the internal logic circuitry. The drivers of the external MOSFET's have their separate current return, namely the power ground pin PGND (28). Take care of keeping separate the routes of signal ground and the power ground pin when laying out the PCB (see "Layout and grounding" section). The two PWM regulators share the internal oscillator, programmable or synchronizable through pin OSC (15).

PWM Regulators

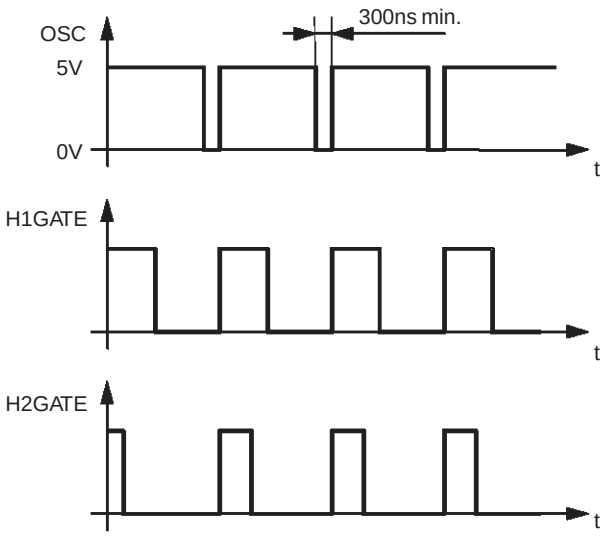
Each PWM regulator includes control circuitry as well as gate-drive circuits for a step-down DC-DC converter in buck topology using synchronous rectification and current mode control.
The two regulators are independent and almost identical. As one can see in the Block Diagram, they share only

the oscillator and the internal supply and differ for the pre-set output voltages.
Each converter can be turned on and off independently: RUN1 and RUN2 are control inputs which disable the relevant section when a low logic level (below 0.8 V) is applied and enable its operation with a high logic level (above 2.4 V). When both inputs are low the device is in stand-by condition and its current consumption is extremely reduced (less than 120mA over the entire input voltage range).
The device is able to regulate the desired output voltage in two different ways: classic PWM operation and Pulse Skip operation (see the relevant sections).

Oscillator

The oscillator, which does not require any external timing component, controls the PWM switching frequency. This can be either 200 or 300 kHz, depending on the logic state of the control pin OSC, or else can be synchronized by an external oscillator.
If the OSC pin is grounded or connected to pin PREG5 (5V) the oscillator works at 200kHz. By connecting the OSC pin to a 2.5 V voltage, 300 kHz operation will be selected. Moreover, if pin OSC is fed with an external signal like the one shown in fig. 2, the oscillator will be synchronized by its falling edges.
Considering the spread of the oscillator, synchronization can be guaranteed for frequencies above 230kHz. Even though a maximum frequency value is in practice imposed by efficiency considerations it should be noticed that increasing frequency too much arises problems (noise, subharmonic oscillation, etc.) without significant benefits in terms of external component size reduction and better dynamic performance.
The oscillator imposes a time interval (300 ns min.), during which the high-side MOSFET is definitely OFF, to recharge the bootstrap capacitor (see "MOSFET's Drivers" section). This, implies a limit on the maximum duty cycle (88.5%@fSW=300kHz, 92.6%@fsw=200kHz, worst case) which, in turn, imposes a limit on the minimum operating input voltage.

Figure 2. Synchronization signal and operation



PWM Operation

The control loop does not employ a traditional error amplifier in favour of an error summing comparator which sums the reference voltage, the feedback signal, the voltage drop across an external sense resistor and a slope compensation ramp (to avoid subharmonic oscillation with duty cycles greater than 50%) with the appropriate signs.
With reference to the schematic of fig. 3, the output latch of both controllers is set by every pulse coming from

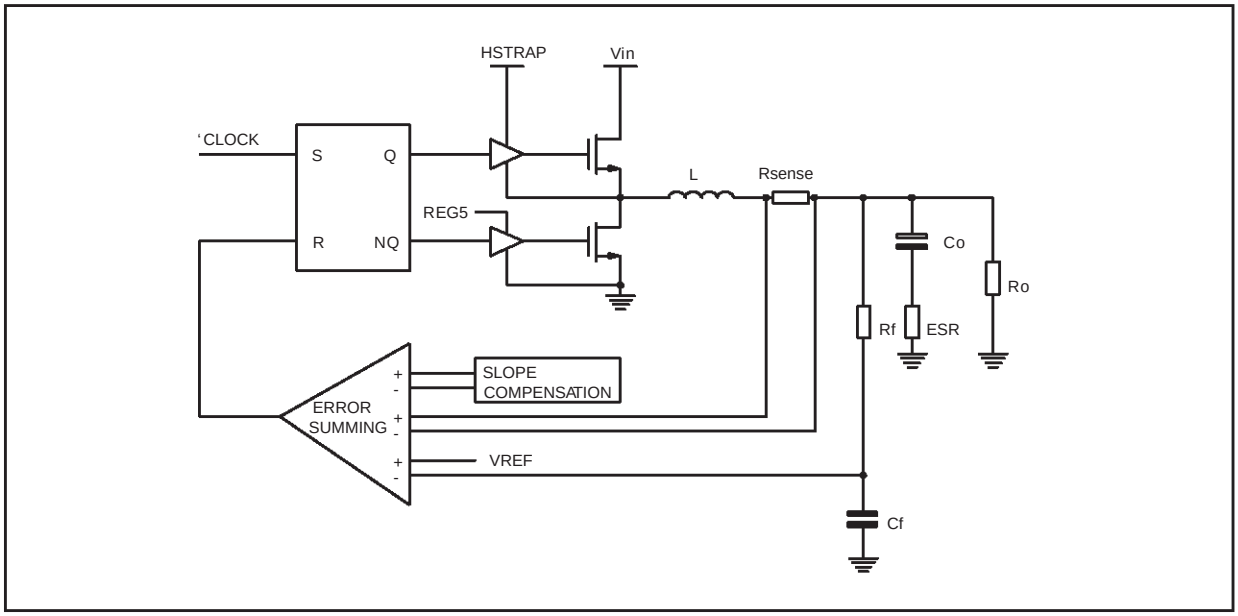
the oscillator. That turns off the low-side MOSFET (synchronous rectifier) and, when the low-side gate voltage falls below 0.3V to prevent cross-conduction, turns on the high-side one, thus allowing energy to be drawn from the input source and stored in the inductor.
The error summing, by comparing the above mentioned signals, determines the moment in which the output latch is to be reset. The high-side MOSFET is then turned off and the synchronous rectifier is turned on when the voltage on the high-side MOSFET source falls below 2V to prevent cross-conduction, thus making the inductor current recirculate. The high side mosfet is in any case turned off on the clock signal falling edge: this is the reason why the duty cicle is limited in its maximum value.
The reached state is maintained until the next oscillator pulse.
The open-loop transfer function of such a kind of control system, under the assumption of an ideal slope compensation, is:

$$F(s) = A \cdot \frac{R_o}{2 \cdot R_{sense}} \cdot \frac{1 + s \cdot ESR \cdot C_O}{(1 + s \cdot R_o \cdot C_o) \cdot (1 + s \cdot R_F \cdot C_F)}$$

where A is the gain of the error summing comparator, which is 2 by design.

The system is inherently very fast since it tends to correct output voltage deviations nearly on a cycle-by-cycle basis. Actually, in case of line or load changes, few switching cycles can be sufficient for the transient to expire. The operation above illustrated is modified during particular or anomalous conditions. Leaving out other circumstances (described in "Protections" section) for the moment, consider when the load current is low enough or during the first switching cycles at start-up: the inductor current may become discontinuous, so it is zero during the last part of each cycle. In such a case, a "zero current comparator" detects the event and turns off the synchronous rectifier, avoiding inductor current reversal and reproducing the natural turn-off of a diode when reverse biased. This allows to increase the efficiency in ligth load. Both MOSFET's stay in off state until the next oscillator pulse.

Figure 3. Control loop.



Synchronous Rectification

Very high efficiency is achieved at high load current with the synchronous rectification technique, which is particularly advantageous because of the low output voltage. The low-side MOSFET, that is the synchronous rectifier, is selected with a very low on-resistance, so that the paralleled Schottky diode is not turned on, except for the small time in which neither MOSFET is conducting. The effect is a considerable reduction of power loss during the recirculation period.

Although the Schottky might appear to be redundant, it is not in a system where a very high efficiency is required. In fact, its lower threshold prevents the lossy body-diode of the synchronous rectifier MOSFET from turning on during the above mentioned dead-time. Both conduction and reverse recovery losses are cut down and efficiency can improve of 1-2% in some cases. Besides a small diode is sufficient since it conducts for a very short time.

See the "Power Management" section to see how both synchronous rectifiers are used to ensure zero voltage output in stand-by conditions or in case of overvoltage.

Pulse-skipping operation

To achieve high efficiency at light load current as well, under this condition the regulators change their operation (unless this feature is disabled): they abandon PWM and enter the so-called pulse-skipping mode, in which a single switching cycle takes place every many oscillator periods.

The "light load condition" is detected when the voltage across the external sense resistor (V_{RSENSE}) does not exceed the pulse skipping threshold (13mV typ.) while the high-side MOSFET is conducting. When the reset signal of the output latch comes from the error summing comparator while V_{RSENSE} is below this value, it is ignored and the actual reset is driven as soon as V_{RSENSE} reaches the pulse skipping threshold. This gives some extra energy that maintains the output voltage above its nominal value for a while. The oscillator pulses now set the output latch only when the feedback signal indicates that the output voltage has fallen below its nominal value. In this way, most of oscillator pulses are skipped and the resulting switching frequency is much lower, as expressed by the following relationship:

$$f_{PS} = K \cdot \frac{R_{SENSE}^2}{L} \cdot I_{OUT} \cdot V_{OUT} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where $K = 3.2 \times 10^3$ and f_{PS} is in Hz. As a result, the losses due to switching and to gate-drive, which mostly account for power dissipation at low output power, are considerably reduced.

The section 1 can work with the input voltage very close to the output one (i.e. the output voltage is 5V), where the current waveform may be so flat to prevent pulse-skipping from being activated. To avoid this, the pulse-skipping threshold (of section 1 only) is roughly halved at low input voltages ($V_{IN} < 6.8V$). Under this condition, in the above formula the constant K becomes 12.8×10^3.

When in pulse-skipping, the output voltage is some ten mV higher than in PWM mode, just because of its mode of operation. If this "load regulation" effect is undesirable for any reason, the pulse skipping feature can be disabled (see "Power Management" section) to the detriment of efficiency at light load.

MOSFET's Drivers

To get the gate-drive voltage for the high-side N-channel MOSFET a bootstrap technique is employed. A capacitor is alternately charged through a diode from the 5V PREG5 line when the high-side MOSFET is OFF and then connected to its gate-source leads by the internal floating driver to turn the MOSFET on. The PREG5 line is used to drive the synchronous rectifier as well, and therefore the use of low-threshold MOSFET's (the so-called "logic-level" devices) is highly recommended.

The drivers are of "dynamic" type, which means they do not give origin to current consumption when they are in static conditions (ON or OFF), but only during transitions. This feature is aimed at minimizing the power consumption of the device even during stand-by when both low-side MOSFET's are ON.

Adaptative anti shoot-through protection is implemented to prevent cross-conduction: the low side mosfet turn on is disbled until the HSRC pin is above 2V and, in the same way, the high side mosfet turn on is disabled until the RGATE pin is above 0.3V. During the time in which both mosfets are in off state, the recirculation of the current is insured by the schottky diode. The resulting dead time depends on the mosfets used and on the current flowing in the inductor; in this way many kinds of mosfets may be used and cross conduction is avoided.

Protections

Each converter is fully protected against fault conditions. A monitoring system checks for overvoltages of the output, quickly disabling the interested converter in case such an event occurs. This condition is latched and to allow the device to start again either the supply voltages have to be removed or the relative RUNx pin has to be driven low.

Also the undervoltage conditions are detected: a light undervoltage (90% of the programmed value) only causes the relative PWROKx to be driven low while an hard undervolatge (70% of the programmed value) causes interruption of the operation of both converters. This is a protection against short circuits.

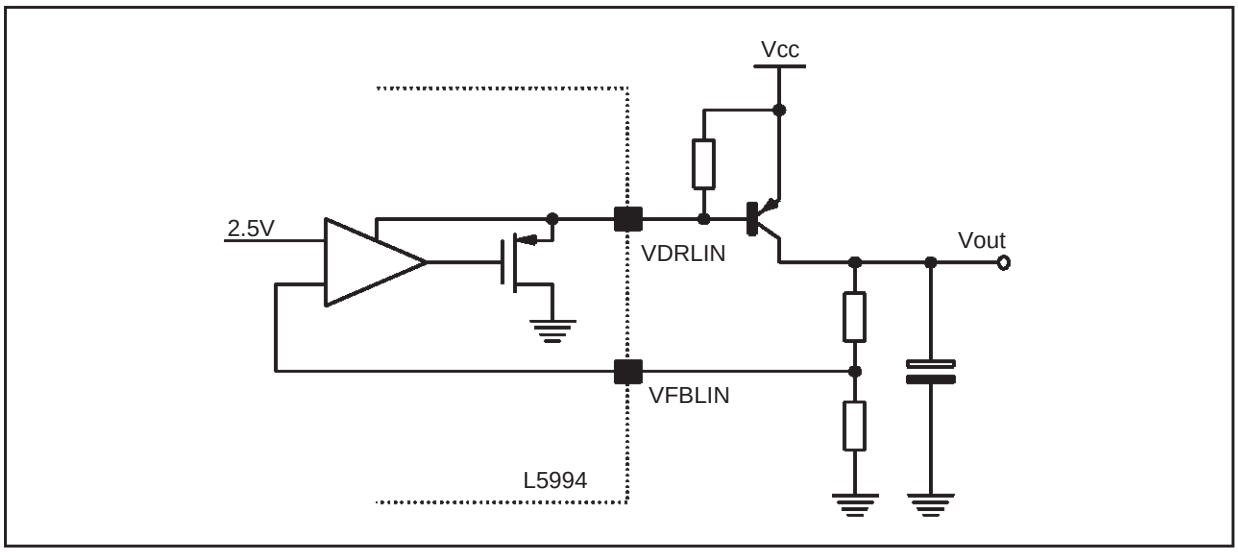
PWROKx signals (at pin 10 and 23) reveals the anomaly of the relative section (output voltage not within the ±10% of the programmed voltage) with a low output level. If the chip overheats (above 135°C typ.) the device stops operating as long as the temperature falls below a safe value (105°C typ.). The overtemperature condition is signalled by a low level on both PWROKx as well.

A current limitation comparator prevents from excessive current in case of overload. It intervenes as the voltage VRSENSE exceeds 50mV, turning off the high-side switch before the error summing does. By the way, this also gives the designer the ability to program the maximum operating current by selecting an appropriate sense resistor. This pulse-by-pulse limitation gives a quasi-constant current characteristic.

Linear Driver

The Linear driver is capable of sinking up to 60mA from an external PNP transistor through the pin VDRLIN considering the typical application circuit shown in fig. 4. The internal comparator is supplied by the same pin VDRLIN which accepts voltages included in the range from 4.5V to 20V. If the application works with input voltages that allows the regulation, the supply for the regulator can be obtained directly from the input source (VIN). If such is not the case and is not available an additional input voltage, the most convenient way to get the supply is to use an auxiliary winding on one of the two sections inductor with a catch diode, DS, and a filter capacitor, CS, as shown in fig. 5. This winding delivers energy to pin VDRLIN during the recirculation period of each switching cycle with a voltage determined by the turns ratio n and little dependent on the input voltage.

Figure 4. Linear regulator supply with auxiliary winding



In case the section with the auxiliary winding is working at full load and the linear regulator is lightly loaded, the voltage at pin VDRLIN can exceed the expected value. In fact, DS and CS act as a peak-holding circuit and VDRLIN is influenced by the voltage spikes at switching transients. An internal clamp limits the voltage on the VDRLIN pin at a maximum value of 16V, but, in case of intervention, the chip power dissipation will rise.The linear driver is always active as long as PREG5 and VREF are present on the chip (see the relevant section); it

works in order to obtain a voltage on the VFBLIN pin of about 2.5V. In this way, the minimum regulated voltage is of 2.5V, obtained connecting directly the VFBLIN pin to the output, while the maximum is of about the supply voltage minus the bipolar PNP VceSAT.

For a correct operation of the regulator, the voltage at pin VDRLIN must not be too low. The flyback connection of the two windings ensures a well regulated voltage, provided if there is good magnetic coupling. The coupled inductors configuration, however, is not able to sustain the auxiliary voltage if the main output is lightly loaded: the secondary voltage drops and the system goes out of regulation.

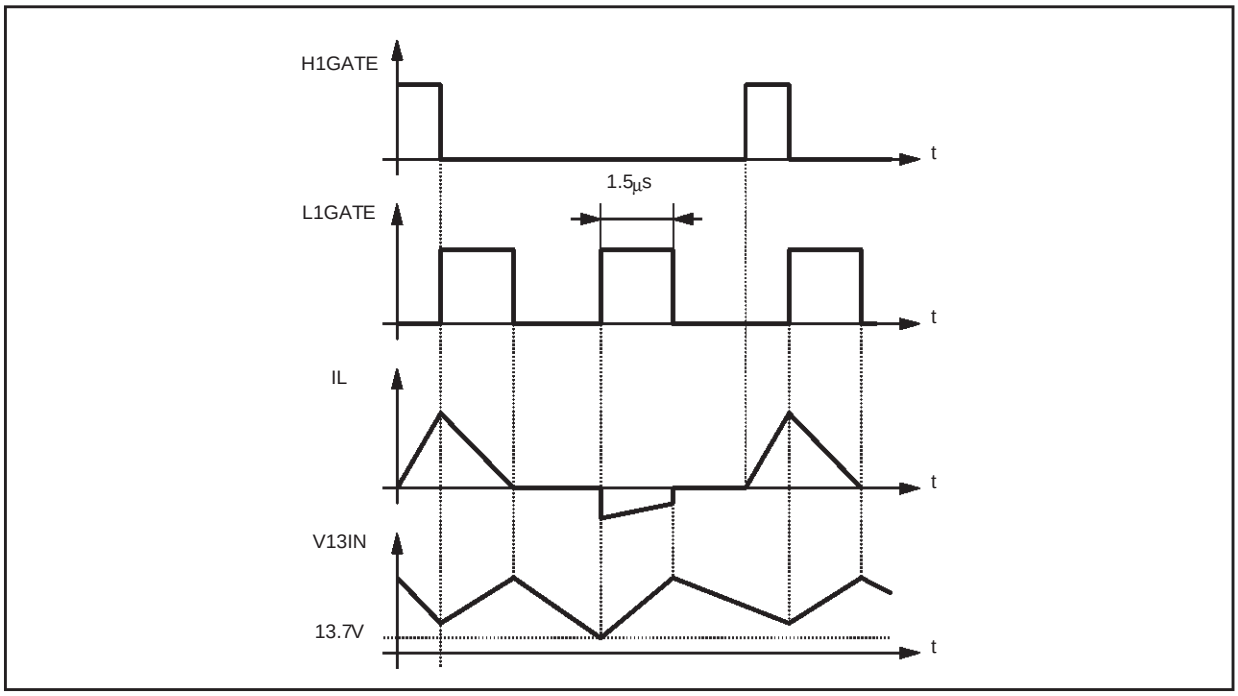
The additional winding may be implemented with L5994 if the relative section is loaded enough.

To overcome this problem, in L5994A, when the VDRLIN voltage falls below a certain threshold (13.7V ±5%) because of too light a load on the section 2, the relevant synchronous rectifier is turned on for 1.5 ms max. during the interval in which the inductor current is zero (”one-shot” feature, see fig. 6). In this way, the inductor current reverses and draws from the output capacitor energy which is forward transferred to the auxiliary output.

Since that the linear driver is supplied from the VDRLIN pin, if the linear regulator is not necessary for the application, leave floating this pin implies that the linear driver is not supplied and so no power is wasted (L5994 only).

The linear regulator is active, if at the least one of the two runx signal is asserted

Figure 5. ”One Shot” pulse to substain VDRLIN voltage



+5V Linear Regulator and +2.5V Reference Voltage Generator

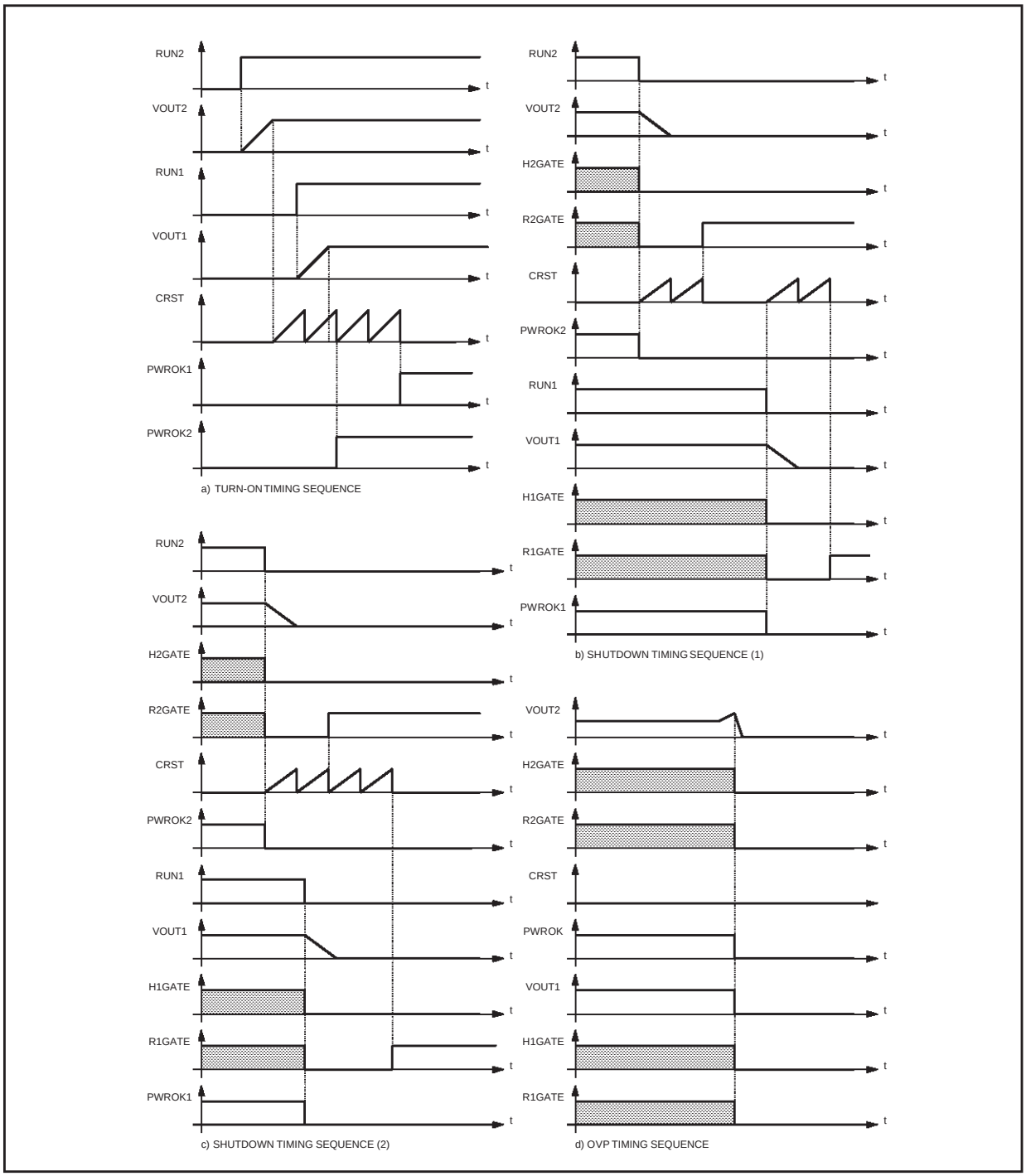
The 5V low drop-out regulator powers directly the MOSFET drivers and it is externally available through pin PREG5. A low pass filter is connected between PREG5 pin and SREG5 pin from who all the internal circuitry is powered. The introduction of this R-C network is useful to minimize noise effects.

The typical external use of this generator is to charge the bootstrap capacitors used to produce the gate-drive voltage for the high-side MOSFET’s of both PWM converters.

At start-up and when the 5V section is not operating, this regulator is powered by the chip input voltage. To reduce power consumption, the linear regulator is turned off and the PREG5 pin is internally connected to the 5V PWM regulator output via V5SW pin, when the 5V PWM regulator is active and its output voltage is above the switchover threshold, 4.5V. This happens when V5SW pin is connected to the section 1 output regulating 5V. In any case, if V5SW is above 4.5V, the internal regulator is turned off and PREG5 is powered through this pin.

The 5V regulator is always active, even if both PWM regulators are disabled, as long as power is applied to the chip.
The 2.5V reference voltage generator, provides comparison levels for threshold detection and device operation. It is allowed to source up to 5mA to an external load from its buffered output, externally available through pin VREF.
The reference voltage generator is active if at least one of the two RUNx signal is asserted.
If either PREG5 or VREF does not deliver the correct voltage, the device is shut down.

Figure 6. Controlled timing sequencies



Power management

The device is provided with some control pins suitable to perform some functions which are commonly used or sometimes required in battery-operated equipment. Besides, it features controlled timing sequences in case of turn-on/off and device shutdown for a safe and reliable behaviour under all conditions.
As above mentioned, RUN1 and RUN2 pins allow to disable separately both PWM converters by means of logic signals (likely coming from a µP) as mentioned earlier.
NOSKIP can disable the pulse-skipping feature: when it is held high neither of the PWM regulators is allowed to enter this kind of operation.
The two PWROKx signals, one for each section, drive low immediately when the relative PWM regulator output falls below its own undervoltage (light or hard) threshold or when it is disabled. It is high when the relative regulator runs properly.
A capacitor connected between CRST and ground fixes a time, in the order of 1.5msec/nF, which delays the transition low-high of PWROKx. This happens at start-up of each section or after recovering an undervoltage condition using the relative RUNx command. The delay starts from the moment in which the output voltage has reached its correct value.
The same delay intervenes also in another circumstance: when a section is disabled (because its RUNx is driven low or owing to a thermal shutdown), the relevant synchronous rectifier is turned on after the above delay in order to make sure that the load is no longer supplied.
This delay, however, does not intervene in case of overvoltage: the synchronous rectifier is immediately turned on after the shutdown, thus acting as a built-in "crowbar".
All these timing sequences are illustrated in fig. 7.

Design procedure

Basically, the application circuit topology is fixed, and the design procedure concerns only the selection of the component values suitable for the voltage and current requirements of the specific application.
The design data one needs to know are therefore:

- Input voltage range: the minimum (V_{INMIN}) and the maximum (V_{INMAX}) voltage under which the application is expected to operate;
- Maximum load current for each of the two sections;
- I_{out1} for the section 1;
- I_{out2} for the section 2;
- Output voltage and current for the linear regulator, setted for 12V 50mA using an additional winding on the 5.1V section;
- Maximum peak-to-peak ripple amplitude of the output voltage for each switching section:
- V_{rpp1} for the section 1;
- V_{rpp2} for the section 2;
- The operating frequency f_{SW} (200kHz / 300kHz or externally synchronized).

It is worth doing some preliminary considerations. The selection of the switching frequency depends on the requirements of the application. If the aim is to minimize the size of the external components, 300kHz will be chosen. For low input voltage applications 200kHz is preferred, since it leads to a higher maximum duty cycle.
As for the switching regulators, the inductance value of the output filter affects the inductor current ripple: the higher the inductance the lower the ripple. This implies a lower current sense resistor value (for a given IOUT), lower core losses and a lower output voltage ripple (for a given output capacitor) but, on the other hand, more copper losses and a worse transient behaviour due to load changes. Usually the maximum ripple peak-to-peak amplitude (which occurs at V_{INMAX}) is chosen between 15% and 50% of the full load current. It is convenient to introduce a ripple factor coefficient, RF, that is therefore a number between 0.15 and 0.5.
As for the linear regulator, its input voltage VDRLIN should not fall below 12V and therefore the auxiliary winding, if used, should be dimensioned to get this voltage with a certain margin (say, 13-14V). Conversely, an higher input voltage leads to higher losses inside the PNP transistor, to the detriment of efficiency, and to higher total current on the +5V inductor. Besides it implies a higher turns ratio and therefore a worse magnetic coupling, which affect energy transfer during flyback.

+3.3V Inductor

To define the inductor, it is necessary to determine firstly the inductance value. Its minimum value is given by:

$$L_{3MIN} = \frac{3.3 - (V_{INMAX} - 3.3)}{V_{INMAX} \cdot f_{SW} \cdot I_{OUT3} \cdot RF}$$

and a value $L_3 > L_{3MIN}$ should be selected. Core geometry selection is connected to the requirements of the specific application in terms of space utilization and other practical issues like ease of mounting, availability and so on. As to the material, the choice should be directed towards ferrite, molypermalloy or KoolMμ, to achieve high efficiency. These materials provide low core losses (ferrite in particular), so that the design can be concentrated on preventing saturation and limiting copper losses. Saturation must be avoided even at maximum peak current:

$$I_{L3PK} = I_{OUT3} + \frac{3.3 \cdot (V_{INMAX} - 3.3)}{2 \cdot f_{SW} \cdot L_3 \cdot V_{INMAX}}$$

To limit copper losses, the winding DC resistance, R_L, should be as low as possible (in the range of mΩ). AC losses can usually be neglected. A practical criterion to minimize DC resistance could be to use the largest wire that fits the selected core.

Anyway the best solution, whenever possible, is to use an off-the-shelf inductor which meets the requirements in terms of inductance and maximum DC current. Nowadays there is a broad range of products offered by manufacturer, also for surface mount assemblies.

+5.1V Transformer

The primary winding carries the secondary power as well, thus the total primary average current is:

$$I_{TOT5} = I_{OUT5} + \frac{V_{INLIN} \cdot I_{OUT12}}{5.1}$$

where V_{DRLIN} is the voltage generated during the recirculation of the primary and fed into the input of the +12V linear regulator. The turns ratio 1:n of the transformer is chosen so that V_{DRLIN} is above 13V. To reduce the turns ratio in order to minimize stray parameters, the secondary is referred to the 5.1V output, and therefore the minimum value is given by:

$$\eta_{MIN} = \frac{V_{INLIN} - 5.1 + V_f}{5.1}$$

where V_f is the forward drop across the rectifier (assume 1V to be conservative). Make sure the secondary is connected with the proper polarity (see fig. 4). The minimum primary inductance value can be expressed as:

$$L_{5pmin} = \frac{3}{4} \cdot \frac{5.1 \cdot (V_{IN} - 5.1)^2}{V_{IN} \cdot f_{SW} \cdot [I_{TOT5} \cdot RF \cdot (V_{IN} - 5.1) - \eta \cdot V_{IN} \cdot I_{OUT12}]}$$

where RF, to get positive values for L_{5PMIN}, must satisfy the inequality:

$$RF > \frac{\eta \cdot V_{IN} \cdot I_{OUT12}}{I_{TOT5} \cdot (V_{IN} - 5.1)}$$

and where V_{IN} can be either V_{INMIN} or V_{INMAX}, whichever gives the higher value for L_{5PMIN}. With a primary inductance $L_{5P} > L_{5PMIN}$ the primary peak current, which must not saturate the magnetic core, will be:

$$I_{5PK} = I_{5TOT} + \frac{5.1 \cdot (V_{INMAX} - 5.1)}{2 \cdot f_{SW} \cdot L_{5P} \cdot V_{INMAX}} + \eta \cdot I_{OUT12}$$

As to the transformer realization, the considerations regarding to the +3.3V inductor can be here repeated.

Power MOSFET's and Schottky Diodes

Since the gate drivers of the device are powered by a 5V bus , the use of logic-level MOSFET's is highly recommended, especially for high current applications. Their breakdown voltage $V_{(BR)DSS}$ must be greater than V_{INMAX} with a certain margin, so the selection will address 20V or 30V devices.

The $R_{DS(ON)}$ can be selected once the allowable power dissipation has been established. By selecting identical power MOSFET's as the main switch and the synchronous rectifier, the total power they dissipate does not depend on the duty cycle. Thus, if PON is this power loss (few percent of the rated output power), the required RDS(ON) (@ 25 °C) can be derived from:

$$R_{DS(ON)} = \frac{P_{ON}}{I_{OUT}^2 \cdot (1 + \alpha \cdot \Delta T)}$$

where I_{out} is either I_{TOT5} or I_{OUT3}, according to the section under consideration, a is the temperature coefficient of $R_{DS(ON)}$ (typically, $a = 5 \cdot 10^{-3}\ °C^{-1}$ for these low-voltage classes) and ΔT the admitted temperature rise. It is worth noticing, however, that generally the lower $R_{DS(ON)}$, the higher is the gate charge Q_g, which leads to a higher gate drive consumption. In fact, each switching cycle, a charge Q_g moves from the input source to ground, resulting in an equivalent drive current:

$$I_g = Q_g \cdot f_{SW}$$

which affects efficiency at low load currents. Besides, this current is drawn from the PREG5 line whose source capability, I_{SRC} (25mA min), must not be exceeded, thus a further constraint concernes the MOSFET total gate charge (@V_{GS} = 5V):

$$Q_g \leq \frac{I_{SRC}}{4 \cdot f_{SW}}$$

assuming four identical MOSFET's.

The Schottky diode to be placed in parallel to the synchronous rectifier must have a reverse voltage V_{RRM} greater than V_{INMAX}. Since it conducts for less than 5% of the switching period, the current rating can be much lower than Iout. The selection criterion should be:

$$V_{t(Schottky)} < V_{t(body\text{-}diode)} @ I = I_{LPK}$$

Sense Resistors

The sense resistor of each section is selected according to their respective maximum output current. The current sense comparator limits the inductor peak current and therefore the maximum DC output current is the peak value less half of the peak-to-peak ripple. The intervention threshold is set at 50mV for both sections, thus the resistor values should be:

$$R_{SENSE5} = \frac{50}{I_{L5PK}} [m\Omega] \qquad R_{SENSE5} - \frac{50}{I_{L5PK}} [m\Omega]$$

Since the comparator threshold that triggers pulse-skipping mode is 11mV, the output current at which the system enters this kind of operation is approximately one fourth of the maximum output current. The sense resistors values are in the low milliohms thus it is important to take correctly the current sense signals. Make sure that the Kelvin connections between the current sense pins of the IC and the sense resistor do not carry the output current.

Input Capacitors

A pulsed current (with zero average value) flows through the input capacitor of a buck converter. The AC component of this current is quite high and dissipates a considerable amount of power on the ESR of the capacitor:

$$Pc_{IN} = ESR \cdot I_{OUT}^2 \cdot \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{V_{IN}^2}$$

It is easy to find that PCIN has a maximum equal to IOUT/2 (@ VIN=2×VOUT, that is, 50% duty cycle). The input capacitor of each section, therefore, should be selected for a RMS ripple current rating as high as half the respective maximum output current. The capacitance value is not very important but in reality a minimum value must be ensured for stability reasons. In fact, switching regulators exhibit a negative input impedance that, at low frequencies, is:

$$Z_{IN(DC)} = \frac{V_{IN}^2}{V_{OUT} \cdot I_{OUT}}$$

thus, if the impedance of the power source is not well below the absolute value of $Z_{IN(DC)}$ at frequencies up to the bandwidth of the regulator control loop, there is the possibility for oscillations. To ensure stability, the following condition must be satisfied:

$$C_{IN} \gg \frac{L_{EQ}}{ESR_{IN} \cdot |Z_{IN(DC)}|}$$

where L_{EQ} is the inductance of the circuit upstream the switching regulator input and ESR_{IN} is related to the input capacitor itself.The use of high performance electrolytic capacitors is recommended. If a higher cost is of no concern, OS-CON capacitors are an excellent choice because they offer the smallest size for a given ESR or current rating. Tantalum capacitors do not tolerate pulsed current, so their use is not advisable.

Output Capacitors

The output capacitor selection is based on the output voltage ripple requirements. This ripple is related to the current ripple through the inductor and is almost entirely due to the ESR of the output capacitor. Therefore, the goal is to achieve an ESR lower than a certain value, regardless of the actual capacitance value.

The maximum current ripple of the +3.3V section is:

$$\Delta I_{L3} = 2 \cdot (I_{L3PK} - I_{OUT3})$$

considering the values obtained in the paragraph "+3.3V inductor". As for the +5.1V, the maximum ripple is given by:

$$\Delta I_{L5} = \eta \cdot I_{OUT12} \cdot \frac{V_{IN}}{V_{IN} - 5.1} + \frac{3}{4} \cdot \frac{5.1 \cdot (V_{IN} - 5.1)}{f_{SW} \cdot L_{3P} \cdot V_{IN}}$$

where V_{IN} is V_{INMIN} or V_{INMAX}, as selected in the "+5.1 transformer" section.

Anyhow, the maximum ESR will be:

$$ESR_X \leq \frac{V_{RPKX}}{\Delta I_{LX}}$$

where the subscript x refers to either section.

In pulse-skipping operation, the capacitive component of the output ripple is comparable to the resistive one,

thus both should be considered:

$$V_{RPPX}^{(R)} = 0.011 \cdot \frac{ESR_X}{R_{SENSEX}}$$

$$V_{RPPX}^{(R)} = 3.1 \cdot 10^{-6} \cdot \frac{L_X}{C_{OUTX}} \cdot \frac{1}{R_{SENSEX}^2} \cdot \left(\frac{1}{V_{INMIN} - V_{OUT}} - \frac{1}{V_{OUT}} \right)$$

If specification on the output ripple under pulse-skipping condition is also given, C_{OUTX} and ESR_X must comply with it as well.
Further constraints on the minimum output capacitance can arise from specifications regarding the maximum undershoot, ΔV^-_{OUT}, or overshoot, ΔV^+_{OUT}, due to a step-load change ΔI_{OUT}:

$$C_{OUT} > \frac{L \cdot \Delta I_{OUT}^2}{\Delta V_{OUT}^- \cdot (V_{INMIN} \cdot D_{MAX} - V_{OUT})} \qquad C_{OUT} > \frac{L \cdot \Delta I_{OUT}^2}{\Delta V_{OUT}^+ \cdot V_{OUT}}$$

whichever is greater, and where Dmax is the maximum duty cycle and the quantities are relevant either to the +3.3V or +5.1V section. High performance capacitors should be employed to reduce the capacitance needed for a given ESR, to avoid paralleling several parts with a considerable waste of space. Although excellent electrolytic capacitors are available, OS-CON or tantalums may be preferred especially if very compact design is required, or in case of surface mount assemblies. Multilayer ceramic capacitors with extremely low ESR are now available, but they have a large spread of the capacitance value, so they should be paralleled with another more stable, high-ESR capacitor.

Miscellaneous Components

The feedback loop has virtually unlimited bandwidth, thus a filter is necessary to make the system insensitive to the switching frequency ripple and, in general, to prevent noise from disturbing the correct operation of the error summing comparator. Anyway, the cut-off frequency of this filter can be very high, so that line and load transient response is extremely fast. This filter is a simple R-C type where resistance and capacitance can be chosen for a typical 3dB cut-off frequency of 60kHz.
As to the bootstrap diodes, even though small signal diodes might be effectively used, it is preferable to employ low-power Schottky rectifiers, since that increase slightly the gate drive voltage, in favour of efficiency. The bootstrap capacitor can be a 100nF film capacitor.
The soft-start capacitors determine the time during which the current limitation circuit moves gradually the set-point from zero up to 50mV in order to limit the current inflow at start-up. This ramp lasts approximately 1 ms per nF of soft-start capacitance (10 to 100 nF typical values), but the actual time necessary to the output voltage to reach the steady-state value depends on the load current and the output filter capacitance.
There are some critical points of the IC that may require by-pass capacitors to prevent noise from disturbing the circuit. These points are the reference voltage VREF, the IC supply pin VIN, the PREG5 line and the alternative supply pin V5SW. Use film capacitors suitable for AC decoupling.

External PNP bipolar transistor

As the output of the auxiliary winding on the 5.1V section is dimensioned for 13V, considering an output voltage of 12V the power loss across the external PNP transistor is of:

$$P_{LOSS} = (V_{IN} - V_{OUT}) \cdot I_{OUT}$$

The collector-emitter breakdown voltage must be greater than the one delivered by the transformer on the 5.1V section and this is true also for the collector-base junction. A small signal trnsistor is enough for the considered application.

Transformer Catch Diode (L5994A only)

The diode which steers the current generated by the secondary winding of the +5.1V transformer should be a fast-recovery one, with a breakdown voltage greater than:

$$V_{RR} = (V_{INLIN} - 5.1) + \eta \cdot (V_{INMAX} - 5.1)$$

with a certain safety margin. The diode has to withstand a pulsed current whose peak value is approximately:

$$I_{13PK} - I_{OUT12} \cdot \frac{V_{INMIN}}{V_{INMIN} - 5.1}$$

while its RMS value is given by:

$$I_{13RMS} = I_{OUT12} \cdot \sqrt{\frac{V_{INMIN}}{V_{INMIN} - 5.1}}$$

The DC value is obviously I_{OUT12}.

Transformer Filter Capacitors

The most stringent requirement on the input filter capacitor (connected between V13IN and ground) is its RMS ripple current rating, which should be at least:

$$I_{13AC} = I_{OUT12} \cdot \sqrt{\frac{5.1}{V_{INMIN} - 5.1}}$$

The working voltage should be higher than the voltage generated when the regulator is lightly loaded. Also for this part the use of high quality electrolytic or OS-CON capacitors is advised.

Layout and Grounding

The electrical design is only the first step in the development of a switching converter. Since currents ranging from mA to some A, both DC and switched, live together on the same circuitboard, the PCB layout is vital for a correct operation of the circuit but is not an easy task.
A proper layout process generally includes careful component placing, proper grounding, correct traces routing, and appropriate trace widths. Fortunately, since low voltages are involved in this kind of applications, isolation requirements are of no concern.
Referring to literature for a detailed analysis of this matter, only few important points will be here reminded.

1) All current returns (signal ground, power ground, etc.) should be mutually isolated and should be connected only at a single ground point. Ground planes may be extremely useful both to arrange properly current returns and to minimize radiation (see next 2 points), even though they cannot solve every problem
2) Noise coupling between adjacent circuitry can be reduced minimizing the area of the loop where current flows. This is particularly important where there are high pulsed currents, that is the circuit including the input filter capacitor, the power switch, the synchronous rectifier and the output capacitor. The next priority should be given to the gate drive circuits.
3) Magnetic field radiation (and stray inductance) can be reduced by keeping all traces which carry switched currents as short as possible.
4) The Kelvin-connected traces of current sense should be kept short and close together.
5) For high current paths, the traces could be doubled on the other side of the PCB whenever possible: this will reduce both the resistance and the inductance of the wiring.
6) In general, traces carrying signal currents should run far from traces carrying pulsed currents or with quickly swinging voltages. From this viewpoint, particular care should be taken of the high impedance paths (feedback input, current sense traces...). It could be a good idea to route signal traces on one PCB

side and power traces on the other side.

7) Use heavy copper traces: this will reduce their resistance, increasing overall efficiency and will improve their heat-sinking ability.

L5994 Evaluation Kit

The L5994 Evaluation kit is a fully assembled and tested demonstration board that implements a standard application circuit, configured according to the following specifications:

Input Voltage Range: 5V to 25V;

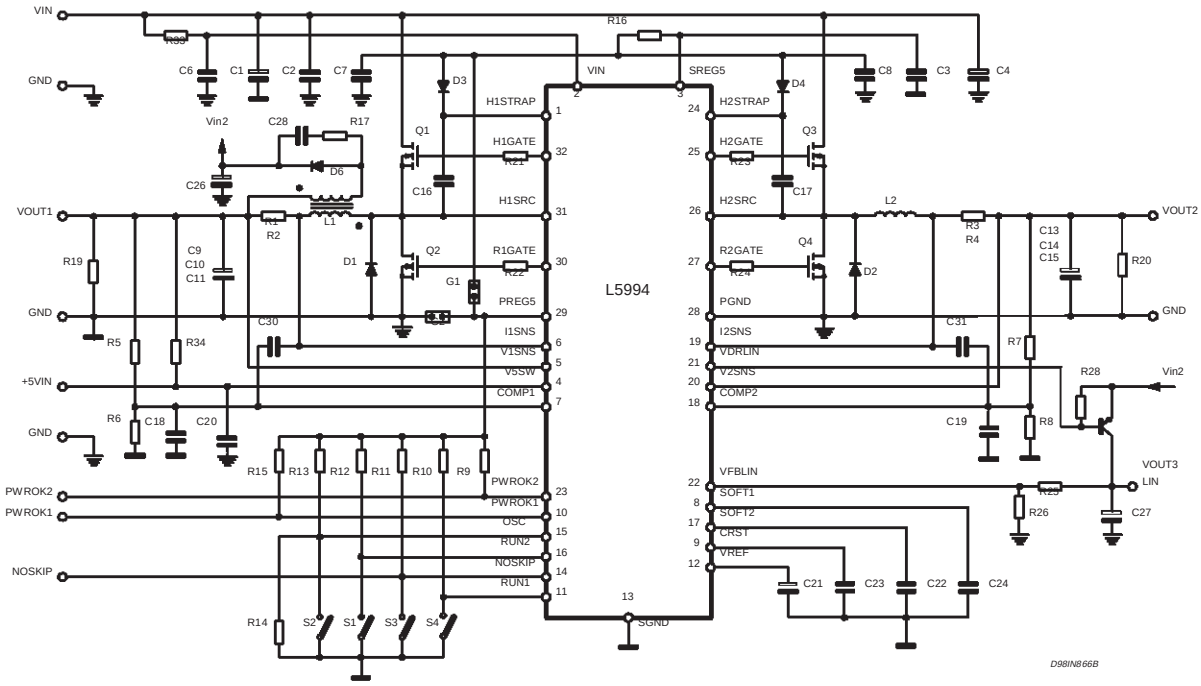
3.3V Output: Iout3 = 3A;

5.1V Output: Iout5 = 3A;

12V Output: Iout12 = 50mA;

Switching frequency: f_{SW} = 300kHz.

Figure 7. L5994 Evaluation kit



The electrical schematic, illustrated in fig. 7, shows that some pull-up/down resistor are added to the components strictly needed in a real application. Along with a quad dip-switch, they allow to set manually the logic signals that control the chip operation. These signals are in the present case:

- Switch 1: RUN1 (0= 5.1V OFF, 1= 5.1V ON)
- Switch 2: OSC (0= 200kHz, 1=300kHz)
- Switch 3: NOSKIP (0= pulse-skipping ON, 1= pulse-skipping OFF)
- Switch 4: RUN2 (0= 3.3V OFF, 1= 3.3V ON)

Please note that as long as each regulator is disabled, the relevant low-side MOSFET is in ON state. Hence, if the load is capable of sourcing current, it will be short-circuited to ground through the choke and the low-side MOS.

Although the default switching frequency is 300kHz (switch 2 set on 1) and the passive components have been selected for this frequency, the demo board will work satisfactorily at 200kHz as well. Actually, at 200kHz the regulators exhibit the maximum efficiency and the maximum extension of the input voltage range downwards. On the other hand, the output ripple is greater and the dynamic behaviour slightly worse.

The demonstration board, as it is, does not provide an interface for synchronization. Anyway, it is possible to synchronize the oscillator (with an appropriate signal: 5V amplitude pulses, spaced out by 400ns min.), provided the switch is set on 1, simply by feeding the signal into the middle of the divider R8-R9. In this way, synchronization can be achieved at a frequency higher than 300kHz. To synchronize the oscillator to a frequency between 200kHz and 300kHz, heavier interventions on the board are needed.

Pulse-skipping operation is enabled by default in order to maximize efficiency also in low load current range. The transition between PWM and pulse-skipping occurs approximately below 1A, however there is a region in which the two operation modes coexist rather than a definite boundary. That can be seen on the scope as an irregularity of the waveforms but does not have much influence both on output ripple and efficiency.

Those who do not appreciate asynchronous operation of the pulse-skipping mode can disable it for both regulators, by setting switch 3 on 1. That maintains PWM operation up to very low output currents where, however, the regulation becomes incompatible with the switching frequency. This means that the minimum ON-time of the high-side MOSFET is too long for the thruput energy level at the operating frequency. Thus the control system begins skipping conduction cycles to avoid the output voltage drifting upwards.

Component list

Table shows the complete L5994/ L5994A Evaluation Kit parts list. Critical components characteristics are given in detail.

Resistors	R1,R2,R3,R4	0.02	1W - 1% DALE WSL-2512	SMD - 2512
	R5	5.6k	0.1W - 1%	SMD - 0603
	R6	3.3k	0.1W - 1%	SMD - 0603
	R7,R8	3.9k	0.1W - 1%	SMD - 0603
	R9,R15	47k	0.1W	SMD - 0603
	R10,R11,R12,R13,R14	1M	0.1W	SMD - 0603
	R16	4.7	1/4W	SMD - 1206
	R17,R18,R19,R20	N.C.	0.1W	SMD - 0603
	R21,R22,R23,R24	2	1/4W	SMD - 0603
	R25	8.2K	1/4W	SMD - 0603
	R26	2.2K	1/4W	SMD – 0603
	R27	0	1/4W	SMD – 0603
	R28	1K	1/4W	SMD - 0603
	R33,R34	4.7	1/4W	SMD - 1206
Capacitors	C1,C4	47µ	SANYO - OS-CON 25V - 25SC47M	Radial 10 - 5
	C2,C6	1µ	Ceramic 25V	SMD - 1206
	C3,C7,C8,C20	1µ	Ceramic	SMD - 1206
	C9,C15	N.C.		TANTD
	C10,C11,C13,C14	330µ	KEMET 10V - T510	TANTD
	C16,C17,C23	100n	Ceramic	SMD - 0603
	C18,C19	22n	Ceramic	SMD - 0603
	C21,C27	4.7µ	Tantalium 16V	SMD - 3528
	C22,C24	100n	Ceramic	SMD - 0603
	C25	N.C.		Radial 8 - 2.5
	C26 (L5994A only)	15µ	SANYO - OS-CON 25V - 25SC15M	Radial 8 - 2.5
	C28,C29	N.C.	Ceramic	SMD - 0603
	C30,C31	47n	Ceramic	SMD - 0603
Magnetics	T1	10µ	Transpower Technologies TTI5870	
			(only for L5994A)	
	L1	10µ	SUMIDA CDR125-100 (only for L5994)	
	L2	10µ	SUMIDA CDR125-100	
Transistors	Q1,Q2	SI4410		SO8
	Q3,Q4	SI4410		SO8
	Q5	BC807		SOT23
Diodes	D1,D2	STPS340S		SMC
	D3,D4	BAR18		SOT23
	D5	N.C.		SMA
	D6 (L5994A only)	STPR120A		SMA
IC	U1	L5994/ L5994A		TQFP32
Jumper	G1	SHORTED		
	G2,G3,G4	OPEN		

Figure 8. PCB and component layout

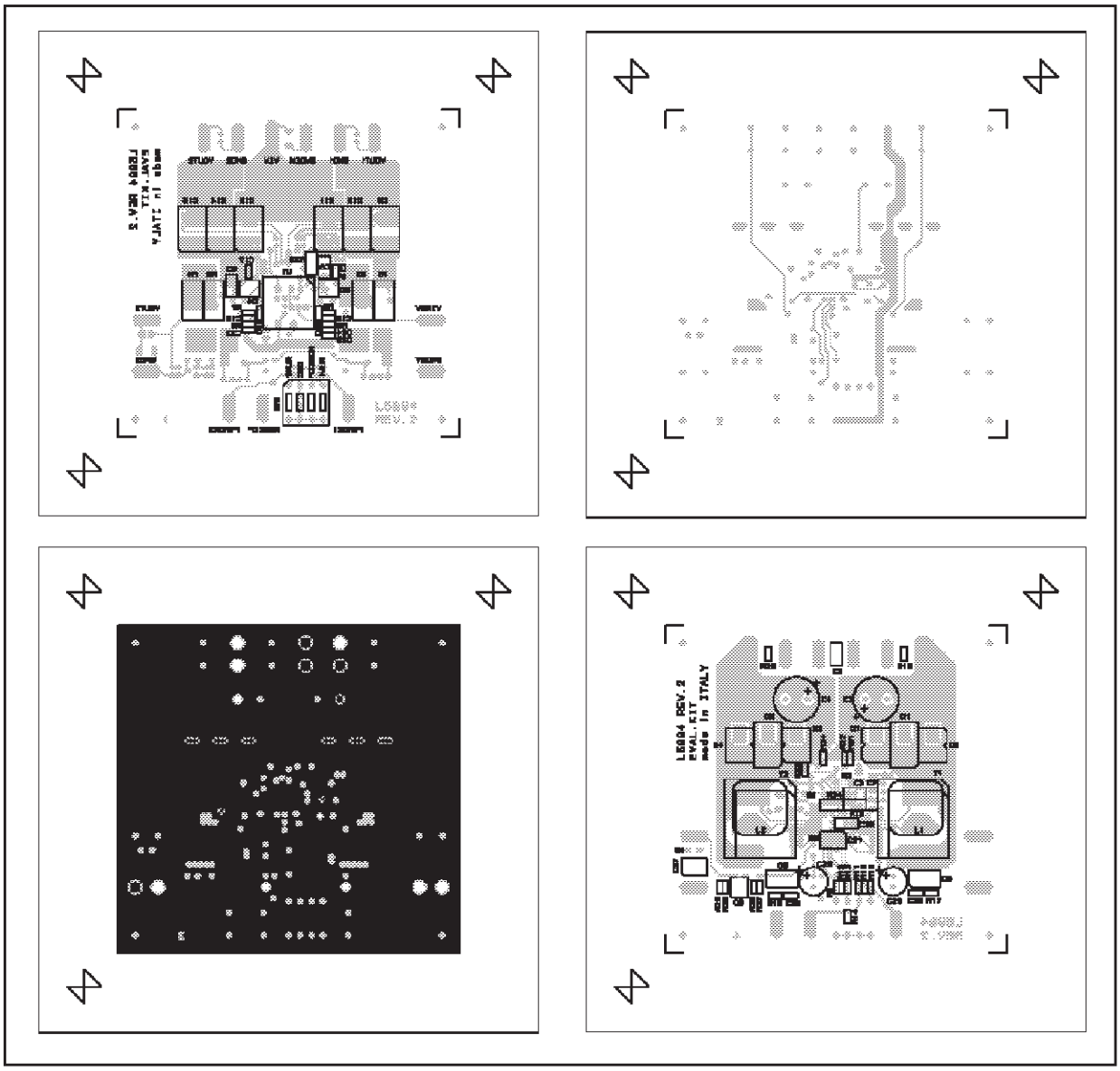


Figure 9. Demo Board Efficiency vs Output Current

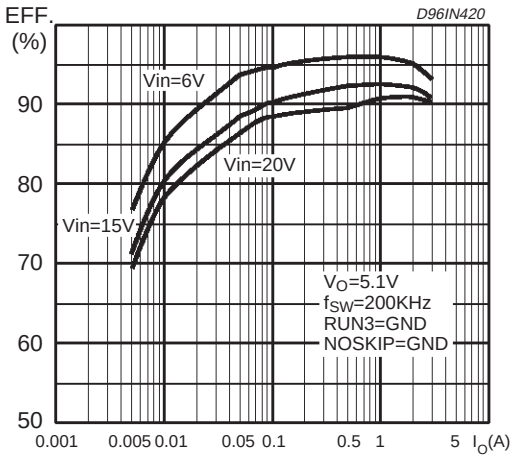


Figure 10. Demo Board Efficiency vs Output Current

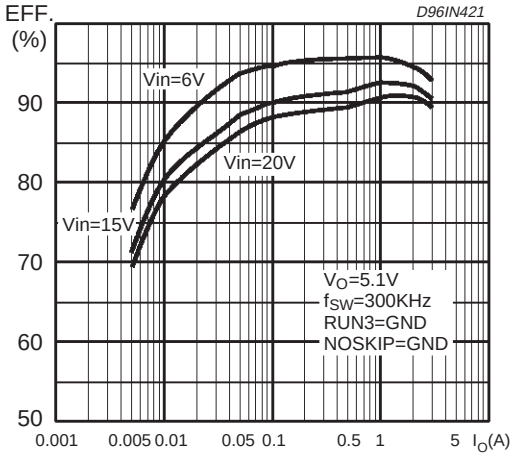


Figure 11. Demo Board Efficiency vs Output Current

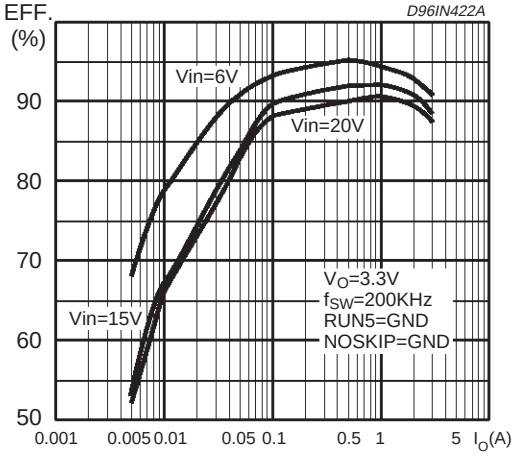


Figure 12. Demo Board Efficiency vs Output Current

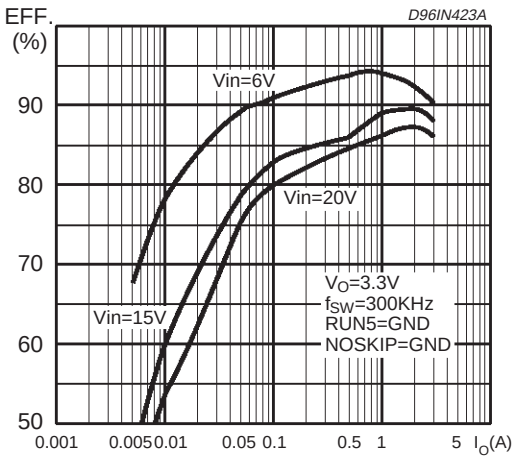


Figure 13. Demo Board Overall Efficiency (Iout3 = 3A, REG12 = OPEN, OSC = GND)

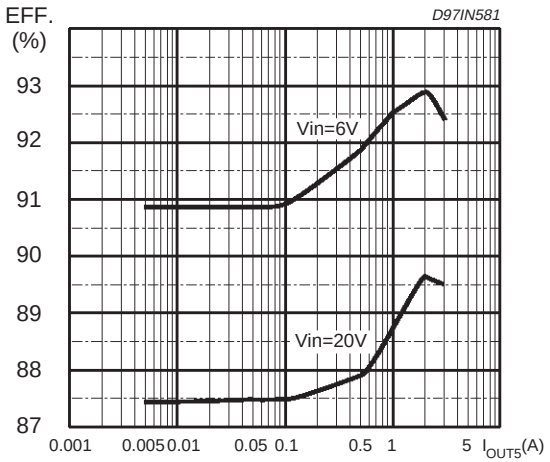
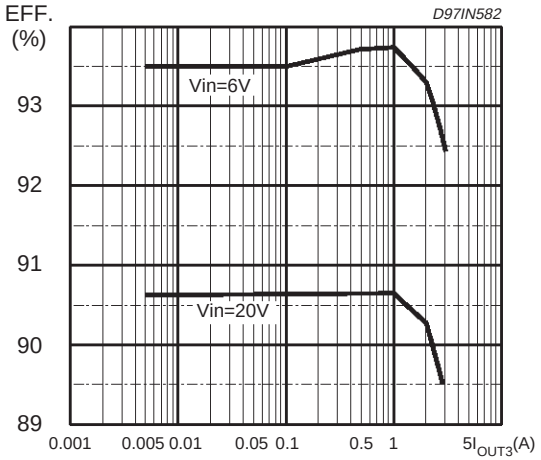
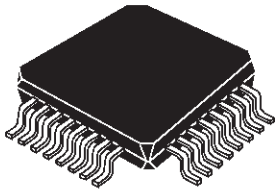


Figure 14. Demo Board Overall Efficiency (Iout5 = 3A, REG12 = OPEN, OSC = GND)



DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.30	0.37	0.45	0.012	0.015	0.018
C	0.09		0.20	0.004		0.008
D		9.00			0.354	
D1		7.00			0.276	
D3		5.60			0.220	
e		0.80			0.031	
E		9.00			0.354	
E1		7.00			0.276	
E3		5.60			0.220	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
K	0°(min.), 7°(max.)					

OUTLINE AND MECHANICAL DATA



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