QRR9901
QUALITY & RELIABILITY REPORT

April 1998 to March 1999 - EPROM, Flash Memory, EEPROM and NVRAM Products

INTRODUCTION

STMicroelectronics manufactures a wide range of memory types which include:

Non-volatile memories: Flash memory, UV EPROM, OTP EPROM and EEPROMs. EPROM products are manufactured in both 1.5µm NMOS and 0.8µm to 0.6µm CMOS technology; Flash memories in 0.8µm to 0.35µm CMOS technology; OTP EPROMs in 0.8µm to 0.6µm and EEPROMs in 1.2µm to 0.6µm CMOS technology.

Packages for non-volatile memories include both ceramic FDIP and plastic PDIP, PLCC, SO and TSOP.

Non-volatile RAM: ZEROPOWER and TIMEKEEPER ranges are manufactured in 1.2-0.7µm HCMOS technology.

Packages for ZEROPOWER and TIMEKEEPER products use a modified PDIP or SO with an additional "top hat" assembly mounted above and containing a Lithium battery and optionally a quartz crystal. The battery and crystal are sealed in the plastic cap with a plastic resin.

The results presented in this quarterly report cover the tests made from April 1998 to March 1999. Regular reports are issued each quarter with the last years cumulative results.

Director of
Memory Products Group
Quality Control & Reliability

Attilio PANCHIERI

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Table 1. Final Average Outgoing Quality (AOQ)
April 1998 to March 1999

Process	Electrical ppm				Visual ppm			
	2Q98	3Q98	4Q98	1Q99	2Q98	3Q98	4Q98	1Q99
UV EPROM								
CMOS	18	7	4	6	19	12	9	8
NMOS	20	0	0	0	20	20	0	0
OTP EPROM								
CMOS	20	19	14	20	8	6	5	13
FLASH								
CMOS	3	9	8	3	6	5	12	12
NVRAM								
CMOS	0	0	0	0	3	0	0	5
EEPROM								
CMOS	4	7	3	2	8	2	7	11

Table 2. Failure Rate Predictions (Fit)
April 1998 to March 1999

Process	Actual Device hrs		Temperature Activation Energy (eV)	Voltage Acceleration Factor	Equivalent hrs 55 °C (x 10^6)	Life Test Failure	Failure Rate (Fit) Confidence Level	
	Dev. hrs (x 10^6)	Temp. (°C)					60%	90%
UV EPROM								
CMOS E5 -35%	1.439	140	0.6	4.0	373	0	2.4	6.2
CMOS E6 - DM	1.178	140	0.6	4.0	1,178	0	2.9	7.5
CMOS E6 -10%	4.421	140	0.6	4.0	1,146	0	0.8	2.0
OTP EPROM								
CMOS E5 -35%	2.270	140	0.6	4.0	588	0	1.5	3.9
CMOS E6 -10%	1.760	140	0.6	4.0	456	0	2.00	5.00
FLASH								
CMOS T5 -20%	2.004	140	0.6	4.0	519	0	1.8	4.4
CMOS T6	22.333	140	0.6	4.6	6,657	0	0.13	0.35
CMOS T6X -35%	2.651	140	0.6	4.6	790	0	1.16	2.91
EEPROM								
CMOS F4S	2.869	140	0.6	3.0	674	0	1.3	3.4
CMOS F6SP	2.433	140	0.6	4.6	877	0	1.1	2.6
NVRAM								
HCMOS S3	1.679	100	0.7	64	2,149	1	0.9	1.8
HCMOS 4DZ	1.844	125	0.7	6.0	851	1	2.4	4.6

Table 3. NMOS E3/1.5µm Process UV EPROM Reliability Data, Die Related Tests
April 1998 to March 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M2764A		M27256	
			Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,				
		– 48 hrs	585	0	-	-
		– 168 hrs	460	0	-	-
		– 500 hrs	460	0	-	-
		– 1000 hrs	460	0	-	-
Retention Bake	1008	250°C,				
		– 48 hrs	850	0	-	-
		– 168 hrs	850	0	-	-
		– 500 hrs	770	0	-	-

Table 4. CMOS E5/0.8µm Process UV EPROM Reliability Data, Die Related Tests
April 1998 to March 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C64A	
			Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz, – 48 hrs – 168 hrs – 500 hrs – 1000 hrs	 154 80 80 80	 0 0 0 0
Retention Bake	1008	250°C, – 48 hrs – 168 hrs – 500 hrs	 - - -	 - - -

Table 5A. CMOS E5/0.6µm Process (–35% upgrade) UV EPROM Reliability Data, Die Related Tests
April 1998 to March 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C256 (D) M87C257 (D)		M27C512 (D)	
			Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,				
		– 48 hrs	3,917	0	4,095	0
		– 168 hrs	320	0	630	0
		– 500 hrs	320	0	550	0
		– 1000 hrs	320	0	550	0
Retention Bake	1008	250°C,				
		– 48 hrs	470	0	630	0
		– 168 hrs	470	0	630	0
		– 500 hrs	470	0	550	0
		– 1000 hrs	-	-	-	-

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 5B. CMOS E5/0.6µm Process (–35% upgrade) UV EPROM Reliability Data, Die Related Tests
April 1998 to March 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C801 (D)	
			Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,		
		– 48 hrs	2,929	0
		– 168 hrs	80	0
		– 500 hrs	80	0
		– 1000 hrs	80	0
Retention Bake	1008	250°C,		
		– 48 hrs	80	0
		– 168 hrs	80	0
		– 500 hrs	80	0
		– 1000 hrs	-	-

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 6. CMOS E6/0.6µm Process (–10% upgrade) UV EPROM Reliability Data, Die Related Tests
April 1998 to March 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C1001 (F)		M27C1024 (F)		M27C2001 (F)		M27C4001 (F)		M27C4002 (F)		M27C801 (F)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,												
		– 48 hrs	1,993	0	537	0	2,097	0	2,251	0	710	0	18,125	0
		– 168 hrs	530	0	460	0	550	0	550	0	710	0	870	0
		– 500 hrs	450	0	460	0	550	0	470	0	630	0	790	0
		– 1000 hrs	450	0	460	0	550	0	470	0	630	0	710	0
Retention Bake	1008	250°C,												
		– 48 hrs	530	0	460	0	550	0	550	0	710	0	870	0
		– 168 hrs	530	0	460	0	550	0	550	0	710	0	870	0
		– 500 hrs	450	0	460	0	550	0	470	0	630	0	790	0

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 7. CMOS E6DM/0.6µm Process UV EPROM Reliability Data, Die Related Tests
April 1998 to March 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C4001 (F)		M27C800 (F)		M27C160 (F)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,						
		– 48 hrs	80	0	4,341	0	9,416	0
		– 168 hrs	80	0	160	0	300	0
		– 500 hrs	80	0	160	0	300	0
		– 1000 hrs	80	0	160	0	300	0
Retention Bake	1008	250°C,						
		– 48 hrs	80	0	160	0	300	0
		– 168 hrs	80	0	160	0	300	0
		– 500 hrs	80	0	160	0	300	0
		– 1000 hrs	-	-	-	-	-	-

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 8. UV EPROM Reliability Data, Package Related Tests (Ceramic Frit-Seal)
April 1998 to March 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	Samp.	Fail
Temperature Cycling	1010	–65 to 150°C, – 100 cycles – 500 cycles – 1000 cycles	 3,695 3,645 3,265	 0 0 0
– Fine Leak – Gross Leak	1014 1014	Test Condition A1 Test Condition C1		
Solderability	2003	245°C, 5sec, Precondition Steam, 1hr	1,110	0
Resistance to Solvents	2015	4 Solvent Solutions	244	0
Lead Integrity	2004	Test Condition B2 (lead fatigue)	180	0
– Fine Leak – Gross Leak	1014 1014	Test Condition A1 Test Condition C1		

Table 9A. CMOS E5/0.6µm Process (–35% upgrade) OTP EPROM Reliability Data, Die Related Tests
April 1998 to March 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C256 (D) M87C257 (D)		M27C512 (D)		M27C516 (D)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,						
		– 168 hrs	450	0	870	0	480	0
		– 500 hrs	390	0	750	0	480	0
		– 1000 hrs	390	0	690	0	480	0
Retention Bake	1008	150°C,						
		– 168 hrs	450	0	870	0	480	0
		– 500 hrs	390	0	750	0	480	0
		– 1000 hrs	390	0	690	0	480	0

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 9B. CMOS E5/0.6µm Process (–35% upgrade) OTP EPROM Reliability Data, Die Related Tests
April 1998 to March 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C1001 (D)		M27C1024 (D)		M27C2001 (D)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,						
		– 168 hrs	180	0	180	0	290	0
		– 500 hrs	180	0	180	0	290	0
		– 1000 hrs	180	0	180	0	290	0
Retention Bake	1008	150°C,						
		– 168 hrs	180	0	180	0	290	0
		– 500 hrs	180	0	180	0	290	0
		– 1000 hrs	180	0	180	0	290	0

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 10A. CMOS E5/0.6µm Process (–35% upgrade) OTP EPROM Reliability Data, Package Related Tests
April 1998 to March 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C256 (D) M87C257 (D)		M27C512 (D)		M27C516 (D)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs	 450 390 390	 0 0 0	 870 750 690	 0 0 0	 480 480 480	 0 0 0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V, – 48 hrs – 96 hrs – 168 hrs – 240 hrs	 190 190 135 65	 0 0 0 0	 360 360 335 65	 0 0 0 0	 200 200 175 75	 0 0 0 0
Pressure Pot		121°C, 2Atm, – 48 hrs – 96 hrs – 168 hrs – 240 hrs	 390 390 390 390	 0 0 0 0	 750 750 750 750	 0 0 0 0	 480 480 480 480	 0 0 0 0
Temperature Cycling	1010	–65 to 150°C, – 100 cycles – 500 cycles – 1000 cycles	 337 337 277	 0 0 0	 640 640 640	 0 0 0	 480 480 480	 0 0 0
Solderability								
– PLCC/TSOP Packages	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	(See cumulative data on Table 10B)					
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	(See cumulative data on Table 10B)					
Resistance to solvents	2015	4 Solvent Solutions	(See cumulative data on Table 10B)					

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 10B. CMOS E5/0.6µm Process (–35% upgrade) OTP EPROM Reliability Data, Package Related Tests
April 1998 to March 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C1001 (D)		M27C1024 (D)		M27C2001 (D)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,						
		– 168 hrs	180	0	180	0	290	0
		– 500 hrs	180	0	180	0	290	0
		– 1000 hrs	180	0	180	0	290	0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,						
		– 48 hrs	80	0	75	0	120	0
		– 96 hrs	80	0	75	0	120	0
		– 168 hrs	50	0	75	0	95	0
		– 240 hrs	25	0	25	0	70	0
Pressure Pot		121°C, 2Atm,						
		– 48 hrs	240	0	180	0	290	0
		– 96 hrs	240	0	180	0	290	0
		– 168 hrs	240	0	180	0	290	0
		– 240 hrs	240	0	180	0	290	0
Temperature Cycling	1010	–65 to 150°C,						
		– 100 cycles	180	0	180	0	290	0
		– 500 cycles	180	0	180	0	290	0
		– 1000 cycles	180	0	180	0	290	0
Solderability								
– PLCC/TSOP Packages	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	Cumulative Sample/Fail = 765/0					
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	Cumulative Sample/Fail = 95/0					
Resistance to solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 280/0					

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 11. CMOS E6/0.6µm Process (–10% upgrade) OTP EPROM Reliability Data, Die Related Tests
April 1998 to March 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C1001 (F)		M27C1024 (F)		M27C2001 (F)		M27C4001 (F)		M27C4002 (F)		M27C801 (F)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,												
		– 168 hrs	1,110	0	330	0	50	0	290	0	340	0	60	0
		– 500 hrs	990	0	330	0	50	0	170	0	280	0	-	-
		– 1000 hrs	930	0	270	0	50	0	110	0	220	0	-	-
Retention Bake	1008	150°C,												
		– 168 hrs	1,110	0	330	0	50	0	290	0	340	0	60	0
		– 500 hrs	990	0	330	0	50	0	170	0	280	0	-	-
		– 1000 hrs	930	0	270	0	50	0	110	0	220	0	-	-

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 12A. CMOS E6/0.6µm Process (–10% upgrade) OTP EPROM Reliability Data, Package Related Tests
April 1998 to March 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C1001 (F)		M27C1024 (F)		M27C2001 (F)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,						
		– 168 hrs	1,110	0	330	0	50	0
		– 500 hrs	990	0	330	0	50	0
		– 1000 hrs	930	0	270	0	50	0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,						
		– 48 hrs	460	0	135	0	20	0
		– 96 hrs	460	0	135	0	20	0
		– 168 hrs	395	0	135	0	20	0
		– 240 hrs	70	0	40	-	-	-
Pressure Pot		121°C, 2Atm,						
		– 48 hrs	990	0	330	0	50	0
		– 96 hrs	990	0	330	0	50	0
		– 168 hrs	990	0	330	0	50	0
		– 240 hrs	980	0	330	0	50	0
Temperature Cycling	1010	–65 to 150°C,						
		– 100 cycles	1,046	0	330	0	50	0
		– 500 cycles	1,046	0	330	0	50	0
		– 1000 cycles	946	0	270	0	50	0
Solderability								
– PLCC Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	(See cumulative data on Table 12B)					
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs						
Resistance to solvents	2015	4 Solvent Solutions	(See cumulative data on Table 12B)					

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 12B. CMOS E6/0.6µm Process (–10% upgrade) OTP EPROM Reliability Data, Package Related Tests
April 1998 to March 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C4001 (F)		M27C4002 (F)		M27C801 (F)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,						
		– 168 hrs	290	0	340	0	60	0
		– 500 hrs	170	0	280	0	-	-
		– 1000 hrs	110	0	220	0	-	-
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,						
		– 48 hrs	120	0	140	0	25	0
		– 96 hrs	120	0	140	0	-	-
		– 168 hrs	95	0	115	0	-	-
		– 240 hrs	-	-	65	0	-	-
Pressure Pot		121°C, 2Atm,						
		– 48 hrs	170	0	280	0	60	0
		– 96 hrs	170	0	280	0	-	-
		– 168 hrs	170	0	280	0	-	-
		– 240 hrs	170	0	280	0	-	-
Temperature Cycling	1010	–65 to 150°C,						
		– 100 cycles	230	0	340	0	60	0
		– 500 cycles	170	0	280	0	-	-
		– 1000 cycles	170	0	280	0	-	-
Solderability								
– PLCC Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	Cumulative Sample/Fail = 256/0					
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs						
Resistance to solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 64/0					

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 13. CMOS E6DM/0.6µm Process OTP EPROM Reliability Data, Die Related Tests
April 1998 to March 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C4001 (F)		M27C800 (F)		M27C160 (F)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz, – 168 hrs – 500 hrs – 1000 hrs	 120 120 120	 0 0 0	 60 60 60	 0 0 0	 120 120 120	 0 0 0
Retention Bake	1008	150°C, – 168 hrs – 500 hrs – 1000 hrs	 120 120 120	 0 0 0	 60 60 60	 0 0 0	 120 120 120	 0 0 0

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 14. CMOS E6DM/0.6µm Process OTP EPROM Reliability Data, Package Related Tests
April 1998 to March 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C4001 (F)		M27C800 (F)		M27C160 (F)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs	 120 120 120	 0 0 0	 60 60 60	 0 0 0	 120 120 120	 0 0 0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V, – 48 hrs – 96 hrs – 168 hrs – 240 hrs	 50 50 50 25	 0 0 0 0	 25 25 25 -	 0 0 0 -	 50 50 50 50	 0 0 0 0
Pressure Pot		121°C, 2Atm, – 48 hrs – 96 hrs – 168 hrs – 240 hrs	 120 120 120 120	 0 0 0 0	 60 60 60 60	 0 0 0 0	 120 120 120 120	 0 0 0 0
Temperature Cycling	1010	–65 to 150°C, – 100 cycles – 500 cycles – 1000 cycles	 120 120 120	 0 0 0	 60 60 60	 0 0 0	 120 120 120	 0 0 0
Solderability – PLCC/TSOP Packages	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	Cumulative Sample/Fail = 100/0					
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	Cumulative Sample/Fail = 40/0					
Resistance to solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 44/0					

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 15. CMOS T5/0.8µm Process (–20% upgrade) Flash Memory Reliability Data, Die Related Tests
April 1998 to March 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F256 (B)		M28F512 (B)		M28F101 (B)		M28F102 (B)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test (1)	1005	140°C, V_{CC} = 6V,f = 500kHz,								
		– 24 hrs	120	0	1,297	0	3,003	0	4,072	0
		– 168 hrs	120	0	1,140	0	985	0	905	0
		– 500 hrs	120	0	580	0	580	0	410	0
		– 1000 hrs	120	0	520	0	520	0	410	0
Retention Bake (1)	1008	150°C,								
		– 168 hrs	120	0	640	0	490	0	530	0
		– 500 hrs	120	0	580	0	430	0	410	0
		– 1000 hrs	60	0	520	0	430	0	410	0
Retention Bake	1008	250°C,								
		– 168 hrs	-	-	-	-	376	0	60	0
		– 500 hrs	-	-	-	-	376	0	60	0
		– 1000 hrs	-	-	-	-	376	0	-	-
Write/Erase Cycling		1,000 cycles	448	0	4,694	0	5,976	0	8,704	0
		10,000 cycles	-	-	-	-	733	0	-	-
Retention Bake	1008	150°C, 36 hrs	448	0	4,694	0	5,243	0	8,704	0

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.
1. A quarter of sample size was subjected to 10,000 Write/Erase cycles before operating life test and retention bake.

Table 16. CMOS T5/0.8µm Process (–20% upgrade) Flash Memory Reliability Data, Package Related Tests
April 1998 to March 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F256 (B)		M28F512 (B)		M28F101 (B)		M28F102 (B)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,								
		– 168 hrs	120	0	640	0	640	0	530	0
		– 500 hrs	120	0	580	0	580	0	410	0
		– 1000 hrs	120	0	520	0	580	0	410	0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,								
		– 48 hrs	60	0	265	0	280	0	225	0
		– 96 hrs	60	0	265	0	280	0	225	0
		– 168 hrs	60	0	240	0	280	0	225	0
		– 240 hrs	-	-	240	0	165	0	170	0
Pressure Pot		121°C, 2Atm,								
		– 48 hrs	120	0	580	0	580	0	470	0
		– 96 hrs	120	0	580	0	580	0	470	0
		– 168 hrs	120	0	420	0	580	0	410	0
		– 240 hrs	120	0	420	0	580	0	410	0
Temperature Cycling	1010	–65 to 150°C,								
		– 100 cycles	60	0	580	0	550	0	470	0
		– 500 cycles	60	0	580	0	550	0	410	0
		– 1000 cycles	60	0	520	0	490	0	410	0
Thermal Shock	1011	–55 to 125°C,								
		– 100 cycles	-	-	-	-	-	-	-	-
		– 500 cycles	-	-	-	-	-	-	-	-
Solderability										
– TSOP/PLCC Packages	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	Cumulative Sample/Fail = 400/0							
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	Cumulative Sample/Fail = 90/0							
Resistance to solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 168/0							

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 17A. CMOS T6/0.55µm Process Flash Memory Reliability Data, Die Related Tests
April 1998 to March 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F201 (B)		M28F210 (C) M28F211 (C) M28F220 (C)		M28F411 (C) M28F410 (C) M28F420 (C)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test (1)	1005	140°C, V_{CC} = 6V,f = 500kHz,						
		– 24 hrs	13,290	0	123,681	0	10,537	0
		– 168 hrs	60	0	470	0	60	0
		– 500 hrs	60	0	470	0	60	0
		– 1000 hrs	60	0	470	0	60	0
Retention Bake (1)	1008	150°C,						
		– 168 hrs	60	0	470	0	60	0
		– 500 hrs	60	0	470	0	60	0
		– 1000 hrs	60	0	470	0	60	0
Retention Bake	1008	250°C,						
		– 168 hrs	361	0	-	-	180	0
		– 500 hrs	361	0	-	-	180	0
		– 1000 hrs	361	0	-	-	180	0
Write/Erase Cycling		1,000 cycles	1,408	0	13,147	0	1,120	0
		10,000 cycles	-	-	-	-	32	0
		100,000 cycles	-	-	-	-	-	-
		200,000 cycles	-	-	-	-	-	-
Retention Bake	1008	150°C, 36 hrs	1,408	0	13,147	0	1,088	0

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.
1. A quarter of sample size was subjected to 10,000 Write/Erase cycles before operating life test and retention bake.

Table 17B. CMOS T6/0.55µm Process Flash Memory Reliability Data, Die Related Tests
April 1998 to March 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M29F102 M29F105		M29F002		M29F200 M29F100		M29F040 (C) M29W040		M29F400 M29W400	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test (1)	1005	140°C, V_{CC} = 6V,f = 500kHz,										
		– 24 hrs	320,967	0	89,402	0	30,563	0	116,814	0	109,304	0
		– 168 hrs	690	0	350	0	110	0	920	0	530	0
		– 500 hrs	390	0	290	0	110	0	920	0	530	0
		– 1000 hrs	390	0	230	0	110	0	920	0	530	0
Retention Bake (1)	1008	150°C,										
		– 168 hrs	690	0	350	0	110	0	625	0	530	0
		– 500 hrs	390	0	290	0	110	0	625	0	470	0
		– 1000 hrs	390	0	230	0	110	0	625	0	470	0
Retention Bake	1008	250°C,										
		– 168 hrs	120	0	126	0	51	0	617	0	162	0
		– 500 hrs	120	0	126	0	51	0	617	0	162	0
		– 1000 hrs	120	0	66	0	51	0	617	0	162	0
Write/Erase Cycling		1,000 cycles	35,986	0	11,239	0	3,200	0	13,467	0	11,999	0
		10,000 cycles	831	0	64	0	-	-	864	0	735	0
		100,000 cycles	63	0	64	0	-	-	542	0	351	0
		200,000 cycles	-	-	-	-	-	-	63	0	60	0
		1,000,000 cycles	-	-	-	-	-	-	-	-	60	0
Retention Bake	1008	150°C, 36 hrs	35,155	0	11,175	0	3,200	0	12,658	0	11,264	0

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.
1. A quarter of sample size was subjected to 10,000 Write/Erase cycles before operating life test and retention bake.

Table 18A. CMOS T6/0.55µm Process Flash Memory Reliability Data, Package Related Tests
April 1998 to March 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F201 (B)		M28F211 (C) M28F210 (C) M28F220 (C)		M28F411 (C) M28F410 (C) M28F420 (C)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,						
		– 168 hrs	60	0	470	0	60	0
		– 500 hrs	60	0	470	0	60	0
		– 1000 hrs	60	0	470	0	60	0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,						
		– 48 hrs	30	0	205	0	30	0
		– 96 hrs	30	0	205	0	30	0
		– 168 hrs	30	0	205	0	30	0
		– 240 hrs	-	-	120	0	-	-
Pressure Pot		121°C, 2Atm,						
		– 48 hrs	60	0	470	0	60	0
		– 96 hrs	60	0	470	0	60	0
		– 168 hrs	60	0	470	0	60	0
		– 240 hrs	60	0	470	0	60	0
Temperature Cycling	1010	–65 to 150°C,						
		– 100 cycles	-	-	470	0	60	0
		– 500 cycles	-	-	470	0	60	0
		– 1000 cycles	-	-	470	0	60	0
Thermal Shock	1011	–55 to 125°C,						
		– 100 cycles	-	-	-	-	-	-
		– 500 cycles	-	-	-	-	-	-
Solderability								
– TSOP/SO Packages	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	(See cumulative data on Table 18B)					
Resistance to solvents	2015	4 Solvent Solutions	(See cumulative data on Table 18B)					

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 18B. CMOS T6/0.55µm Process Flash Memory Reliability Data, Package Related Tests
April 1998 to March 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M29F102 M29F105		M29F002		M29F200 M29F100		M29F040 (C) M29W040		M29F400 M29W400	
			Fail	Fail	Samp.	Fail	Samp.	Samp.	Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,										
		– 168 hrs	690	0	350	0	110	0	920	0	590	0
		– 500 hrs	390	0	290	0	110	0	920	0	530	0
		– 1000 hrs	390	0	230	0	110	0	920	0	530	0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,										
		– 48 hrs	260	0	145	0	50	0	400	0	260	0
		– 96 hrs	260	0	145	0	50	0	400	0	260	0
		– 168 hrs	234	0	120	0	50	0	400	0	235	0
		– 240 hrs	209	0	120	0	20	0	255	0	-	-
Pressure Pot		121°C, 2Atm,										
		– 48 hrs	510	0	255	0	110	0	920	0	530	0
		– 96 hrs	510	0	255	0	110	0	920	0	530	0
		– 168 hrs	330	0	255	0	110	0	870	0	530	0
		– 240 hrs	330	0	255	0	110	0	870	0	530	0
Temperature Cycling	1010	–65 to 150°C,										
		– 100 cycles	510	0	290	0	110	0	920	0	530	0
		– 500 cycles	390	0	290	0	110	0	920	0	530	0
		– 1000 cycles	390	0	230	0	110	0	860	0	530	0
Thermal Shock	1011	–55 to 125°C,										
		– 100 cycles	-	-	-	-	-	-	-	-	-	-
		– 500 cycles	-	-	-	-	-	-	-	-	-	-
Solderability												
– TSOP/SO Packages	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	Cumulative Sample/Fail = 535/0									
Resistance to solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 240/0									

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 19. CMOS T6X/0.35µm Process Flash Memory Reliability Data
April 1998 to March 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28W800 M29W008	
			Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V,f = 500kHz,		
		– 24 hrs	103,390	0
		– 168 hrs	272	0
		– 500 hrs	272	0
		– 1000 hrs	136	0
Retention Bake	1008	150°C,		
		– 168 hrs	120	0
		– 500 hrs	120	0
		– 1000 hrs	60	0
Retention Bake	1008	250°C,		
		– 168 hrs	278	0
		– 500 hrs	278	0
		– 1000 hrs	278	0
Write/Erase Cycling		1,000 cycles	11,034	0
		10,000 cycles	351	0
		100,000 cycles	100	0
		200,000 cycles	-	-
Retention Bake	1008	150°C, 36 hrs	11,034	0

Table 20. CMOS T6X/0.35µm Process Flash Memory Reliability Data, Die Related Tests
April 1998 to March 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28W800 M29W008	
			Fail	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85% V_{CC} = 5V		
		– 168 hrs	120	0
		– 500 hrs	120	0
		– 1000 hrs	60	0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V		
		– 48 hrs	50	0
		– 96 hrs	50	0
		– 168 hrs	50	0
		– 240 hrs	50	0
Pressure Pot		121°C, 2Atm,		
		– 48 hrs	312	0
		– 96 hrs	312	0
		– 168 hrs	312	0
		– 240 hrs	312	0
Temperature Cycling	1010	65°C to 150°C,		
		– 100 cycles	240	0
		– 500 cycles	240	0
		– 1000 cycles	240	0

Table 21. CMOS F4/1.2µm Process EEPROM Reliability Data, Die Related Tests
April 1998 to March 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST93Cxxx	
			Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, – 24 hrs – 168 hrs – 500 hrs – 1000 hrs	 6,160 960 960 -	 0 0 0 -
Retention Bake	1008	150°C, – 168 hrs – 500 hrs – 1000 hrs	 600 600 600	 0 0 0
Write/Erase Cycling		100,000 cycles 1,000,000 cycles	2,216 545	0 0
Retention Bake	1008	150°C, 168 hrs	-	-

Table 22. CMOS F4/1.2µm Process EEPROM Reliability Data, Package Related Tests
April 1998 to March 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST93Cxxx	
			Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs	 520 520 520	 0 0 0
Pressure Pot		121°C, 2Atm, – 48 hrs – 96 hrs – 168 hrs – 240 hrs	 1,400 1,400 1,400 700	 0 0 0 0
Temperature Cycling	1010	–65 to 150°C, – 100 cycles – 200 cycles –40 to 150°C, – 500 cycles – 1000 cycles	 1,400 700 - -	 0 0 - -
Soderability – PDIP Package – SO Package	 2003 CECC 90,000	 245°C, 5sec, Precondition Steam, 8hrs 215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	 (See cumulative data on Table 26B) (See cumulative data on Table 26B)	
Resistance to solvents	2015	4 Solvent Solutions	(See cumulative data on Table 26B)	
Resistance to Surface Mount: – SO Package			(See cumulative data on Table 26B)	

Table 23A. CMOS F4S/1.0µm Process EEPROM Reliability Data, Die Related Tests
April 1998 to March 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST24C01 ST24W01		ST24C02 ST24W02		ST24C04 ST24W04		ST24C08		ST24C16 ST25C16		ST24LC21	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V,												
		– 24 hrs	960	0	43,360	0	1,520	0	480	0	1,440	0	-	-
		– 168 hrs	160	0	560	0	720	0	80	0	240	0	-	-
		– 500 hrs	160	0	560	0	720	0	80	0	240	0	-	-
		– 1000 hrs	-	-	-	-	-	-	-	-	-	-	-	-
Retention Bake	1008	150°C,												
		– 168 hrs	100	0	350	0	450	0	50	0	330	0	-	-
		– 500 hrs	100	0	350	0	450	0	50	0	330	0	-	-
		– 1000 hrs	100	0	350	0	450	0	50	0	330	0	-	-
		– 2000 hrs	-	-	-	-	-	-	-	-	-	-	-	-
Write/Erase Cycling		100,000 cycles	590	0	5,455	0	4,564	2 (a)	2,498	2 (a)	4,694	2 (a)	890	1 (a)
		1,000,000 cycles	-	-	1,980	0	2,881	3 (a)	1,067	1 (a)	1,140	0	-	-
Retention Bake	1008	150°C, 168 hrs	-	-	-	-	-	-	-	-	-	-	-	-

Note: a. Single bit fail.
Oxide quality improvements are addressed in two directions:
– Continuous quality improvement by fab task force.
– “Build in” robustness through product and process design.

Table 23B. CMOS F4S/1.0µm Process EEPROM Reliability Data, Die Related Tests
April 1998 to March 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M24C16		M93C06		M93C46		M93C56		M93C66		M28C64D M28C64	
			Samp	Fail	Samp	Fail	Samp	Fail	Samp	Fail	Samp	Fail	Samp	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V,												
		– 24 hrs	-	-	-	-	1,840	0	480	0	960	0	2,980	0
		– 168 hrs	-	-	-	-	240	0	80	0	160	0	2,980	0
		– 500 hrs	-	-	-	-	240	0	80	0	160	0	1,980	0
		– 1000 hrs	-	-	-	-	-	-	-	-	-	-	760	0
Retention Bake	1008	150°C,												
		– 168 hrs	-	-	-	-	100	0	50	0	100	0	430	0
		– 500 hrs	-	-	-	-	100	0	50	0	100	0	430	0
		– 1000 hrs	-	-	-	-	100	0	50	0	100	0	430	0
Write/Erase Cycling		50,000 cycles	-	-	362	0	2,799	0	1,576	0	1,396	0	-	-
		1,000,000 cycles	-	-	-	-	450	0	473	0	473	0	-	-
Retention Bake	1008	150°C, 168 hrs	-	-	-	-	-	-	-	-	-	-	-	-

Table 24A. CMOS F4S/1.0µm Process EEPROM Reliability Data, Package Related Tests
April 1998 to March 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST24C01 ST24W01		ST24C02 ST24W02		ST24C04 ST24W04		ST24C08	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,								
		– 168 hrs	200	0	200	0	120	0	280	0
		– 500 hrs	200	0	200	0	120	0	280	0
		– 1000 hrs	200	0	200	0	120	0	280	0
Pressure Pot		121°C, 2Atm,								
		– 48 hrs	700	0	500	0	650	0	700	0
		– 96 hrs	700	0	500	0	650	0	700	0
		– 168 hrs	700	0	500	0	650	0	700	0
		– 240 hrs	300	0	250	0	200	0	350	0
Temperature Cycling	1010	–65 to 150°C,								
		– 100 cycles	600	0	500	0	650	0	700	0
		– 200 cycles	300	0	250	0	200	0	350	0
		–40 to 150°C,								
		– 500 cycles	-	-	-	-	-	-	-	-
		– 1000 cycles	-	-	-	-	-	-	-	-
Solderability										
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	(See cumulative data on Table 26B)							
– SO Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	(See cumulative data on Table 26B)							
Resistance to solvents	2015	4 Solvent Solutions	(See cumulative data on Table 26B)							
Resistance to Surface Mount:										
– SO Package			(See cumulative data on Table 26B)							

Table 24B. CMOS F4S/1.0µm Process EEPROM Reliability Data, Package Related Tests
April 1998 to March 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST24C16 ST25C16		M24C16		M93C46	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,						
		– 168 hrs	200	0	-	-	120	0
		– 500 hrs	200	0	-	-	120	0
		– 1000 hrs	200	0	-	-	120	0
Pressure Pot		121°C, 2Atm,						
		– 48 hrs	910	0	-	-	750	0
		– 96 hrs	910	0	-	-	750	0
		– 168 hrs	910	0	-	-	750	0
		– 240 hrs	430	0	-	-	200	0
Temperature Cycling	1010	–65 to 150°C,						
		– 100 cycles	500	0	-	-	450	0
		– 200 cycles	250	0	-	-	200	0
		–40 to 150°C,						
		– 500 cycles	-	-	-	-	-	-
		– 1000 cycles	-	-	-	-	-	-
Solderability								
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	(See cumulative data on Table 26B)					
– SO Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	(See cumulative data on Table 26B)					
Resistance to solvents	2015	4 Solvent Solutions	(See cumulative data on Table 26B)					
Resistance to Surface Mount:								
– SO Package			(See cumulative data on Table 26B)					

Table 24C. CMOS F4S/1.0µm Process EEPROM Reliability Data, Package Related Tests
April 1998 to March 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M93C56		M93C66		M28C64 M28C64D	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,						
		– 168 hrs	40	0	80	0	660	0
		– 500 hrs	40	0	80	0	660	0
		– 1000 hrs	40	0	80	0	610	0
Pressure Pot		121°C, 2Atm,						
		– 48 hrs	200	0	350	0	1,230	0
		– 96 hrs	200	0	350	0	1,230	0
		– 168 hrs	200	0	350	0	1,230	0
		– 240 hrs	50	0	100	0	1,180	0
Temperature Cycling	1010	–65 to 150°C,						
		– 100 cycles	200	0	200	0	980	0
		– 200 cycles	50	0	100	0	980	0
		–40 to 150°C,						
		– 500 cycles	-	-	-	-	-	-
		– 1000 cycles	-	-	-	-	-	-
Solderability								
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	(See cumulative data on Table 26B)					
– SO Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	(See cumulative data on Table 26B)					
– PLCC Package			(See cumulative data on Table 26B)					
– TSOP Package			(See cumulative data on Table 26B)					
Resistance to solvents	2015	4 Solvent Solutions	(See cumulative data on Table 26B)					
Resistance to Surface Mount:								
– SO Package			(See cumulative data on Table 26B)					
– TSOP Package			(See cumulative data on Table 26B)					
– PLCC Package			(See cumulative data on Table 26B)					

Table 25A. CMOS F6 0,6µm Process EEPROM Reliability Data, Die Related Tests
April 1998 to March 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M24C01		M24C02		M24C04		M24C08	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V,								
		– 24 hrs	2,400	0	2,400	0	3,760	0	2,320	0
		– 168 hrs	400	0	400	0	560	0	320	0
		– 500 hrs	400	0	400	0	560	0	320	0
		– 1000 hrs	-	-	-	-	-	-	-	-
Retention Bake	1008	150°C,								
		– 168 hrs	250	0	250	0	350	0	200	0
		– 500 hrs	250	0	250	0	350	0	200	0
		– 1000 hrs	250	0	250	0	350	0	200	0
Write/Erase Cycling		100,000 cycles	6,654	0	7,638	0	7,252	1 (a)	9,623	2 (a)
		1,000,000 cycles	2,303	0	2,303	0	2,303	0	2,100	0
Retention Bake	1008	150°C, 168 hrs	-	-	-	-	-	-	-	-

Note: a. Single bit fail.
Oxide quality improvements are addressed in two directions:
– Continuous quality improvement by fab task force.
– “Build in” robustness through product and process design.

Table 25B. CMOS F6 0,6µm Process EEPROM Reliability Data, Die Related Tests
April 1998 to March 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M24C16		M24C32		M24C64	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V,						
		– 24 hrs	3,840	0	3,760	0	1,840	0
		– 168 hrs	3,840	0	560	0	240	0
		– 500 hrs	640	0	560	0	240	0
		– 1000 hrs	-	-	-	-	-	-
Retention Bake	1008	150°C,						
		– 168 hrs	410	0	300	0	150	0
		– 500 hrs	410	0	300	0	150	0
		– 1000 hrs	410	0	300	0	150	0
Write/Erase Cycling		100,000 cycles	6,448	1 (a)	9,653	2 (a)	1,980	0
		1,000,000 cycles	2,100	1 (a)	2,828	0	-	-
Retention Bake	1008	150°C, 168 hrs	-	-	-	-	-	-

Note: a. Single bit fail.
Oxide quality improvements are addressed in two directions:
– Continuous quality improvement by fab task force.
– “Build in” robustness through product and process design.

Table 26A. CMOS F6 0,6µm Process EEPROM Reliability Data, Package Related Tests
April 1998 to March 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M24C01		M24C02		M24C04		M24C08	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,								
		– 168 hrs	80	0	240	0	200	0	320	0
		– 500 hrs	80	0	240	0	200	0	320	0
		– 1000 hrs	80	0	240	0	200	0	320	0
Pressure Pot		121°C, 2Atm,								
		– 48 hrs	650	0	1,450	0	1,200	0	1,350	0
		– 96 hrs	650	0	1,450	0	1,200	0	1,350	0
		– 168 hrs	650	0	1,450	0	1,200	0	1,350	0
		– 240 hrs	200	0	500	0	350	0	450	0
Temperature Cycling	1010	–65 to 150°C,								
		– 100 cycles	700	0	1,000	0	1,200	0	900	0
		– 200 cycles	200	0	500	0	350	0	450	0
		–40 to 150°C,								
		– 500 cycles	-	-	-	-	-	-	-	-
		– 1000 cycles	-	-	-	-	-	-	-	-
Soderability										
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	(See cumulative data on Table 26B)							
– SO Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	(See cumulative data on Table 26B)							
Resistance to solvents	2015	4 Solvent Solutions	(See cumulative data on Table 26B)							
Resistance to Surface Mount:										
– SO Package			(See cumulative data on Table 26B)							

Table 26B. CMOS F6 0,6µm Process EEPROM Reliability Data, Package Related Tests
April 1998 to March 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M24C16		M24C32		M24C64	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,						
		– 168 hrs	200	0	80	0	-	-
		– 500 hrs	200	0	80	0	-	-
		– 1000 hrs	200	0	80	0	-	-
Pressure Pot		121°C, 2Atm,						
		– 48 hrs	1,010	0	250	0	800	0
		– 96 hrs	1,010	0	250	0	800	0
		– 168 hrs	1,010	0	250	0	800	0
		– 240 hrs	430	0	100	0	400	0
Temperature Cycling	1010	–65 to 150°C,						
		– 100 cycles	550	0	200	0	800	0
		– 200 cycles	300	0	100	0	400	0
		–40 to 150°C,						
		– 500 cycles	-	-	-	-	-	-
		– 1000 cycles	-	-	-	-	-	-
Solderability								
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	Cumulative Sample/Fail = 25/0					
– SO Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	Cumulative Sample/Fail = 216/0					
– PLCC Package			Cumulative Sample/Fail = 25/0					
– TSOP Package			Cumulative Sample/Fail = 25/0					
Resistance to solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 196/0					
Resistance to Surface Mount:								
– SO Package			Cumulative Sample/Fail = 13,370/0					
– TSOP Package			Cumulative Sample/Fail = 1,710/0					
– PLCC Package			Cumulative Sample/Fail = 1,010/0					

Table 27. HCMOS S3/1.2µm Process ZEROPOWER NVRAM Reliability Data, Die Related Tests
April 1998 to March 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M48T08 M48T18	
			Samp.	Fail
Operating Life Test	1005	125°C, V_{CC} = 7V, f = 1MHz, – 168 hrs – 500 hrs – 1000 hrs	 1,778 1,774 1,584	 0 0 1(a)

Note: a. Slightly elevated standby current due to gate oxide breakdown in P Channel pull down transistor in the periphery of the die.

Table 28. HCMOS S3/1.2µm Process ZEROPOWER NVRAM Reliability Data, Package Related Tests
April 1998 to March 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M48T08 M48T18	
			Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs	 847 768 767	 0 0 0
Temperature Cycling Caphat	1010	–40 to 100°C, – 100 cycles – 500 cycles – 1000 cycles	 720 - -	 0 - -
Resistance to solvents	2015	4 Solvent Solutions	76	0

Table 29. HCMOS 4DZ/0.8µm Process ZEROPOWER NVRAM Reliability Data, Die Related Tests
April 1998 to March 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M48T35 M48T35Y		M48T58 M48T58Y M48T559Y	
			Samp.	Fail	Samp.	Fail
Operating Life Test	1005	125°C, V_{CC} = 6V, f = 1MHz,				
		– 168 hrs	-	-	899	0
		– 500 hrs	-	-	896	0
		– 1000 hrs	-	-	707	0

Table 30. HCMOS 4DZ/0.8µm Process ZEROPOWER NVRAM Reliability Data, Package Related Tests
April 1998 to March 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M48T35 M48T35Y		M48T58 M48T58Y M48T559Y	
			Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,				
		– 168 hrs	-	-	385	0
		– 500 hrs	-	-	379	0
		– 1000 hrs	-	-	379	0
Hast	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,				
		– 96 hrs	-	-	-	-
		– 168 hrs	-	-	-	-
		– 240 hrs	-	-	-	-
Temperature Cycling	1010	–65 to 150°C,				
		– 100 cycles	-	-	480	0
		– 500 cycles	-	-	400	0
		– 1000 cycles	-	-	320	0
Resistance to solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail =52/0			

Table 31. HCMOS 4DZ/0.7µm Process ZEROPOWER HYBRID MODULE Reliability Data, Die Related Tests
April 1998 to March 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M48T37Y (5V)	
			Samp.	Fail
Operating Life Test	1005	125°C, V_{CC} = 6V, f = 1MHz, – 168 hrs – 500 hrs – 1000 hrs	 1,049 1,043 1,039	 1 (a) 0 0

Note: a. Single bit Failure

Table 32. HCMOS 4DZ/0.7µm Process ZEROPOWER HYBRID MODULE Reliability Data, Package Related Tests
April 1998 to March 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M48T37Y (5V)	
			Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs	 - - -	 - - -
Hast	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V, – 96 hrs – 168 hrs – 240 hrs	 66 66 -	 0 0 -
Temperature Cycling	1010	–40 to 100°C, – 100 cycles – 500 cycles – 1000 cycles	 299 298 298	 0 0 0
Resistance to solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 76/0	

Table 33. ZEROPOWER HYBRID MODULE Reliability Data, Die Related Tests
April 1998 to March 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M48Z512A M48Z2M1		M48Z128 M48Z30	
			Samp.	Fail	Samp.	Fail
Operating Life Test	1005	125°C, V_{CC} = 6V, f = 1MHz,				
		– 168 hrs	-	-	225	0
		– 500 hrs	-	-	224	0
		– 1000 hrs	-	-	175	0

Table 34. ZEROPOWER HYBRID MODULE Reliability Data, Package Related Tests
April 1998 to March 1999

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M48Z512A M48Z2M1		M48Z128 M48Z30	
			Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,				
		– 168 hrs	-	-	104	0
		– 500 hrs	-	-	102	0
		– 1000 hrs	-	-	77	0
Hast	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,				
		– 96 hrs	-	-	-	-
		– 168 hrs	-	-	-	-
		– 240 hrs	-	-	-	-
Temperature Cycling	1010	–40 to 100°C,				
		– 100 cycles	-	-	179	0
		– 500 cycles	-	-	42	0
		– 1000 cycles	-	-	-	-
Resistance to solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = -/-			

Table 35. Statistical Process Control: CMOS E5/0.6µm Process (–35% upgrade) UV EPROM and OTP EPROM, Agrate - Italy F8 Diffusion Line

Key Process Parameters	2Q98	3Q98	4Q98	1Q99
	CPK	CPK	CPK	CPK
Pad Oxide Thickness	2.66	(*)	(*)	2.12
Silicon Nitride Thickness	1.85	(*)	(*)	1.9
Field Oxide Thickness	3.47	(*)	(*)	2.13
Gate Oxide Thickness	2.20	(*)	(*)	1.62
Interpoly Oxide Thickness	2.58	(*)	(*)	1.76
Intermediate Dielectric Thickness	1.7	(*)	(*)	1.73
Polysilicon 1 Thickness	2.72	(*)	(*)	2.54
Active Area Critical Dimensions	1.75	(*)	(*)	2.58
Policide Critical Dimensions	2.00	(*)	(*)	2.13

Key Electrical Parameters	2Q98	3Q98	4Q98	1Q99
	CPK	CPK	CPK	CPK
VT N-Channel Square Tr.	3.94	(*)	(*)	2.31
VT P-Channel Square Tr.	2.17	(*)	(*)	2.22
VT Natural Square Tr.	3.92	(*)	(*)	2.88
VT Memory Cell	1.9	(*)	(*)	1.8
I_{DON} N-Channel	3.48	(*)	(*)	2.79
N+ Active Area Contact Chain	5.85	(*)	(*)	8.1
AL-W Silicide Contact Chain Resistance	1.92	(*)	(*)	2.46

Note: (*) No production data during 3Q98, 4Q98.

Table 36. Statistical Process Control: CMOS E6DM/0.6µm Process (–15% upgrade) UV EPROM and OTP EPROM, Catania - Italy M5 Diffusion Line

Key Process Parameters	2Q98 (1)	3Q98	4Q98	1Q99
	CPK	CPK	CPK	CPK
Pad Oxide Thickness	2.02	(*)	(*)	2.06
Silicon Nitride Thickness	1.78	(*)	(*)	1.81
Field Oxide Thickness	5.20	(*)	(*)	1.62
Gate Oxide Thickness	2.76	(*)	(*)	2.3
Interpoly Oxide Thickness	1.34	(*)	(*)	2.04
Intermediate Dielectric Thickness	1.34	(*)	(*)	1.89
Polysilicon 1 Thickness	2.90	(*)	(*)	1.63
Active Area Critical Dimensions	2.06	(*)	(*)	1.36
Policide Critical Dimensions	1.37	(*)	(*)	1.84

Key Electrical Parameters	2Q98	3Q98	4Q98	1Q99
	CPK	CPK	CPK	CPK
VT N-Channel Square Tr.	3.08	(*)	(*)	2.11
VT P-Channel Square Tr.	1.60	(*)	(*)	1.71
VT Natural Square Tr.	4.55	(*)	(*)	3.06
VT Memory Cell	1.15 (2)	(*)	(*)	1.56
I_{DON} N-Channel	1.14 (2)	(*)	(*)	5.01
N+ Active Area Contact Chain	4.77	(*)	(*)	10.7
AL-W Silicide Contact Chain Resistance	1.35	(*)	(*)	4.68

Note: (*) No production data during 3Q98, 4Q98.
1. Data related to E6 DM Phoenix Diffusion Line.
2. Photo spec. retargeted at poly gate.

Table 37. Statistical Process Control: CMOS E6/0.6µm Process (–10% upgrade) UV EPROM and OTP EPROM, Agrate - Italy F8 Diffusion Line

Key Process Parameters	2Q98	3Q98	4Q98	1Q99
	CPK	CPK	CPK	CPK
Pad Oxide Thickness	2.27	2.22	2.17	2.12
Silicon Nitride Thickness	1.33	1.94	1.59	1.57
Field Oxide Thickness	2.03	3.12	3.70	3.66
Gate Oxide Thickness	2.20	1.72	1.99	1.62
Interpoly Oxide Thickness	2.58	2.37	2.03	1.76
Intermediate Dielectric Thickness	1.72	1.62	1.59	1.73
Polysilicon 1 Thickness	2.72	1.97	2.46	2.54
Active Area Critical Dimensions	2.43	2.26	3.68	2.63
Policide Critical Dimensions	2.07	2.03	1.59	1.74

Key Electrical Parameters	2Q98	3Q98	4Q98	1Q99
	CPK	CPK	CPK	CPK
VT N-Channel 10 x 10µm	2.33	4.35	3.89	2.20
VT P-Channel 10 x 10µm	2.53	2.08	3.27	2.47
VT Natural 10 x 10µm	1.35	2.31	1.93	2.53
VT Memory Cell 0.65 x 0.65µm	1.33	1.51	1.56	1.55
I_{DON} N-Channel 10 x 10µm	2.01	3.15	2.04	2.91
N+ Active Area Contact Chain	5.6	2.87	4.01	4.89
AL-W Silicide Contact Chain Resistance	2.22	2.05	1.87	3.32

Table 38. Statistical Process Control: CMOS E6/0.6µm Process (–10% upgrade) UV EPROM and OTP EPROM, Catania - Italy M5 Diffusion Line

Key Process Parameters	2Q98	3Q98	4Q98	1Q99
	CPK	CPK	CPK	CPK
Pad Oxide Thickness	1.38	1.55	1.62	1.51
Silicon Nitride Thickness	1.33	1.38	1.42	1.38
Field Oxide Thickness	2.59	2.87	2.59	1.64
Gate Oxide Thickness	1.81	2.08	1.81	2.3
Interpoly Oxide Thickness	1.57	1.48	1.57	1.73
N-Well Oxidation	3.74	3.53	3.74	3.24
Polysilicon 1 Thickness	1.51	1.68	1.51	1.81
Active Area Critical Dimensions	2.4	2.98	2.95	1.36
Policide Critical Dimensions	1.44	1.95	1.94	1.84

Key Electrical Parameters	2Q98	3Q98	4Q98	1Q99
	CPK	CPK	CPK	CPK
VT N-Channel Square Tr.	4.12	1.73	2.91	5.06
VT P-Channel Square Tr.	2.76	2.72	3.10	2.49
VT Natural Square Tr.	4.34	1.52	2.08	2.62
VT Memory Cell	1.33	1.44	1.34	1.42
I_{DON} N-Channel	2.72	2.62	2.60	3.16
N+ Active Area Contact Chain	5.51	6.01	6.20	7.87
AL-W Silicide Contact Chain Resistance	2.22	1.72	2.97	2.3

Table 39. Statistical Process Control: CMOS T5/0.8µm Process (–20% upgrade) Flash Memory, Agrate - Italy F8 Diffusion Line

Key Process Parameters	2Q98	3Q98	4Q98	1Q99
	CPK	CPK	CPK	CPK
Field Oxide Thickness	2.44	2.23	2.83	2.61
Polysilicon 1 Thickness	3.64	2.81	4.37	2.75
Gate Oxide Thickness	2.61	1.88	2.01	1.93
Tunnel Oxide Thickness	2.79	2.65	2.60	2.70
ONO Bottom Oxide Thickness	2.06	1.80	2.12	2.52
ONO Nitride Thickness	1.34	1.67	2.19	1.34
ONO Top Oxide Thickness	2.00	2.21	2.58	2.12
Active Area Critical Dimensions	1.73	2.26	1.67	1.80
Polysilicon 2 Critical Dimensions	2.39	2.49	1.82	1.55

Key Electrical Parameters	2Q98	3Q98	4Q98	1Q99
	CPK	CPK	CPK	CPK
VT N-Channel 25 x 25 µm	2.71	1.55	2.19	2.27
VT P-Channel 25 x 25 µm	2.17	1.80	2.33	2.46
BV N-Channel 25 x 0.8 µm	3.36	1.60	1.37	1.86
BV P-Channel 25 x 0.9 µm	4.11	4.10	3.66	3.55
VT Memory Cell 0.8 x 0.8 µm	3.08	2.24	1.59	3.02
I_{DON} N-Channel 25 x 0.8 µm	1.76	2.63	2.56	1.49
Al+N+ Contact Chain	5.16	4.18	4.53	4.55
AL-W Silicide Contact Chain Resistance	5.76	3.81	3.05	2.28

Table 40A. Statistical Process Control: CMOS T6/0.55µm Process Flash Memory, Agrate - Italy R1 Diffusion Line

Key Process Parameters	2Q98	3Q98	4Q98	1Q99
	CPK	CPK	CPK	CPK
Field Oxide Thickness	1.92	2.07	2.23	1.95
First Poly Thickness	1.33	2.05	1.97	2.61
Gate Oxide HV Thickness	2.77	3.05	2.94	2.58
Tunnel Oxide Thickness	1.76	2.17	1.66	2.01
Gate Oxide LV Thickness	1.94	2.22	1.83	2.24
ONO Bottom Oxide Thickness	1.37	1.81	1.34	1.37
ONO Nitride Thickness	1.84	1.89	2.15	2.27
ONO Top Oxide Thickness	1.49	1.96	1.83	2.09
Active Area CD	0.97 (1)	1.15 (1)	1.39	1.39
Second Poly CD	0.99 (2)	1.22 (3)	1.05 (4)	2.29

Note: 1. New resist and new equipment under evaluation.
2. Low CPK value due to new target.
3. Change in exposure energy according to new target.
4. Fine tuning ongoing to align different production island.

Table 40B. Statistical Process Control: CMOS T6/0.55µm Process Flash Memory, Agrate - Italy R1 Diffusion Line

Key Electrical Parameters	2Q98	3Q98	4Q98	1Q99
	CPK	CPK	CPK	CPK
LV-NCh LVS (10 x 0.8) Saturation Current	3.34	4.46	4.79	4.55
LV-PCh LVS (10 x 0.9) BV	2.27	5.4	3.39	2.17
LV-PCh LVS (10 x 0.9) Saturation Current	1.34	2.32	3.90	4.52
LV-PCh SQ. VTh	2.65	1.79	2.23	1.51
HV-NCh SQ. VTh	1.88	1.82	2.09	1.97
HV-NCh (10 x 1.2) LVS Saturation Current	3.34	12.2	14.4	10.2
HV-PCh (10 x 1.3) BV	2.27	3.14	3.31	3.65
HV-PCh (10 x 1.3) Saturation Current	3.29	4.96	5.32	5.00
HV-PCh SQ. VTh	1.59	1.46	1.47	1.35
UV Erased Cell VTh	1.36	1.40	1.49	2.12
N+ Contact Chain	2.54	6.33	7.73	8.73
Silicide Contact Chain	2.36	3.11	3.65	2.97
LV-NCh (10 x 0.8) BV	3.63	4.34	4.92	8.53

Table 41A. Statistical Process Control: CMOS T6/0.55µm Process Flash Memory, Catania - Italy M5 Diffusion Line

Key Electrical Parameters	2Q98	3Q98	4Q98	1Q99
	CPK	CPK	CPK	CPK
Field Oxide Thickness	2.19	2.82	2.28	2.5
First Poly Thickness	1.78	1.45	1.39	1.43
Gate Oxide HV Thickness	(*)	1.61	1.48	1.35
Tunnel Oxide Thickness	1.95	1.51	1.75	1.6
Gate Oxide LV Thickness	1.39	1.66	1.45	1.56
ONO Bottom Oxide Thickness	1.33	1.44	1.33	1.33
ONO Nitride Thickness	1.63	1.52	1.34	1.34
ONO Top Oxide Thickness	1.89	1.83	2.35	2.07
Active Area CD	1.57	2.65	1.88	1.98
Second Poly CD	1.92	2.25	1.41	1.61

Note: (*).No production during 2Q98.

Table 41B. Statistical Process Control: CMOS T6/0.55µm Process Flash Memory, Catania - Italy M5 Diffusion Line

Key Electrical Parameters	2Q98	3Q98	4Q98	1Q99
	CPK	CPK	CPK	CPK
LV-NCh LVS (10 x 0.8) Saturation Current	2.45	1.70	2.91	3.12
LV-PCh LVS (10 x 0.9) BV	2.3	2.29	2.41	2.98
LV-PCh LVS (10 x 0.9) Saturation Current	1.89	1.37	1.87	1.74
LV-PCh SQ. VTh	1.73	1.58	1.97	2.00
HV-NCh (10 x 1.2) LVS BV	(*)	1.99	1.6	2.24
HV-NCh SQ. VTh	(*)	1.53	1.63	1.77
HV-NCh (10 x 1.2) LVS Saturation Current	(*)	3.3	2.8	3.13
HV-PCh (10 x 1.3) BV	(*)	2.44	2.73	3.56
HV-PCh (10 x 1.3) Saturation Current	(*)	2.6	2.3	3.71
HV-PCh SQ. VTh	(*)	1.39	1.36	1.81
UV Erased Cell VTh	1.65	1.88	1.82	1.73
N+ Contact Chain	4.58	3.28	4.51	5.63
Silicide Contact Chain	1.38	1.35	2.55	2.36
LV-NCh (10 x 0.8) BV	3.05	2.08	3.69	3.35

Note: (*).No production during 2Q98.

Table 42A. Statistical Process Control: CMOS T6XU35/0.35µm Process Flash Memory, Agrate - Italy R1 Diffusion Line

Key Process Parameters	2Q98	3Q98	4Q98	1Q99
	CPK	CPK	CPK	CPK
Field Oxide Thickness	-	-	3.16	3.40
First Poly Thickness Gate	-	-	1.33	1.93
Gate Oxide HV Thickness	-	-	2.44	2.10
Tunnel Oxide Thickness	-	-	2.22	1.83
Gate Oxide LV Thickness	-	-	2.09	2.31
ONO Nitride Thickness	-	-	1.03 (1)	1.73
ONO Top Oxide Thickness	-	-	1.01 (1)	1.34
Active Area CD	-	-	1.33	1.77
Second Poly CD	-	-	1.37	2.03

Note: 1. Process optimization to improve thickness uniformity.

Table 42B. Statistical Process Control: CMOS T6XU35/0.35µm Process Flash Memory, Agrate - Italy R1 Diffusion Line

Key Electrical Parameters	2Q98	3Q98	4Q98	1Q99
	CPK	CPK	CPK	CPK
LV-NCh LVS Saturation Current	-	-	1.88	2.13
LV-PCh LVS BV	-	-	1.65	2.61
LV-PCh LVS Saturation Current	-	-	1.44	4.92
LV-PCh SQ. VTh	-	-	1.63	3.15
HV-NCh SQ. VTh	-	-	2.56	2.17
HV-NCh LVS Saturation Current	-	-	2.21	3.39
HV-PCh BV	-	-	4.55	4.19
HV-PCh Saturation Current	-	-	3.82	5.05
HV-NCh LVS BV	-	-	3.51	6.73
LV-NCh LVS BV	-	-	3.20	6.69
LV-NCh SQ. VTh	-	-	4.41	3.65
HV-PCh SQ. VTh	-	-	1.39	2.13
Word Line Resistant	-	-	1.48	1.55
UV Erased Cell VTh	-	-	0.65 (1)	1.98
N+ Contact Chain	-	-	1.69	4.11

Note: 1. Test structure problem suspected. Further investigation in progress.

Table 43A. Statistical Process Control: CMOS T6XU35/0.35µm Process Flash Memory, Catania - Italy M5 Diffusion Line

Key Process Parameters	2Q98	3Q98	4Q98	1Q99
	CPK	CPK	CPK	CPK
Field Oxide Thickness	(*)	(*)	(*)	1.42
First Poly Thickness Gate	(*)	(*)	(*)	1.67
Gate Oxide HV Thickness	(*)	(*)	(*)	1.84
Tunnel Oxide Thickness	(*)	(*)	(*)	1.36
Gate Oxide LV Thickness	(*)	(*)	(*)	1.40
ONO Nitride Thickness	(*)	(*)	(*)	2.97
ONO Top Oxide Thickness	(*)	(*)	(*)	1.67
Active Area CD	(*)	(*)	(*)	0.98 (1)
Second Poly CD	(*)	(*)	(*)	1.33

Note: (*).No production data.New process.
1. Fine tuning of measurement equipment software in progress.

Table 43B. Statistical Process Control: CMOS T6XU35/0.35µm Process Flash Memory, Catania - Italy M5 Diffusion Line

Key Electrical Parameters	2Q98	3Q98	4Q98	1Q99
	CPK	CPK	CPK	CPK
LV-NCh LVS Saturation Current	-	-	-	2.14
LV-PCh LVS BV	-	-	-	1.36
LV-PCh LVS Saturation Current	-	-	-	1.72
LV-PCh SQ. VTh	-	-	-	2.81
HV-NCh SQ. VTh	-	-	-	3.34
HV-NCh LVS Saturation Current	-	-	-	2.15
HV-PCh BV	-	-	-	3.97
HV-PCh Saturation Current	-	-	-	3.26
HV-NCh LVS BV	-	-	-	3.11
LV-NCh LVS BV	-	-	-	2.14
LV-NCh SQ. VTh	-	-	-	2.14
HV-PCh SQ. VTh	-	-	-	2.57
Word Line Resistant	-	-	-	1.33
UV Erased Cell VTh	-	-	-	1.55
N+ Contact Chain	-	-	-	1.72

Table 44. Statistical Process Control: CMOS F6 0.6µm Process EEPROM Memory, Agrate - Italy F8 Diffusion Line

Key Process Parameters	2Q98	3Q98	4Q98	1Q99
	CPK	CPK	CPK	CPK
Pad Oxide Thickness	2.27	2.22	2.17	2.12
Silicon Nitride Thickness	1.37	1.90	1.86	1.58
Field Oxide Thickness	2.44	2.23	2.83	2.61
Gate Oxide 1 Thickness	2.20	1.86	2.23	2.08
Gate Oxide 2 Thickness	1.90	2.34	1.81	2.35
Tunnel Oxide Thickness	3.24	2.50	2.62	2.73
Dialectric Thickness	1.53	1.73	2.20	1.99
Active Area Critical Dimensions	1.51	1.70	1.81	1.53
Policide Critical Dimensions	1.77	2.08	1.89	1.89
Poly Front Deposition Thickness	2.08	1.87	2.21	1.98
Contacts Critical Dimension	1.62	1.59	1.65	1.79

Key Electrical Parameters	2Q98	3Q98	4Q98	1Q99
	CPK	CPK	CPK	CPK
VT N-Channel 10 x 10µm	2.35	1.99	2.26	2.20
VT P-Channel 10 x 10µm	2.61	2.48	2.31	2.55
VT Natural 10 x 10µm	3.18	1.79	3.56	2.37
BV N-Channel 10 x 10µm	2.44	2.77	2.26	2.51
BV P-Channel 10 x 10µm	1.33	2.14	1.42	1.57
EBD-LVN	5.37	5.43	4.67	3.38
N+ Active Area Contact Chain	2.56	2.89	3.46	3.86
EBD-TUN	2.73	1.87	2.92	1.86

Table 45A. Statistical Process Control: CMOS M4S40-F-DLM/0.7µm Process Smartcard Product, Rousset - France Diffusion Line

Key Process Parameters	2Q98	3Q98	4Q98	1Q99
	CPK	CPK	CPK	CPK
Field Oxide Thickness	-	-	-	3.13
Gate Oxide Thickness	-	-	-	1.64
Tunnel Oxide Thickness	-	-	-	1.83
Polysilicium	-	-	-	1.67
Poly for Logic	-	-	-	3.13
Vapox	-	-	-	2.34
TEOS IMD1	-	-	-	2.34
USG IMD1	-	-	-	3.02

Table 45B. Statistical Process Control: CMOS M4S40-F-DLM/0.7µm Process Smartcard Product, Rousset - France Diffusion Line

Key Electrical Parameters	2Q98	3Q98	4Q98	1Q99
	CPK	CPK	CPK	CPK
Resist N+	-	-	-	2.93
Resist P+	-	-	-	3.3
Contact AL/N+	-	-	-	4.19
Contact AL/P+	-	-	-	3.2
Contact AL/POLY	-	-	-	13.08
VT En (25x25)	-	-	-	2.7
VT Ep (25x25)	-	-	-	1.68
VT Mc Erase	-	-	-	2.41
VT Mc Write	-	-	-	4.27
BV Diode N+/P-	-	-	-	4.08
BV Diode P+/N-	-	-	-	9.68
IDS En (25x0.8)	-	-	-	1.89
IDS Ep (25x0.8)	-	-	-	1.74
QBD Tunnel	-	-	-	2.24

Table 46. Statistical Process Control: UV EPROM Ceramic Frit-Seal Package Assembly Line, Singapore

Key Process Parameters	2Q98	3Q98	4Q98	1Q99
	CPK	CPK	CPK	CPK
Shear Test (D.A.)	26.2	4.5	6.9	6.8
Stud Pull	1.57	1.5	1.6	1.9
Bond Strength (W.B.)	5.58	5.5	6.4	6.7
SN Thickness (Tin Plate)	1.77	1.7	1.8	1.6

Table 47. Statistical Process Control: TSOP Package Assembly Line, Singapore

Key Process Parameters	2Q98	3Q98	4Q98	1Q99
	CPK	CPK	CPK	CPK
Shear Test (D.A.)	2.38	2.06	2.33	2.3
Ball Shear (W.B.)	2.65	3.42	3.43	3.9
Bond Strength (W.B.)	2.76	1.67	2.00	2.0
Coplanarity	4.47	2.82	5.47	5.2
Plating Thickness	1.60	2.30	2.03	1.8

Table 48. Statistical Process Control: PLCC Package Assembly Line, Singapore

Key Process Parameters	2Q98	3Q98	4Q98	1Q99
	CPK	CPK	CPK	CPK
Shear Test (D.A.)	3.37	3.5	4.1	3.2
Ball Shear (W.B.)	2.21	2.9	3.2	3.3
Bond Strength (W.B.)	2.10	1.8	1.9	1.8
Plating Thickness	1.90	1.9	1.9	6.5
Coplanarity	-	6.6	5.7	1.8

If you have any questions or suggestion concerning the matters raised in this document please send them to the following electronic mail address:

ask.memory@st.com (for general enquiries)

Please remember to include your name, company, location, telephone number and fax number