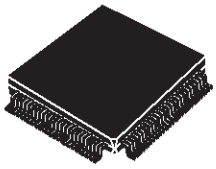
TDA7500

DIGITAL AM/FM SIGNAL PROCESSOR

PRODUCT PREVIEW

- FULL SOFTWARE FLEXIBILITY WITH TWO 24X24 BIT DSP CORES
- AM/FM PROCESSING
- AUDIO-PROCESSING AND SOUND-PROCESSING
- HARDWARE RDS FILTER, DEMODULATOR & DECODER
- INTEGRATED CODEC
- IIC AND SPI CONTROL INTERFACES
- SPI DEDICATED TO DISPLAY MICRO
- 6 CHANNEL SERIAL AUDIO INTERFACE SAI
- SPDIF RECEIVER WITH SAMPLE RATE CONVERTER
- EXTERNAL MEMORY INTERFACE
- DOUBLE DEBUG INTERFACE
- ON-CHIP PLL
- 5V-TOLERANT 3V I/O INTERFACE
- MULTIFUNCTION GENERAL PURPOSE I/O PORTS

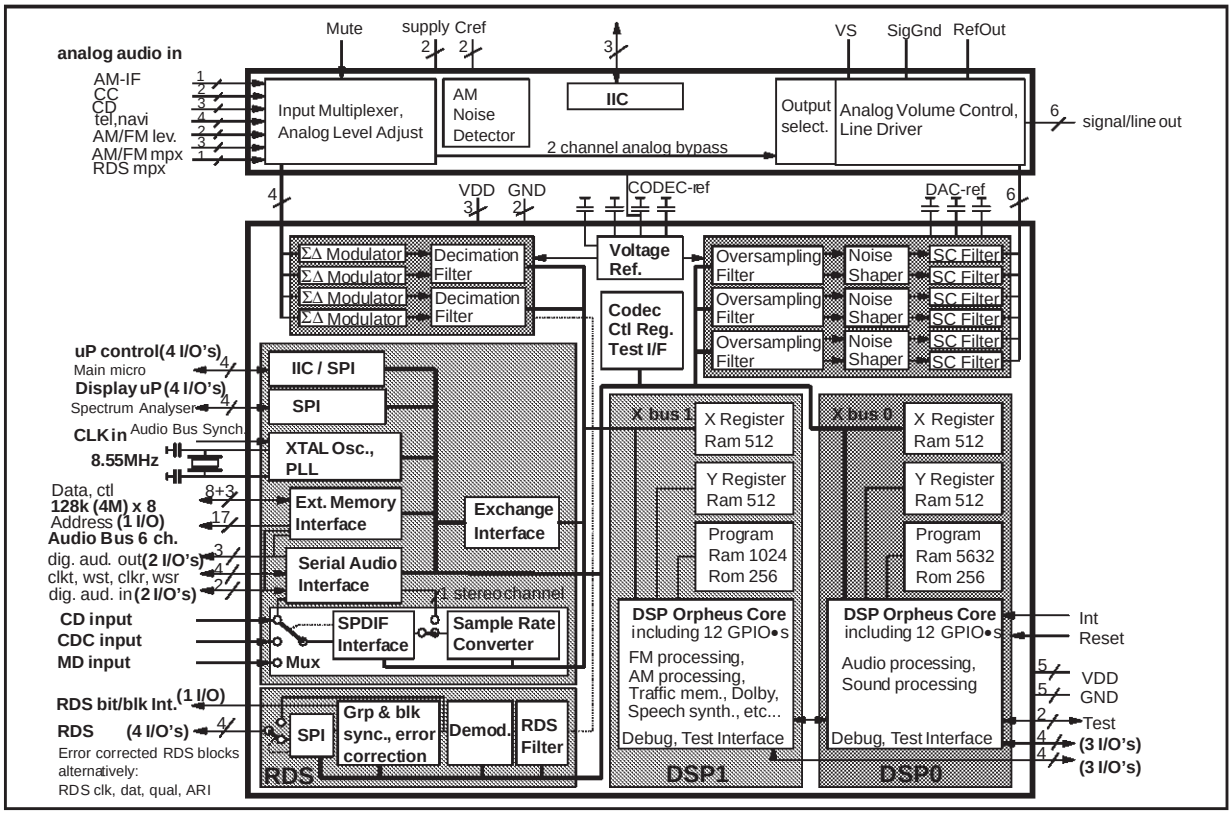


TQFP100 Power with Slug Down

DESCRIPTION

The TDA7500 is an integrated circuit implementing a fully digital, integrated and advanced solution to perform the signal processing in front of the power amplifier and behind the AM/FM tuner or any other audio sources. The chip integrates two 43 MIPs DSP cores: one for stereo decoding, noise blanking, weak signal processing and multi-

BLOCK DIAGRAM



path detection and one for sound processing. An I2C/SPI interface is implemented for control and communication with the main micro.

A separate SPI is available to interface the display micro.

The DSP cores are integrated with their associated data and program memories. The peripherals and interfaces I^2C, SPI, Serial Audio Interface (SAI), PLL Oscillator, External Memory Interface, (EMI), General Purpose I/O register (Port A) and the D/A registers are connected to and controlled by DSP0, whereas the A/D registers, the SPDIF and the General Purpose I/O register (Port B) are connected to and controlled by DSP1. The Debug and Test Interface are connected to both DSP cores.

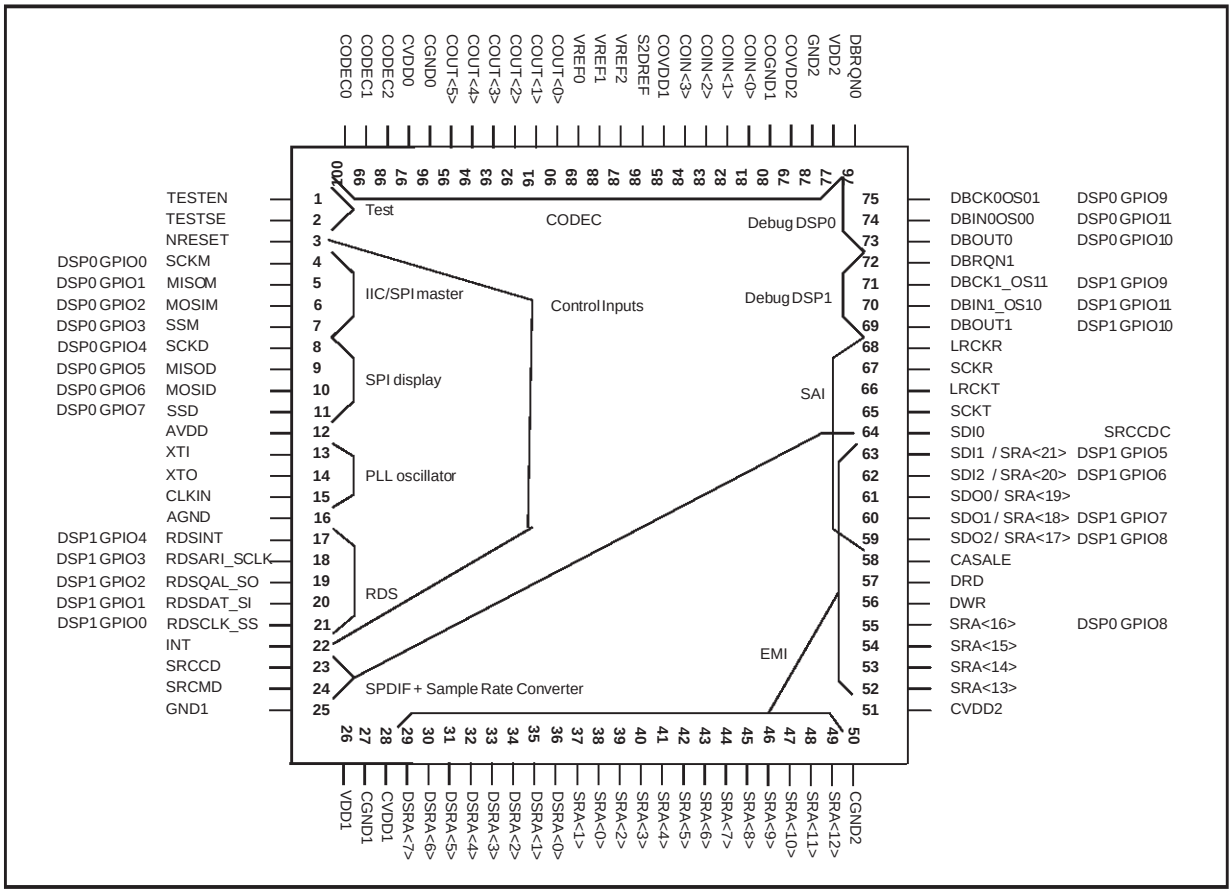
The TDA7500 is supposed to be used in kit with the TDA7501 or any other device of the same family. Thanks to the serial audio interface also digital sources can be processed and a direct output to a digital bus is also available.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
VDD VCC	Power supplies	Digital Analog	4.6 4.6	V V
	Analog Input Voltage		-0.5 to (VDD+0.5)	V
	Digital Input Voltage		-0.5 to (VCC+0.5)	V
T_{amb}	Operating Temperature Range		-40 to 85	°C
T_{stg}	Storage Temperature		-55 to 150	°C

Warning: Operation at or beyond these limit may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

PIN CONNECTION



PIN DESCRIPTION

N°	NAME	TYPE	DESCRIPTION
1	GND1		Ground pin dedicated to the digital periphery.
2	VDD1		Supply pin dedicated to the digital periphery.
3	TESTEN	I	Test Enable (Input). When active, puts the chip into test mode and muxes the XTI clock to all flip-flops. When TEST_SE is also active, the scan chain shifting is enabled.
4	TESTSE	I	SCAN Enable (Input). When active with TESTEN also active, controls the shifting of the internal scan chains. When active with TESTEN not active, sets all tri-state outputs into hi-impedance mode
5	NRESET	I	System Reset (Input). A low level applied to NRESET input initializes the IC.
6	SCKM/DSP0_GPIO0	I/O	I^2C Serial Clock Line (Input/Output)/SPI Bit Clock (Input)/General Purpose I/O (Input/Output). Clock line for I^2C bus. Schmitt trigger input. If SPI interface is enabled, behaves as SPI bit clock. Optionally it can be used as general purpose I/O controlled by DSP0.
7	MISOM/DSP0_GPIO1	I/O	I^2C Serial Data Line (Input/Output)/SPI Master Input Slave Output Serial Data (Input/Output)/General Purpose I/O (Input/Output). Data line for I^2C bus. Schmitt trigger input. If SPI is enabled, behaves as Serial Data Input when in SPI Master Mode and Serial Data Output when in SPI Slave Mode. Optionally it can be used as general purpose I/O controlled by DSP0.
8	MOSIM/DSP0_GPIO2	I/O	SPI Master Output Slave Input Serial Data (Input/Output)/General Purpose I/O (Input/Output). Serial Data Output when in SPI Master Mode and Serial Data Input when in SPI Slave Mode. Optionally it can be used as general purpose I/O controlled by DSP0.
9	SSM/DSP0_GPIO3	I	SPI Slave Select (Input)/General Purpose I/O (Input/Output). If SPI is enabled, behaves as Slave Select line for SPI bus. Optionally it can be used as general purpose I/O controlled by DSP0.
10	SCKD/DSP0_GPIO4	I	SPI Bit Clock (Input)/General Purpose I/O (Input/Output). SPI bit clock. Schmitt trigger input. Optionally it can be used as general purpose I/O controlled by DSP0.
11	MISOD/DSP0_GPIO5	I/O	SPI Master Input Slave Output Serial Data (Input/Output)/General Purpose I/O (Input/Output). Schmitt trigger input. Behaves as Serial Data Input when in SPI Master Mode and Serial Data Output when in SPI Slave Mode. Optionally it can be used as general purpose I/O controlled by DSP0.
12	MISOD/DSP0_GPIO6	I/O	SPI Master Output Slave Input Serial Data (Input/Output)/General Purpose I/O (Input/Output). Serial Data Output when in SPI Master Mode and Serial Data Input when in SPI Slave Mode. Optionally it can be used as general purpose I/O controlled by DSP0.
13	SSD/DSP0_GPIO7	I	SPI Slave Select (Input)/General Purpose I/O (Input/Output). Behaves as Slave Select line for SPI bus. Optionally it can be used as general purpose I/O controlled by DSP0.
14	CLKIN	I	Clock Input pin (Input). Clock from external digital audio source to synchronize the internal PLL.
15	AVDD		audio source to synchronize the internal PLL.
16	XTI	I	Crystal Oscillator Input (Input). External Clock Input or crystal Oscillator input.
17	XTO	O	Crystal Oscillator Output (Output). Crystal Oscillator output drive.
18	AGND		Ground pin dedicated to the PLL
19	RDSINT/DSP1_GPIO4	O	RDS bit/block interrupt (Output)/General Purpose I/O (Input/Output). Provides an interrupt to the main micro. Optionally it can be used as general purpose I/O controlled by DSP1.

PIN DESCRIPTION (continued)

N°	NAME	TYPE	DESCRIPTION
20	RDSARI_SCK/DSP1_GPIO3	O	SPI Bit Clock (Input)/ARI indicator (Output)/General Purpose I/O (Input/Output). Schmitt trigger input. If SPI interface is enabled, behaves as SPI bit clock. Optionally it provides the ARI indication bit. Optionally it can be used as general purpose I/O controlled by DSP1.
21	RDSQAL_SO/DSP1_GPIO2	O	SPI Slave Output Serial Data (Output)/RDS Bit Quality (Output)/General Purpose I/O (Input/Output). If SPI is enabled, behaves as Serial Data Output. Optionally it provides the RDS serial data quality information. Optionally it can be used as general purpose I/O controlled by DSP1.
22	RDSDAT_SI/DSP1_GPIO1	I	SPI Slave Input Serial Data (Input)/RDS Bit Data (Output)/General Purpose I/O (Input/Output). If SPI is enabled, behaves as Serial Data Input. Optionally it provides the RDS serial data stream. Optionally it can be used as general purpose I/O controlled by DSP1.
23	RDSCLK_SS/DSP1_GPIO0	I	SPI Chip Select (Input)/RDS Bit Clock (Output)/General Purpose I/O (Input/Output). If SPI is enabled, behaves as Chip Select line for SPI bus. Optionally it provides the 1187.5Hz RDS Bit Clock. Optionally it can be used as general purpose I/O controlled by DSP1.
24	INT	I	External interrupt line (Input). When this line is asserted low, the DSP may be interrupted.
25	CGND1		Ground pin dedicated to the digital core part.
26	CVDD1		Supply pin dedicated to the digital core part.
27	SCRCCD	I	SPDIF Input 1 (Input). Stereo SPDIF input to connect a digital audio source like a CD.
28	SCRCMD	I	SPDIF Input 2 (Input). Stereo SPDIF input to connect a digital audio source like a MD.
29	DSRA<7>	I/O	DSP SRAM Data Lines<7> (Input/Output). When in SRAM Mode this pin act as the EMI data line 7.
30	DSRA<6>	I/O	DSP SRAM Data Lines<6> (Input/Output). When in SRAM Mode this pin act as the EMI data line 6.
31	DSRA<5>	I/O	DSP SRAM Data Lines<5> (Input/Output). When in SRAM Mode this pin act as the EMI data line 5.
32	DSRA<4>	I/O	DSP SRAM Data Lines<4> (Input/Output). When in SRAM Mode this pin act as the EMI data line 4.
33	DSRA<3>	I/O	DSP SRAM Data Line<3> (Input/Output)/DSP DRAM Data Line<3> (Input/Output). This pin act as the EMI data line 3 in both SRAM Mode and DRAM Mode.
34	DSRA<2>	I/O	DSP SRAM Data Line<2> (Input/Output)/DSP DRAM Data Line<2> (Input/Output). This pin act as the EMI data line 2 in both SRAM Mode and DRAM Mode.
35	DSRA<1>	I/O	DSP SRAM Data Line<1> (Input/Output)/DSP DRAM Data Line<1> (Input/Output). This pin act as the EMI data line 1 in both SRAM Mode and DRAM Mode.
36	DSRA<0>	I/O	DSP SRAM Data Line<0> (Input/Output)/DSP DRAM Data Line<0> (Input/Output). This pin act as the EMI data line 0 in both SRAM Mode and DRAM Mode.
37	SRA<0>	O	DSP SRAM Address Line<0> (Output)/DSP DRAM Address Line<0> (Output). This pin act as the EMI address line 0 in both SRAM Mode and DRAM Mode.
38	SRA<1>	O	DSP SRAM Address Line<1> (Output)/DSP DRAM Address Line<1> (Output). This pin act as the EMI address line 1 in both SRAM Mode and DRAM Mode.

PIN DESCRIPTION (continued)

N°	NAME	TYPE	DESCRIPTION
39	SRA<2>	O	DSP SRAM Address Line<2> (Output)/DSP DRAM Address Line<2> (Output). This pin act as the EMI address line 2 in both SRAM Mode and DRAM Mode.
40	SRA<3>	O	DSP SRAM Address Line<3> (Output)/DSP DRAM Address Line<3> (Output). This pin act as the EMI address line 3 in both SRAM Mode and DRAM Mode.
41	SRA<4>	O	DSP SRAM Address Line<4> (Output)/DSP DRAM Address Line<4> (Output). This pin act as the EMI address line 4 in both SRAM Mode and DRAM Mode.
42	SRA<5>	O	DSP SRAM Address Line<5> (Output)/DSP DRAM Address Line<5> (Output). This pin act as the EMI address line 5 in both SRAM Mode and DRAM Mode.
43	SRA<6>	O	DSP SRAM Address Line<6> (Output)/DSP DRAM Address Line<6> (Output). This pin act as the EMI address line 6 in both SRAM Mode and DRAM Mode.
44	SRA<7>	O	DSP SRAM Address Line<7> (Output)/DSP DRAM Address Line<7> (Output). This pin act as the EMI address line 7 in both SRAM Mode and DRAM Mode.
45	SRA<8>	O	DSP SRAM Address Line<8> (Output)/DSP DRAM Address Line<8> (Output). This pin act as the EMI address line 8 in both SRAM Mode and DRAM Mode.
46	SRA<9>	O	DSP SRAM Address Line<9> (Output)/DSP DRAM Address Line<9> (Output). This pin act as the EMI address line 9 in both SRAM Mode and DRAM Mode.
47	SRA<10>	O	DSP SRAM Address Line<10> (Output)/DSP DRAM Address Line<10> (Output). This pin act as the EMI address line 10 in both SRAM Mode and DRAM Mode.
48	SRA<11>	O	DSP SRAM Address Line<11> (Output)/DSP DRAM Address Line<11> (Output). This pin act as the EMI address line 11 in both SRAM Mode and DRAM Mode.
49	SRA<12>	O	DSP SRAM Address Line<12> (Output)/DSP DRAM Address Line<12> (Output). This pin act as the EMI address line 12 in both SRAM Mode and DRAM Mode.
50	CGND2		Ground pin dedicated to the digital core part.
51	CVDD2		Supply pin dedicated to the digital core part.
52	SRA<13>	O	DSP SRAM Address Line<13> (Output)/DSP DRAM Address Line<13> (Output). This pin act as the EMI address line 13in both SRAM Mode and DRAM Mode.
53	SRA<14>	O	DSP SRAM Address Line<14> (Output)/DSP DRAM Address Line<14> (Output). This pin act as the EMI address line 14 in both SRAM Mode and DRAM Mode.
54	SRA<15>	O	DSP SRAM Address Line<15> (Output)/DSP DRAM Address Line<15> (Output). This pin act as the EMI address line 15 in both SRAM Mode and DRAM Mode.
55	SRA<16>/DSP0_GPIO8	O	DSP SRAM Address Line<16> (Output)/DSP DRAM Address Line<16> (Output)/General Purpose I/O (Input/Output). This pin acts as the EMI address line 16 in both SRAM Mode and DRAM Mode. Optionally it can be used as general purpose I/O controlled by DSP0.
56	DWR	O	DSP SRAM Write Enable (Output)/DRAM Write Enable (Output). This pin serves as the write enable for the EMI in both DRAM and SRAM Mode.
57	DRD	O	DSP SRAM Read Enable(Output)/DRAM Read Enable (Output). This pin serves as the read enable for the EMI in both DRAM and SRAM Mode.

PIN DESCRIPTION (continued)

N°	NAME	TYPE	DESCRIPTION
58	CASALE	O	DSP DRAM Column Address Strobe (Output). When in DRAM Mode this pin acts as the column address strobe.
59	SDO<2>/SRA<17>/DSP1_GPIO<8>	O	SAI Outputs (Output)/EMI SRAM Address Line<17> (Output)/General Purpose I/O (Input/Output). One stereo channel SAI data output in SAI mode. EMI address line 17 in SRAM Mode. Optionally it can be used as a general purpose I/O.
60	SDO<2>/SRA<18>/DSP1_GPIO<7>	O	SAI Outputs (Output)/EMI SRAM Address Line<18> (Output)/General Purpose I/O (Input/Output). One stereo channel SAI data output in SAI mode. EMI address line 18 in SRAM Mode. Optionally it can be used as a general purpose I/O.
61	SDO<0>/SRA<19>	O	SAI Output (Output)/EMI SRAM Address Line<19> (Output). One stereo channel SAI data output in SAI mode. EMI address line 19 in SRAM Mode.
62	SDI<2>/SRA<20>/DSP1_GPIO<6>	I	SAI Input (Input)/EMI SRAM Address Line<20> (Output)/General Purpose I/O (Input/Output). One stereo channel SAI data input in SAI mode. EMI address line 20 in SRAM Mode. Optionally it can be used as a general purpose I/O.
63	SDI<1>/SRA<21>/RAS/DSP1_GPIO<5>	I	SAI Input (Input)/EMI SRAM Address Line<21> (Output)/DRAM Row Address Strobe (Output)/General Purpose I/O (Input/Output). One stereo channel SAI data input in SAI mode. EMI address line 21 in SRAM Mode. When in DRAM Mode this pin acts as the row address strobe. Optionally it can be used as a general purpose I/O.
64	SDI<0>/SRCCDC	I	SAI Input (Input)/SPDIF Input 3 (Input). One stereo channel SAI data input in SAI mode. Stereo SPDIF input intended to connect a digital audio source like a CD changer in SPDIF mode.
65	SCKT	I/O	SAI transmitter Bit Clock (Input/Output). SAI transmitter bit clock. Master or slave.
66	LRCKT	I/O	SAI transmitter Left-Right Clock (Input/Output). SAI transmitter Left-Right clock. Can be master or slave mode.
67	SCKR	I/O	SAI receiver Bit Clock (Input/Output). SAI receiver bit clock.
68	LRCKR	I/O	SAI receiver Left-Right Clock (Input/Output). SAI receiver Left-Right clock.
69	DBOUT1/DSP1_GPIO10	I/O	Debug Port Serial Output (Input/Output)/ General Purpose I/O (Input/Output). The serial data output for the Debug Port. Optionally it can be used as a general purpose I/O.
70	DBIN1/OS10/DSP1_GPIO11	I/O	Debug Port Serial Input/Chip Status 0 (Input/Output)/ General Purpose I/O (Input/Output). The serial data input for the Debug Port is provided when an input. When an output, together with OS1 provides information about the chip status. Optionally it can be used as a general purpose I/O.
71	DBCK1/OS11/DSP1_GPIO9	I/O	Debug Port Bit Clock/Chip Status 1 (Input/Output)/General Purpose I/O (Input/Output). The serial clock for the Debug Port is provided when an input. When an output, together with OS0 provides information about the chip status. Optionally it can be used as a general purpose I/O.
72	DBRQN1	I	Debug Port Request Input (Input). Means of entering the Debug mode of operation.
73	DBOUT0/DSP0_GPIO10	I/O	Debug Port Serial Output (Input/Output)/ General Purpose I/O (Input/Output). The serial data output for the Debug Port. Optionally it can be used as a general purpose I/O.
74	DBIN0/OS00/DSP0_GPIO11	I/O	Debug Port Serial Input/Chip Status 0 (Input/Output)/ General Purpose I/O (Input/Output). The serial data input for the Debug Port is provided when an input. When an output, together with OS1 provides information about the chip status. Optionally it can be used as a general purpose I/O.

PIN DESCRIPTION (continued)

N°	NAME	TYPE	DESCRIPTION
75	DBCK0/OS01/DSP0_GPIO9	I/O	Debug Port Bit Clock/Chip Status 1 (Input/Output)/General Purpose I/O (Input/Output). The serial clock for the Debug Port is provided when an input. When an output, together with OS0 provides information about the chip status. Optionally it can be used as a general purpose I/O.
76	DBRQN0	I	Debug Port Request Input (Input). Means of entering the Debug mode of operation.
77	VDD2		Supply pin dedicated to the digital periphery.
78	GND2		Ground pin dedicated to the digital periphery.
79	ADC<0>	I	Analog Inputs (Input). Single ended analog signal inputs to the ADC.
80	ADC<1>	I	Analog Inputs (Input). Single ended analog signal inputs to the ADC.
81	ADC<2>	I	Analog Inputs (Input). Single ended analog signal inputs to the ADC.
82	ADC<3>	I	Analog Inputs (Input). Single ended analog signal inputs to the ADC.
83	S2DREF	I	Voltage Reference (Input). External decoupling of the analog reference used for the single to differential ended converter.
84	ADCVDDREF	I	Voltage Reference (Input). Analog voltage reference input. Signal is supplied by A354.
85	ADCREF<2>	I	Voltage Reference (Input). External decoupling of the analog references used for the sigma delta modulator.
86	ADCREF<1>	I	Voltage Reference (Input). External decoupling of the analog references used for the sigma delta modulator.
87	ADCREF<0>	I	Voltage Reference (Input). External decoupling of the analog references used for the sigma delta modulator.
88	ADCVDD		Analog Supply pin dedicated to the A/D converter.
89	ADCGND		Analog Ground pin dedicated to the A/D converter.
90	DAC<0>	O	Analog Outputs (Output). Analog signal outputs of the DAC
91	DAC<1>	O	Analog Outputs (Output). Analog signal outputs of the DAC
92	DAC<2>	O	Analog Outputs (Output). Analog signal outputs of the DAC
93	DAC<3>	O	Analog Outputs (Output). Analog signal outputs of the DAC
94	DAC<4>	O	Analog Outputs (Output). Analog signal outputs of the DAC
95	DAC<5>	O	Analog Outputs (Output). Analog signal outputs of the DAC
96	DACREF<2>	I	Voltage Reference (Input). External decoupling of the analog references of the CODEC.
97	DACREF<1>	I	Voltage Reference (Input). External decoupling of the analog references of the CODEC.
98	DACREF<0>	I	Voltage Reference (Input). External decoupling of the analog references of the CODEC.
99	DACGND		Analog Ground pin dedicated to the D/A converter.
100	DACVDD		Analog Supply pin dedicated to the D/A converter.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{DDC}	3.3V Power Supply Voltage		3	3.3	3.6	V
T_j	Operating Junction Temperature		-40		125	°C

POWER CONSUMPTION

Symbol	Parameter	Value	Unit
I_{dd}	Maximum current for core power supply @3.3V	450	mA

Note: 43MHz internal DSP clock at Tamb

ADC PERFORMANCE Some of the relevant ADC parameters are reported in the following table:
(T = 25°C, AV_{DD} = 3.3V, measurement bandwidth 10Hz to 20KHz, A-Weighted Filter.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
	Maximum input level (1)				1	Vrms
	Sample rate		32		48	KHz
	Frequency Response	@ 20KHz with f_s = 44.1KHz		-3		dB
	Instant Dynamic Range	-60dB analog input	90	93		dB
	SNR	1KHz; -3dB analog input	90	93		dB
	(THD + N)/S	-3dB analog input		-85		dB
	PSRR	0.1Vp @ 1KHz	45			dB
	Input Impedance		10	30		KΩ
	Crosstalk	1Vrms input @ 15KHz	70			dB
	Gain mismatch between four input	@ 1KHz	-0.5		0.5	dB
	CMRR	@ 1KHz	40			dB
	CM Input range				100	mV

(1) Corresponding to 2VRMS Maximum Differential Input.

DAC PERFORMANCE Some of the relevant DAC parameters are reported in the following table:
(T = 25°C, AV_{DD} = 3.3V, measurement bandwidth 10Hz to 20KHz, A-Weighted Filter 0dB gain, output load 30kΩ)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
	Maximum output level (1)				1	Vrms
	Sample rate		32		48	KHz
	Frequency Response	@ 20KHz with f_s = 44.1KHz		-3		dB
	Dynamic Range	-60dB analog input	90	93		dB
	SNR	1KHz -3dB analog output	90	93		dB
	Total D R			100		dB
	Digital Silence	0000$ digital input		93		dB
	(THD + N)/S	-3dB analog input		-85		dB
	PSRR	0.1Vp @ 1KHz	45			dB
	Output Impedance		30			kΩ
	Crosstalk	1Vrms output @ 15KHz	70			dB
	Gain mismatch between six outputs	@ 1KHz	-0.5		0.5	dB

(1) Corresponding to 2VRMS Maximum Differential Output.

FUNCTIONAL DESCRIPTION.

The TDA7500 IC broken up into two distinct blocks. One block contains the two DSP Cores and their associated peripherals. The other contains the ADC, DAC and the RDS filter, demodulator and decoder.

24-BIT DSP CORE.

The two DSP cores are used to process the audio and FM/AM data, coming from the ADC, either any kind of digital data coming via SPDIF or SAI. After the digital signal processing these data are sent to the DAC for analog conversion. Functions such as volume, tone, balance, and fader control, as well as spatial enhancement and general purpose signal processing may be performed by the DSP0. When FM/AM mode is selected, DSP1 is fully devoted to AM/FM processing. Nevertheless it can be used for any kind of different application, when a different input source is selected.

Some capabilities of the DSPs are listed below:

- Single cycle multiply and accumulate with convergent rounding and condition code generation
- 2 x 56-bit Accumulators
- Double precision multiply
- Scaling and saturation arithmetic
- 48-bit or 2 x 24-bit parallel moves
- 64 interrupt vector locations
- Fast or long interrupts possible
- Programmable interrupt priorities and masking
- 8 each of Address Registers, Address Offset Registers and Address Modulo Registers
- Linear, Reverse Carry, Multiple Buffer Modulo, Multiple Wrap-around Modulo address arithmetic
- Post-increment or decrement by 1 or by offset, Index by offset, predecrement address
- Repeat instruction and zero overhead DO loops
- Hardware stack capable of nesting combinations of 7 DO loops or 15 interrupts/subroutines
- Bit manipulation instructions possible on all registers and memory locations. Also Jump on bit test.
- 4 pin serial debug interface
- Debug ccess to all internal registers, buses and memory locations
- 5 word deep program address history FIFO
- Hardware and software breakpoints for both program and data memory accesses
- Debug Single stepping, Instruction injection and Disassembly of program memory

DSP PERIPHERALS

There are a number of peripherals that are tightly coupled to the two DSP Cores. Same of the peripherals are connected to DSP 0 others are connected to DSP1.

- 512 x 24-Bit X-RAM.
- 512 x 24-Bit Y-RAM.
- 1024 x 24-Bit Program RAM (5.5K x 24 for DSP1)
- 128 x 24-Bit Boot ROM for each DSP.
- Serial Audio Interface (SAI)
- SPDIF receiver with sampling rate conversion
- I^2C and SPI interface
- XCHG Interface for DSP to DSP communication.
- External Memory Interface (DRAM/SRAM) for time-delay and traffic information.
- Double Debug Port

DATA AND PROGRAM MEMORY

Both DSP0 and DSP1 have an identical set of Data and Program memories attached to them. Each of the memories are described below and it is implied that there are two of each type, one set connected to DSP0 and the other to DSP1. The only exception is the case of the P-RAM where DSP0 has a 1024 x 24-Bit PRAM and DSP1 has a 5.5K x 24-Bit PRAM.

512 x 24-Bit X-RAM (XRAM)

This is a 512 x 24-Bit Single Port SRAM used for storing coefficients. The 16-Bit XRAM address, XABx(15:0) is generated by the Address Generation Unit of the DSP core. The 24-Bit XRAM Data, XDBx(23:0), may be written to and read from the Data ALU of the DSP core. The XDBx Bus is also connected to the Internal Bus Switch so that it can be routed to and from all peripheral blocks.

512 x 24 Bit Y-RAM (YRAM)

This is a 512 x 24-Bit Single Port SRAM used for storing coefficients. The 16-Bit address, YABx(15:0) is generated by the Address Generation Unit of the DSP core. The 24-Bit Data, YDBx(23:0), is written to and read from the Data ALU of the DSP core. The YDBx Bus is also connected to the Internal Bus Switch so that it can be routed to and from other blocks.

1024 x 24-Bit Program RAM (PRAM 5.5K x 24-bit for DSP1)

This is a 1024 x 24-Bit Single Port SRAM used for storing and executing program code. The 16-

Bit PRAM Address, PABx(15:0) is generated by the Program Address Generator of the DSP core for Instruction Fetching, and by the AGU in the case of the Move Program Memory (MOVEM) Instruction. The 24-Bit PRAM Data (Program Code), PDBx(23:0), can only be written to using the MOVEM instruction. During instruction fetching the PDBx Bus is routed to the Program Decode Controller of the DSP core for instruction decoding.

256 x 24-Bit Bootstrap ROM (PROM)

This is a 256 x 24-Bit factory programmed Boot ROM used for storing the program sequence and for initializing the DSP. Essentially this consists of reading the data via I^2C, SPI or EMI interface and store it in PRAM, XRAM, YRAM, and/or external DRAM.

Serial Audio Interface (SAI)

The SAI is used to deliver digital audio to the DSPs from an external source. Once processed by the DSPs, it can be returned through this interface either sent to the DAC for D/A conversion. The features of the SAI are listed below.

- 3 Synchronized Stereo Data Transmission Lines
- 3 Synchronized Stereo Data Reception Lines
- Master and Slave operating mode: clock lines can be both master and slave.
- Receive and Transmit Data Registers have two locations to hold left and right data.

XCHG Interface (DSP to DSP Exchange Interface)

The Exchange Interface peripheral provides bidirectional communication between DSP0 and DSP1. Both 24 bit word data and four bit Flag data can be exchanged. A FIFO is utilized for received data. It minimizes the number of times an Exchange Interrupt Service Routine would have to be called if multi-word blocks of data were to be received. The Transmit FIFO is in effect the Receive FIFO of the other DSP and is written directly by the transmitting DSP. The features of the XCHG are listed below.

- 10 Word XCHG Receive FIFO on both DSPs
- Four Flags for each XCHG for DSP to DSP signaling
- Condition flags can optionally trigger interrupts on both DSPs

DRAM/SRAM Interface (EMI)

The External DRAM/SRAM Interface is viewed as a memory mapped peripheral. Data transfers are performed by moving data into/from data registers and the control is exercised by polling status flags in the control/status register or by servicing interrupts. An external memory write is executed by writing data into the EMI Data Write Register. An external memory read operation is executed by either writing to the offset register or reading the EMI Data Read Register, depending on the configuration.

The features of the EMI are listed below.

- Data bus width fixed at 4 bits for DRAM and 8 bits for SRAM.
- Data word length 16 or 24 bits for DRAM.
- Data word length 8or 16 or 24 bits for SRAM.
- Thirteen DRAM address lines means 2^{26} = 32MB addressable DRAM.
- Refresh rate for DRAM can be chosen among eight divider factor.
- SRAM relative addressing mode; 2^{22} = 4MB addressable SRAM.
- Four SRAM Timing choices.
- Two Read Offset Registers.

Debug Interface

A dedicated Debug Port is available for each DSP Cores. The debug logic is contained in the core design of the DSP. The features of the Debug Port are listed below:

- Breakpoint Logic
- Trace Logic
- Single stepping
- Instruction Injection
- Program Disassembly

Serial Peripheral Interface

The DSP core requires a serial interface to receive commands and data over the LAN. During an SPI transfer, data is transmitted and received simultaneously. A serial clock line synchronizes shifting and sampling of the information on the two serial data lines. A slave select line allows individual selection of a slave SPI device.

When an SPI transfer occurs an 8-bit word is shifted out one data pin while another 8-bit character is simultaneously shifted in a second data pin.
The central element in the SPI system is the shift register and the read data buffer. The system is single buffered in the transfer direction and double buffered in the receive direction.

I^2C Interface

The inter Integrated Circuit bus is a single bidirectional two-wire bus used for efficient inter IC control. All I^2C bus compatible devices incorporate an on-chip interface which allows them communicate directly with each other via the I^2C bus.

Every component hooked up to the I^2C bus has its own unique address whether it is a CPU, memory or some other complex function chip. Each of these chips can act as a receiver and /or transmitter on its functionality.

General Purpose Input/Output

The DSP requires a set of external general purpose input/output lines, and a reset line. These signals are used by external devices to signal events to the DSP. The GPIO lines are implemented as DSP 's peripherals. The GPIO lines are grouped in Port A which is connected to DSP 0, and Port B, which is connected to DSP1.

PLL Clock Oscillator

The PLL Clock Oscillator can accept an external clock at XTI or it can be configured to run an internal oscillator when a crystal is connected across pins XTI & XTO. There is an input divide block IDF (1 -> 32) at the XTI clock input and a multiply block MF (9 -> 128) in the PLL loop. Hence the PLL can multiply the external input clock by a ratio MF/IDF to generate the internal clock. This allows the internal clock to be within 1 MHz of any desired frequency even when XTI is much greater than 1 MHz. It is recommended that the input clock is not divided down to less than 1 MHz as this reduces the Phase Detector's update rate.

The clocks to the DSP can be selected to be either the VCO output divided by 2 to 16, or be driven by the XTI pin directly.

The crystal oscillator and the PLL will be gated off when entering the power-down mode (by setting a register on DSP0).

Codec

The CODEC is composed of four AD mono converters, three DA stereo converters. The ADC can operate both in audio mode and in FM/AM mode. When in audio mode, it converts the audio bandwidth from 20 to 20KHz. The A to D is a third order Sigma-Delta converter, the converter resolutions is 20 bit with 93 dB of dynamic range and 85dB of total harmonic distortion. When in FM mode, the converted bandwidth is up to 192KHz. The D to A is a third order Sigma-Delta converter with a low noise reconstructing analog filter, the converter resolution is 20 bit with 93 dB of dynamic range and 85dB of total harmonic distortion. All the reference voltages are generated inside the chip.

Some capabilities of the CODEC are listed below:

- 20-Bit Resolution
- Digital Anti-Alias Filtering embedded
- Adjustable System Sampling Rates
- 93dB D/A Dynamic Range (A-Weighted)
  93dB A/D Dynamic Range (A-Weighted)
- 85dB D/A (THD+N/S)
  85dB A/D (THD+N/S)
- Internal Differential Analog Architecture
- +3.3V Power Supply

SOFTWARE FEATURES

A great flexibility is guaranteed by the two programmable DSP cores. A list of the main software functions which can be implemented in the TDA7500 is enclosed hereafter. A block diagram of the audio processing flow is shown in Fig. 1 below.

AM/FM Baseband Signal Processing

- FM weak signal processing
- Integrated 19 kHz MPX filter and deemphasis
- flexible noise cancellation
- flexible multipath detector

Generic Audio Signal Processsing

- Loudness
- Bass, treble, fader control
- Volume control
- Distortion Limiting
- Premium Equalization
- Soft mute

TAPE Signal Processsing

- Dolby B Noise Reduction
- Automatic Music Search

CD Signal Proceessing

- Dynamic Range Compression

Audiophile (optional)

- Parametric Equalization
- Crossover Patters
- Channel Delays
- Center Channel Imaging Output
- Audio Noise Reduction

Application Scheme

The TDA7500 can operate as a standalone device either it can interface the TDA7501 which contains the analog input multiplexer, analog volume control and the line-driver. The FM_MPX and FM_LEVEL signals coming from the tuner and other signals supplied by analog sources are adapted by the TDA7501 and fed to the TDA7500. A block diagram of the system is shown in Fig.2 below.

The TDA7500 converts all the analog signals into

digital domain and performs AM/FM processing and audio/sound processing. Thanks to this, it is possible to process any audio source as well analog as digital in parallel, to record FM mono for traffic information, telephone response, navigation and RDS. Finally the digital signals are D/A converted and sent to the TDA7501 for the final level adjustment and for the analog volume control.

Figure 1. Software Block Diagram of Audio & Sound Processing

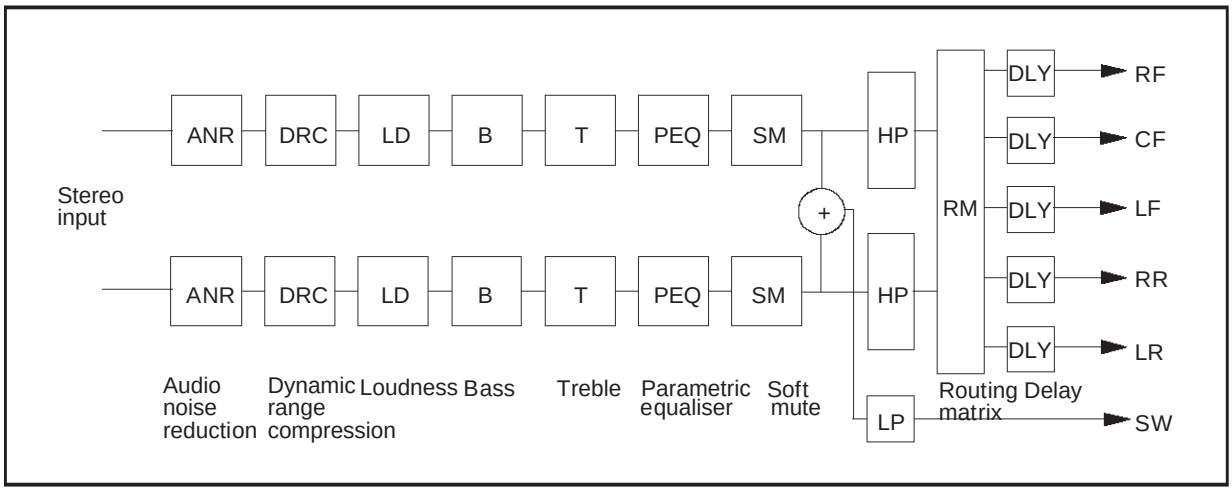
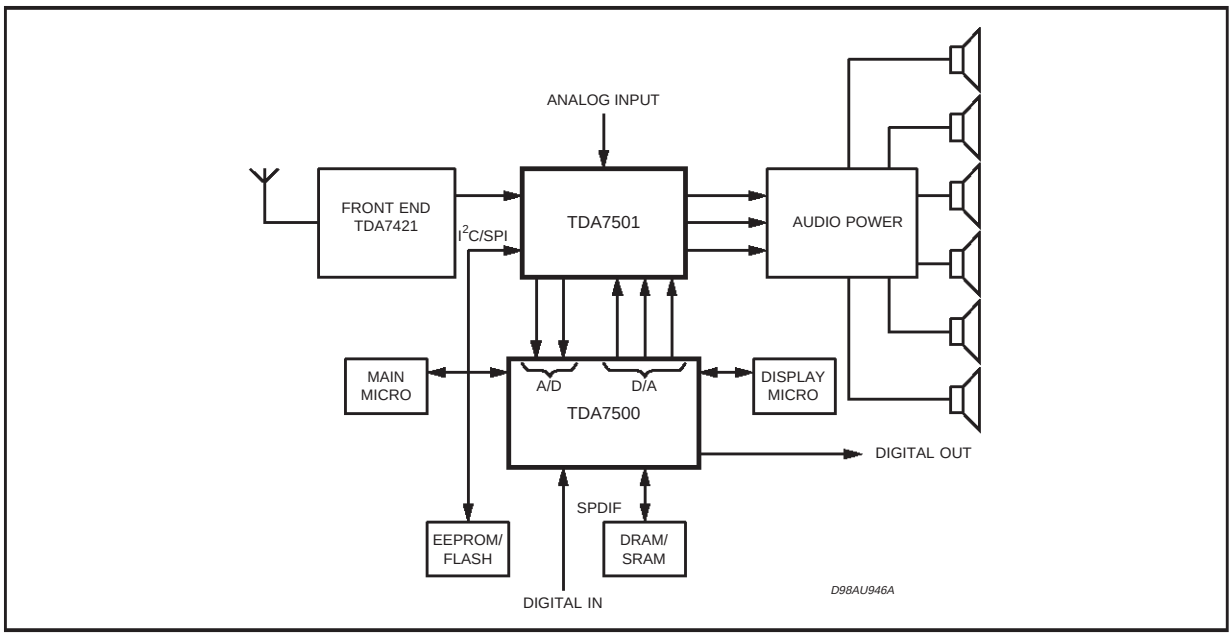
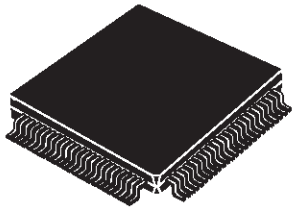


Figure 2. Block Diagram of Car Amplifier Audio Sub-System.



DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.17	0.22	0.27	0.007	0.009	0.011
C	0.09		0.20	0.003		0.008
D		16.00			0.630	
D1		14.00			0.551	
D3		12.00			0.472	
e		0.50			0.020	
E		16.00			0.630	
E1		14.00			0.551	
E3		12.00			0.472	
H		9.85			0.388	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
S	8.80			0.346		
S1	8.80			0.346		
K	0° (min.), 3.5° (typ.), 7°(max.)					
ccc		0.080			0.003	

OUTLINE AND MECHANICAL DATA



TQFP100 (14x14x1.40mm)
with Slug Down (10x10mm)