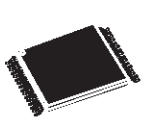
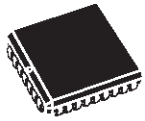
M29W512B

512 Kbit (64Kb x8, Bulk)
Low Voltage Single Supply Flash Memory

- SINGLE 2.7 to 3.6V SUPPLY VOLTAGE for PROGRAM, ERASE and READ OPERATIONS
- ACCESS TIME: 55ns
- PROGRAMMING TIME
  - 10µs per Byte typical
- PROGRAM/ERASE CONTROLLER
  - Embedded Byte Program algorithm
  - Embedded Chip Erase algorithm
  - Status Register Polling and Toggle Bits
- UNLOCK BYPASS PROGRAM COMMAND
  - Faster Production/Batch Programming
- LOW POWER CONSUMPTION
  - Standby and Automatic Standby
- 100,000 PROGRAM/ERASE CYCLES
- 20 YEARS DATA RETENTION
  - Defectivity below 1 ppm/year
- ELECTRONIC SIGNATURE
  - Manufacturer Code: 20h
  - Device Code: 27h



TSOP32 (NZ)
8 x 14mm



PLCC32 (K)

Figure 1. Logic Diagram

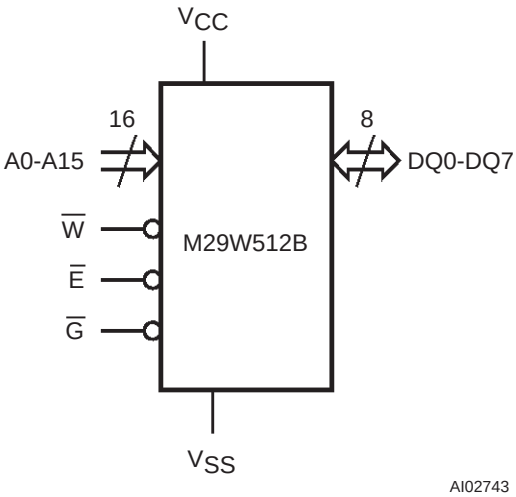


Figure 2. TSOP Connections

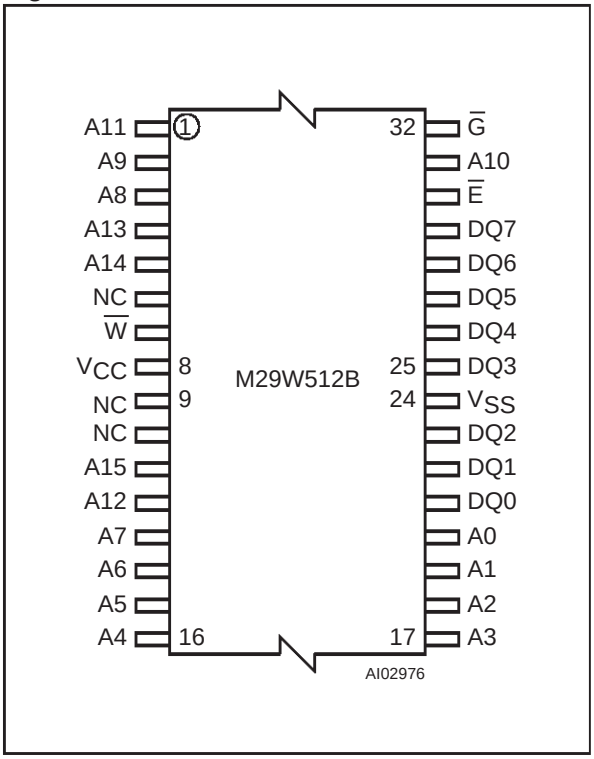


Figure 3. PLCC Connections

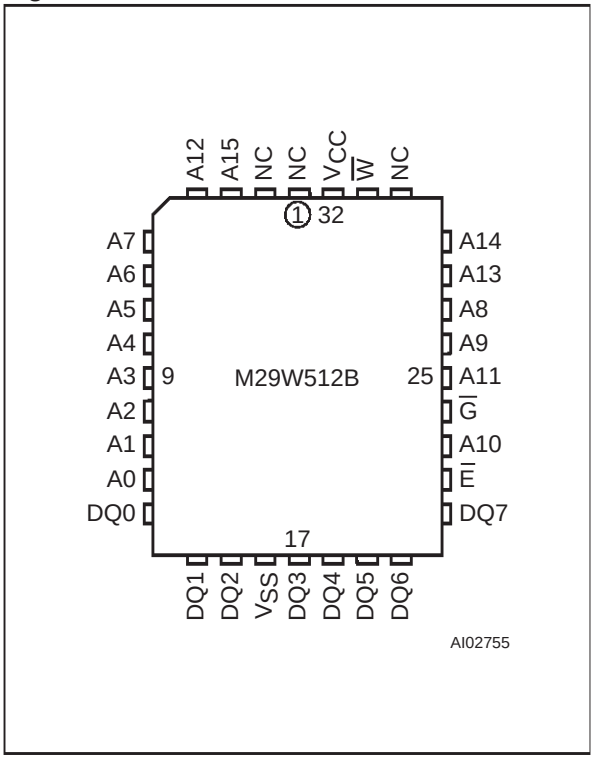


Table 1. Signal Names

A0-A15	Address Inputs
DQ0-DQ7	Data Inputs/Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground
NC	Not Connected Internally

SUMMARY DESCRIPTION

The M29W512B is a 512 Kbit (64Kb x8) non-volatile memory that can be read, erased and reprogrammed. These operations can be performed using a single low voltage (2.7 to 3.6V) supply. On power-up the memory defaults to its Read mode where it can be read in the same way as a ROM or EPROM.

Program and Erase commands are written to the Command Interface of the memory. An on-chip Program/Erase Controller simplifies the process of programming or erasing the memory by taking care of all of the special operations that are required to update the memory contents. The end of a program or erase operation can be detected and any error conditions identified. The command set required to control the memory is consistent with JEDEC standards.

Chip Enable, Output Enable and Write Enable signals control the bus operation of the memory. They allow simple connection to most microprocessors, often without additional logic.

The memory is offered in TSOP32 (8 x 14mm) and PLCC32 packages and it is supplied with all the bits erased (set to '1').

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltage	–0.6 to 4	V
V_{CC}	Supply Voltage	–0.6 to 4	V
V_{ID}	Identification Voltage	–0.6 to 13.5	V

Note: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.
2. Minimum Voltage may undershoot to –2V during transition and for less than 20ns during transitions.

SIGNAL DESCRIPTIONS

See Figure 1, Logic Diagram, and Table 1, Signal Names, for a brief overview of the signals connected to this device.

Address Inputs (A0-A15). The Address Inputs select the cells in the memory array to access during Bus Read operations. During Bus Write operations they control the commands sent to the Command Interface of the internal state machine.

Data Inputs/Outputs (DQ0-DQ7). The Data Inputs/Outputs output the data stored at the selected address during a Bus Read operation. During Bus Write operations they represent the commands sent to the Command Interface of the internal state machine.

Chip Enable ($\overline{E}$). The Chip Enable, $\overline{E}$, activates the memory, allowing Bus Read and Bus Write operations to be performed. When Chip Enable is High, V_{IH}, all other pins are ignored.

Output Enable ($\overline{G}$). The Output Enable, $\overline{G}$, controls the Bus Read operation of the memory.

Write Enable ($\overline{W}$). The Write Enable, $\overline{W}$, controls the Bus Write operation of the memory's Command Interface.

V_{CC} Supply Voltage. The V_{CC} Supply Voltage supplies the power for all operations (Read, Program, Erase etc.).

The Command Interface is disabled when the V_{CC} Supply Voltage is less than the Lockout Voltage, V_{LKO}. This prevents Bus Write operations from accidentally damaging the data during power-up, power-down and power surges. If the Program/Erase Controller is programming or erasing during this time then the operation aborts and the memory contents being altered will be invalid.

A 0.1µF capacitor should be connected between the V_{CC} Supply Voltage pin and the V_{SS} Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations, I_{CC3}.

Vss Ground. The V_{SS} Ground is the reference for all voltage measurements.

BUS OPERATIONS

There are five standard bus operations that control the device. These are Bus Read, Bus Write, Output Disable, Standby and Automatic Standby. See Table 3, Bus Operations, for a summary. Typically glitches of less than 5ns are ignored by the memory and do not affect bus operations.

Bus Read. Bus Read operations read from the memory cells, or specific registers in the Command Interface. A valid Bus Read operation involves setting the desired address on the Address Inputs, applying a Low signal, V_{IL}, to Chip Enable and Output Enable and keeping Write Enable High, V_{IH}. The Data Inputs/Outputs will output the value, see Figure 8, Read Mode AC Waveforms, and Table 10, Read AC Characteristics, for details of when the output becomes valid.

Bus Write. Bus Write operations write to the Command Interface. A valid Bus Write operation begins by setting the desired address on the Address Inputs. The Address Inputs are latched by the Command Interface on the falling edge of Chip Enable or Write Enable, whichever occurs last. The Data Inputs/Outputs are latched by the Command Interface on the rising edge of Chip Enable or Write Enable, whichever occurs first. Output Enable must remain High, V_{IH}, during the whole Bus Write operation. See Figures 9 and 10, Write AC Waveforms, and Tables 11 and 12, Write AC Characteristics, for details of the timing requirements.

Output Disable. The Data Inputs/Outputs are in the high impedance state when Output Enable is High, V_{IH}.

Standby. When Chip Enable is High, V_{IH}, the memory enters Standby mode and the Data Inputs/Outputs pins are placed in the high-impedance state. To reduce the Supply Current to the Standby Supply Current, I_{CC2}, Chip Enable should be held within $V_{CC} \pm 0.2V$. For the Standby current level see Table 9, DC Characteristics.

During program or erase operations the memory will continue to use the Program/Erase Supply Current, I_{CC3}, for Program or Erase operations until the operation completes.

Automatic Standby. If CMOS levels ($V_{CC} \pm 0.2V$) are used to drive the bus and the bus is inactive for 150ns or more the memory enters Automatic Standby where the internal Supply Current is reduced to the Standby Supply Current, I_{CC2}. The Data Inputs/Outputs will still output data if a Bus Read operation is in progress.

Special Bus Operations

Additional bus operations can be performed to read the Electronic Signature. These bus operations are intended for use by programming equipment and are not usually used in applications. They require V_{ID} to be applied to some pins.

Electronic Signature. The memory has two codes, the manufacturer code and the device code, that can be read to identify the memory. These codes can be read by applying the signals listed in Table 3, Bus Operations.

Table 3. Bus Operations

Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	Address Inputs	Data Inputs/Outputs
Bus Read	V_{IL}	V_{IL}	V_{IH}	Cell Address	Data Output
Bus Write	V_{IL}	V_{IH}	V_{IL}	Command Address	Data Input
Output Disable	X	V_{IH}	V_{IH}	X	Hi-Z
Standby	V_{IH}	X	X	X	Hi-Z
Read Manufacturer Code	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IL}, A1 = V_{IL}, A9 = V_{ID}, Others V_{IL} or V_{IH}	20h
Read Device Code	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IH}, A1 = V_{IL}, A9 = V_{ID}, Others V_{IL} or V_{IH}	27h

Note: X = V_{IL} or V_{IH}.

COMMAND INTERFACE

All Bus Write operations to the memory are interpreted by the Command Interface. Commands consist of one or more sequential Bus Write operations. Failure to observe a valid sequence of Bus Write operations will result in the memory returning to Read mode. The long command sequences are imposed to maximize data security.

The commands are summarized in Table 4, Commands. Refer to Table 4 in conjunction with the text descriptions below.

Read/Reset Command. The Read/Reset command returns the memory to its Read mode where it behaves like a ROM or EPROM. It also resets the errors in the Status Register. Either one or three Bus Write operations can be used to issue the Read/Reset command.

If the Read/Reset command is issued during a Chip Erase operation the memory will take about 10µs to abort the Chip Erase. During the abort period no valid data can be read from the memory. Issuing a Read/Reset command during a Chip Erase operation will leave invalid data in the memory.

Auto Select Command. The Auto Select command is used to read the Manufacturer Code and the Device Code. Three consecutive Bus Write operations are required to issue the Auto Select command. Once the Auto Select command is issued the memory remains in Auto Select mode until another command is issued.

From the Auto Select mode the Manufacturer Code can be read using a Bus Read operation with A0 = V_{IL} and A1 = V_{IL}. The other address bits may be set to either V_{IL} or V_{IH}. The Manufacturer Code for STMicroelectronics is 20h.

The Device Code can be read using a Bus Read operation with A0 = V_{IH} and A1 = V_{IL}. The other address bits may be set to either V_{IL} or V_{IH}. The Device Code for the M29W512B is 27h.

Program Command. The Program command can be used to program a value to one address in the memory array at a time. The command requires four Bus Write operations, the final write operation latches the address and data in the internal state machine and starts the Program/Erase Controller.

Table 4. Commands

Command	Length	Bus Write Operations											
		1st		2nd		3rd		4th		5th		6th	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read/Reset	1	X	F0										
	3	555	AA	2AA	55	X	F0						
Auto Select	3	555	AA	2AA	55	555	90						
Program	4	555	AA	2AA	55	555	A0	PA	PD				
Unlock Bypass	3	555	AA	2AA	55	555	20						
Unlock Bypass Program	2	X	A0	PA	PD								
Unlock Bypass Reset	2	X	90	X	00								
Chip Erase	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10

Note: X Don't Care, PA Program Address, PD Program Data.

All values in the table are in hexadecimal.

The Command Interface only uses address bits A0-A10 to verify the commands, the upper address bits are Don't Care.

Read/Reset. After a Read/Reset command, read the memory as normal until another command is issued.

Auto Select. After an Auto Select command, read Manufacturer ID or Device ID.

Program, Unlock Bypass Program, Chip Erase. After these commands read the Status Register until the Program/Erase Controller completes and the memory returns to Read Mode.

Unlock Bypass. After the Unlock Bypass command issue Unlock Bypass Program or Unlock Bypass Reset commands.

Unlock Bypass Reset. After the Unlock Bypass Reset command read the memory as normal until another command is issued.

During the program operation the memory will ignore all commands. It is not possible to issue any command to abort or pause the operation. Typical program times are given in Table 5. Bus Read operations during the program operation will output the Status Register on the Data Inputs/Outputs. See the section on the Status Register for more details.

After the program operation has completed the memory will return to the Read mode, unless an error has occurred. When an error occurs the memory will continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read mode.

Note that the Program command cannot change a bit set at '0' back to '1'. The Chip Erase command must be used to set all the bits in the memory from '0' to '1'.

Unlock Bypass Command. The Unlock Bypass command is used in conjunction with the Unlock Bypass Program command to program the memory. When the access time to the device is long (as with some EPROM programmers) considerable time saving can be made by using these commands. Three Bus Write operations are required to issue the Unlock Bypass command.

Once the Unlock Bypass command has been issued the memory will only accept the Unlock Bypass Program command and the Unlock Bypass Reset command. The memory can be read as if in Read mode.

Unlock Bypass Program Command. The Unlock Bypass Program command can be used to program one address in memory at a time. The command requires two Bus Write operations, the final write operation latches the address and data in the internal state machine and starts the Program/Erase Controller.

The Program operation using the Unlock Bypass Program command behaves identically to the Program operation using the Program command. The operation cannot be aborted and the Status Register is read. Errors must be reset using the Read/Reset command, which leaves the device in Unlock Bypass Mode. See the Program command for details on the behavior.

Unlock Bypass Reset Command. The Unlock Bypass Reset command can be used to return to Read/Reset mode from Unlock Bypass Mode. Two Bus Write operations are required to issue the Unlock Bypass Reset command.

Chip Erase Command. The Chip Erase command can be used to erase the memory. Six Bus Write operations are required to issue the Chip Erase Command and start the Program/Erase Controller.

All Bus Read operations during the Chip Erase operation will output the Status Register on the Data Inputs/Outputs. See the section on the Status Register for more details. Typical chip erase times are given in Table 5.

After the Chip Erase operation has completed the memory will return to the Read Mode, unless an error has occurred. When an error occurs the memory will continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read Mode.

The Chip Erase command sets all of the bits in the memory to '1'. All previous data is lost.

Table 5. Program, Erase Times and Program, Erase Endurance Cycles
(T_A = 0 to 70°C)

Parameter	Min	Typ (1)	Typical after 100k W/E Cycles (1)	Max	Unit
Chip Erase (All bits in the memory set to '0')		0.5	0.5		sec
Chip Erase		1	1	6	sec
Program		10	10	200	µs
Chip Program		0.7	0.7	4	sec
Program/Erase Cycles	100,000				cycles

Note: 1. T_A = 25°C, V_{CC} = 3.3V.

STATUS REGISTER

Bus Read operations from any address always read the Status Register during Program and Erase operations.

The bits in the Status Register are summarized in Table 6, Status Register Bits.

Data Polling Bit (DQ7). The Data Polling Bit can be used to identify whether the Program/Erase Controller has successfully completed its operation. The Data Polling Bit is output on DQ7 when the Status Register is read.

During Program operations the Data Polling Bit outputs the complement of the bit being programmed to DQ7. After successful completion of the Program operation the memory returns to Read mode and Bus Read operations from the address just programmed output DQ7, not its complement.

During Erase operations the Data Polling Bit outputs '0', the complement of the erased state of DQ7. After successful completion of the Erase operation the memory returns to Read Mode.

Figure 4, Data Polling Flowchart, gives an example of how to use the Data Polling Bit. A Valid Address is the address being programmed or any address while erasing the chip.

Toggle Bit (DQ6). The Toggle Bit can be used to identify whether the Program/Erase Controller has successfully completed its operation. The Toggle Bit is output on DQ6 when the Status Register is read.

During Program and Erase operations the Toggle Bit changes from '0' to '1' to '0', etc., with successive Bus Read operations at any address. After successful completion of the operation the memory returns to Read mode.

Figure 5, Data Toggle Flowchart, gives an example of how to use the Data Toggle Bit.

Error Bit (DQ5). The Error Bit can be used to identify errors detected by the Program/Erase Controller. The Error Bit is set to '1' when a Program or Chip Erase operation fails to write the correct data to the memory. If the Error Bit is set a Read/Reset command must be issued before other commands are issued. The Error bit is output on DQ5 when the Status Register is read.

Note that the Program command cannot change a bit set at '0' back to '1' and attempting to do so may or may not set DQ5 at '1'. In both cases, a successive Bus Read operation will show the bit is still '0'. The Chip Erase command must be used to set all the bits the memory from '0' to '1'.

Table 6. Status Register Bits

Operation	Address	DQ7	DQ6	DQ5
Program	Any Address	$\overline{DQ7}$	Toggle	0
Program Error	Any Address	$\overline{DQ7}$	Toggle	1
Chip Erase	Any Address	0	Toggle	0
Erase Error	Any Address	0	Toggle	1

Note: Unspecified data bits should be ignored.

Figure 4. Data Polling Flowchart

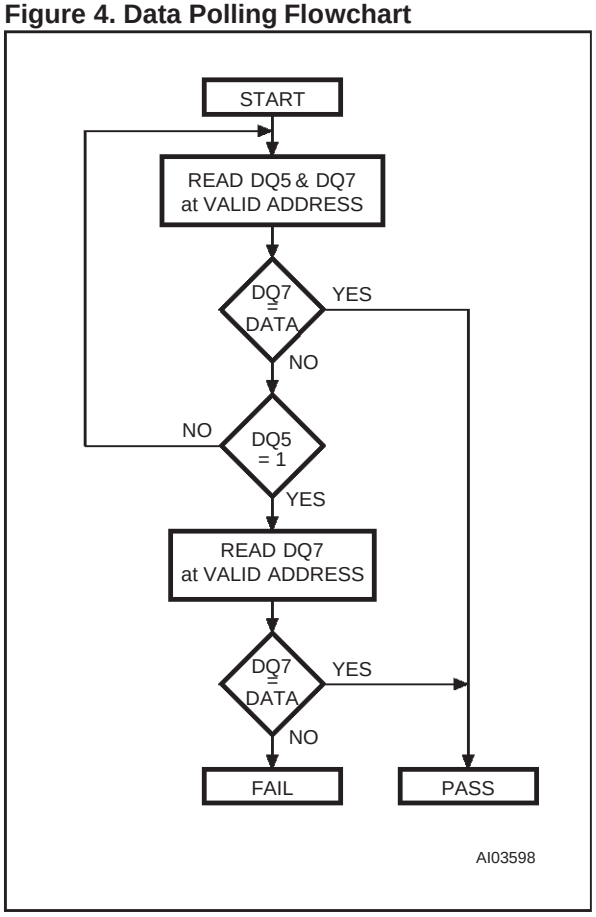


Figure 5. Data Toggle Flowchart

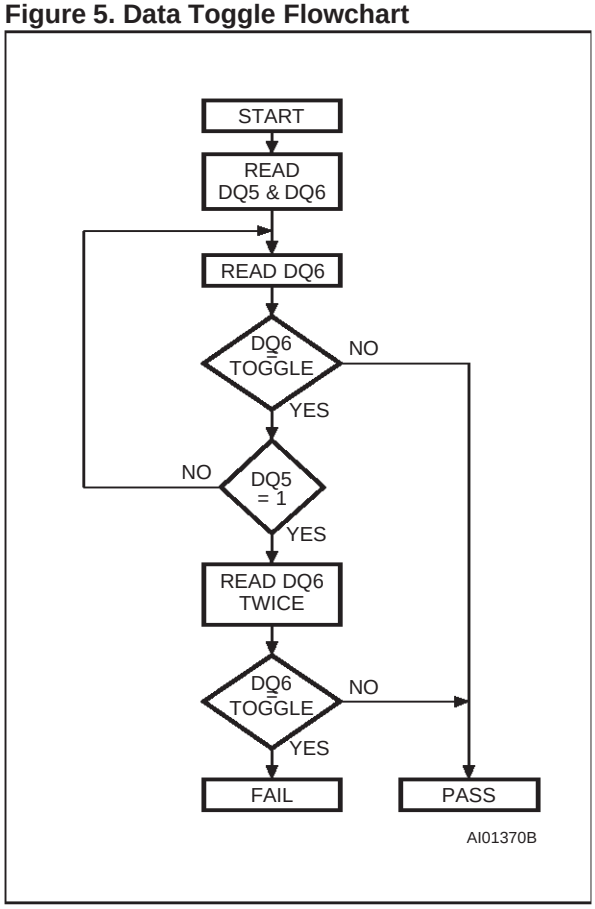


Table 7. AC Measurement Conditions

Parameter	M29W512B	
	55	70 / 90 / 120
V_{CC} Supply Voltage	3.0 to 3.6V	2.7 to 3.6V
Load Capacitance (C_L)	30pF	30pF
Input Rise and Fall Times	≤ 10ns	≤ 10ns
Input Pulse Voltages	0 to 3V	0 to 3V
Input and Output Timing Ref. Voltages	1.5V	1.5V

Figure 6. AC Testing Input Output Waveform

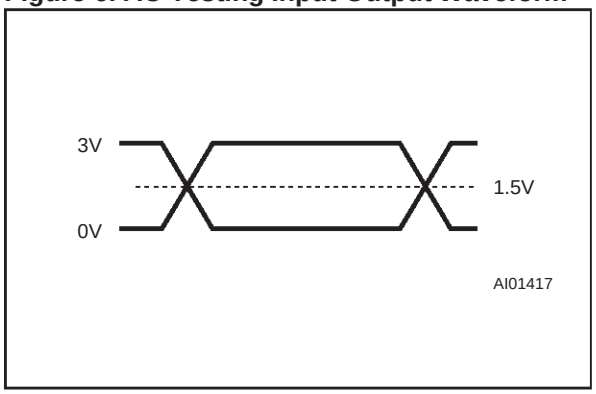


Figure 7. AC Testing Load Circuit

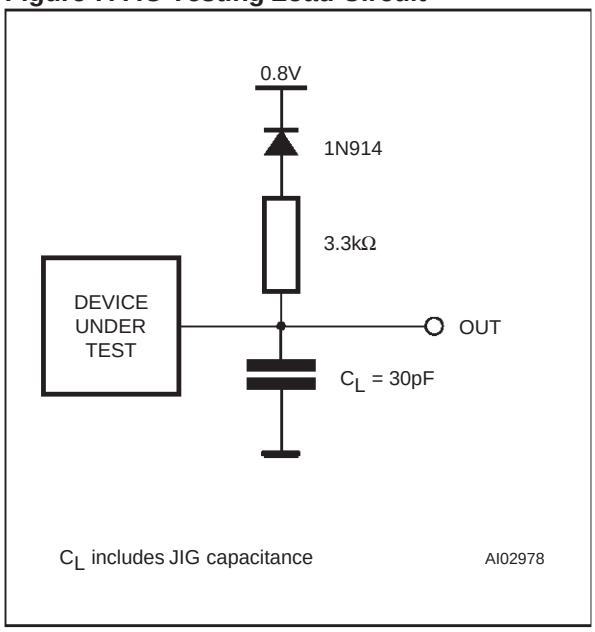


Table 8. Capacitance
(T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: Sampled only, not 100% tested.

Table 9. DC Characteristics
(T_A = 0 to 70°C)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±1	µA
I_{CC1}	Supply Current (Read)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$, f = 6MHz		10	mA
I_{CC2}	Supply Current (Standby)	$\overline{E} = V_{CC} \pm 0.2V$		100	µA
I_{CC3} (1)	Supply Current (Program/Erase)	Program/Erase Controller active		20	mA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 1.8mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –100µA	V_{CC} – 0.4		V
V_{ID}	Identification Voltage		11.5	12.5	V
I_{ID}	Identification Current	$A9 = V_{ID}$		100	µA
V_{LKO} (1)	Program/Erase Lockout Supply Voltage		1.8	2.3	V

Note: 1. Sampled only, not 100% tested.

Table 10. Read AC Characteristics
(TA = 0 to 70°C)

Symbol	Alt	Parameter	Test Condition		M29W512B			Unit
					55	70	90 / 120	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	Min	55	70	90	ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	Max	55	70	90	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	Min	0	0	0	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}	Max	55	70	90	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	Min	0	0	0	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}	Max	30	30	35	ns
t_{EHQZ} (1)	t_{HZ}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	Max	20	25	30	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	Max	20	25	30	ns
t_{EHQX} t_{GHQX} t_{AXQX}	t_{OH}	Chip Enable, Output Enable or Address Transition to Output Transition		Min	0	0	0	ns

Note: 1. Sampled only, not 100% tested.

Figure 8. Read Mode AC Waveforms

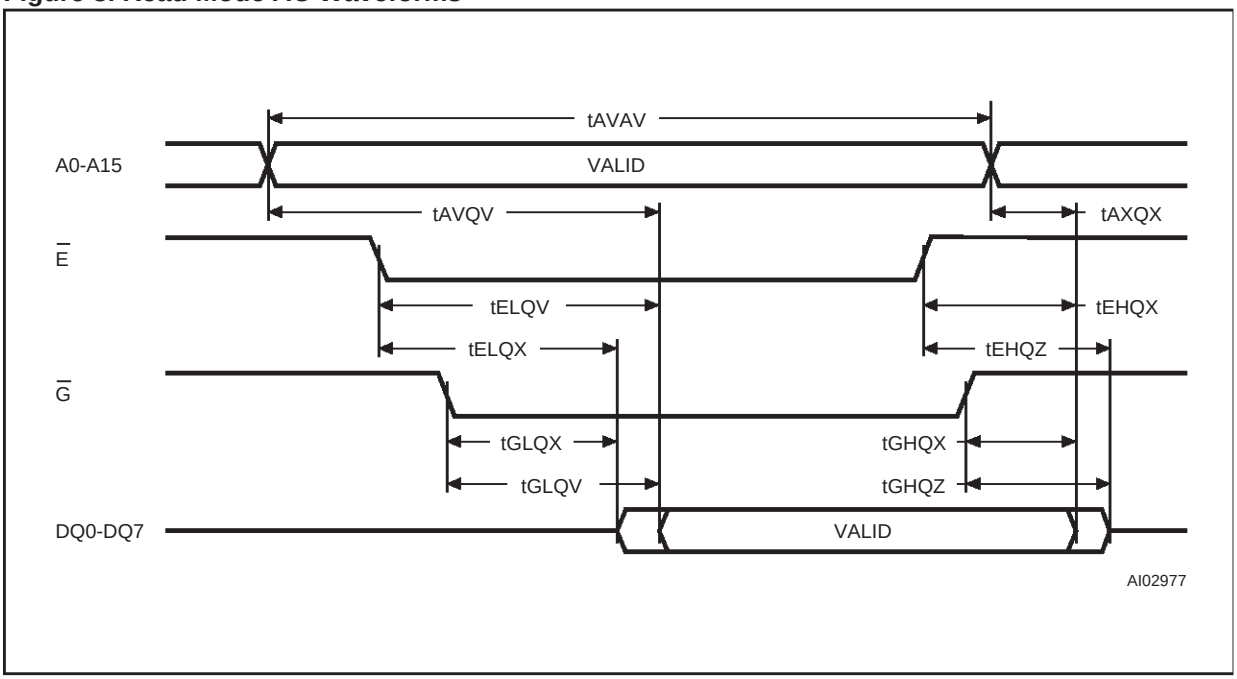


Table 11. Write AC Characteristics, Write Enable Controlled
(T_A = 0 to 70 °C)

Symbol	Alt	Parameter		M29W512B			Unit
				55	70	90 / 120	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	Min	55	70	90	ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	Min	0	0	0	ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	Min	40	45	45	ns
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	Min	25	30	45	ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	Min	0	0	0	ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	Min	0	0	0	ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	Min	30	30	30	ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	Min	0	0	0	ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	Min	40	45	45	ns
t_{GHWL}		Output Enable High to Write Enable Low	Min	0	0	0	ns
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low	Min	0	0	0	ns
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low	Min	50	50	50	µs

Figure 9. Write AC Waveforms, Write Enable Controlled

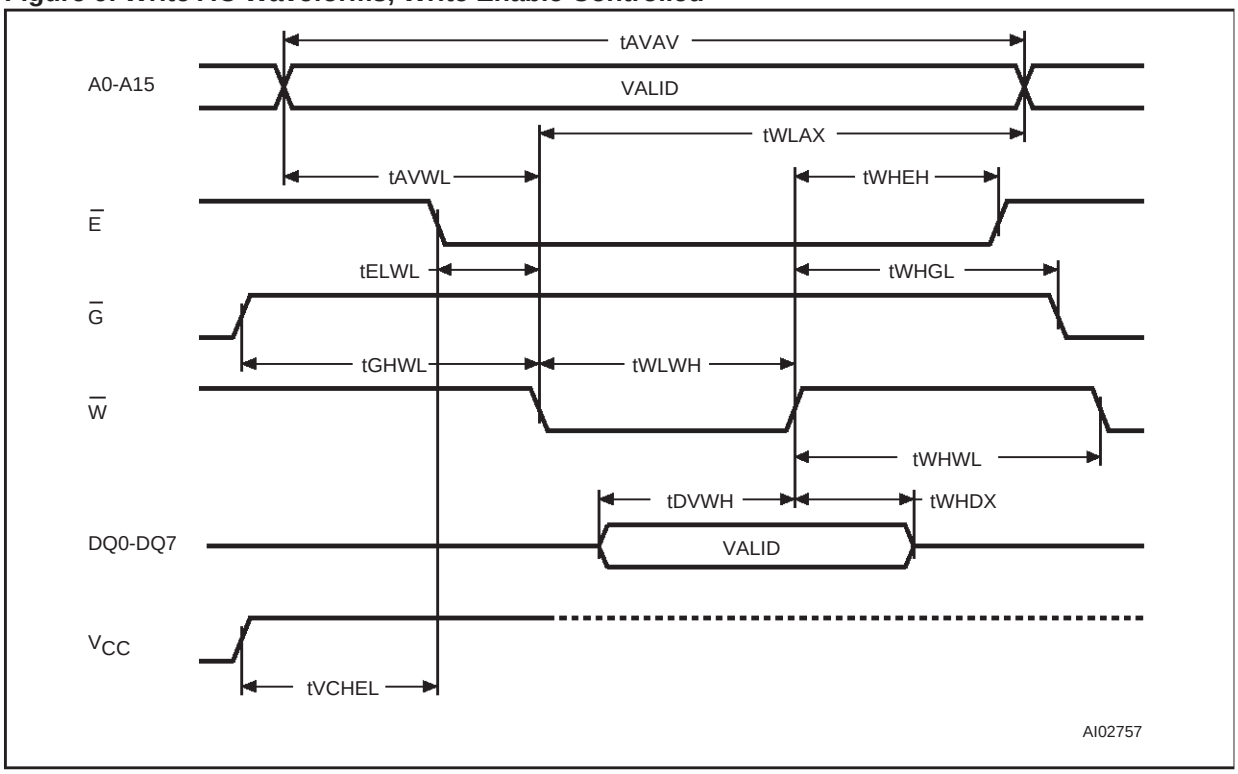


Table 12. Write AC Characteristics, Chip Enable Controlled
(T_A = 0 to 70 °C)

Symbol	Alt	Parameter		M29W512B			Unit
				55	70	90 / 120	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	Min	55	70	90	ns
t_{WLEL}	t_{WS}	Write Enable Low to Chip Enable Low	Min	0	0	0	ns
t_{ELEH}	t_{CP}	Chip Enable Low to Chip Enable High	Min	40	45	45	ns
t_{DVEH}	t_{DS}	Input Valid to Chip Enable High	Min	25	30	45	ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition	Min	0	0	0	ns
t_{EHWH}	t_{WH}	Chip Enable High to Write Enable High	Min	0	0	0	ns
t_{EHEL}	t_{CPH}	Chip Enable High to Chip Enable Low	Min	30	30	30	ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	Min	0	0	0	ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition	Min	40	45	45	ns
t_{GHEL}		Output Enable High Chip Enable Low	Min	0	0	0	ns
t_{EHGL}	t_{OEH}	Chip Enable High to Output Enable Low	Min	0	0	0	ns
t_{VCHWL}	t_{VCS}	V_{CC} High to Write Enable Low	Min	50	50	50	µs

Figure 10. Write AC Waveforms, Chip Enable Controlled

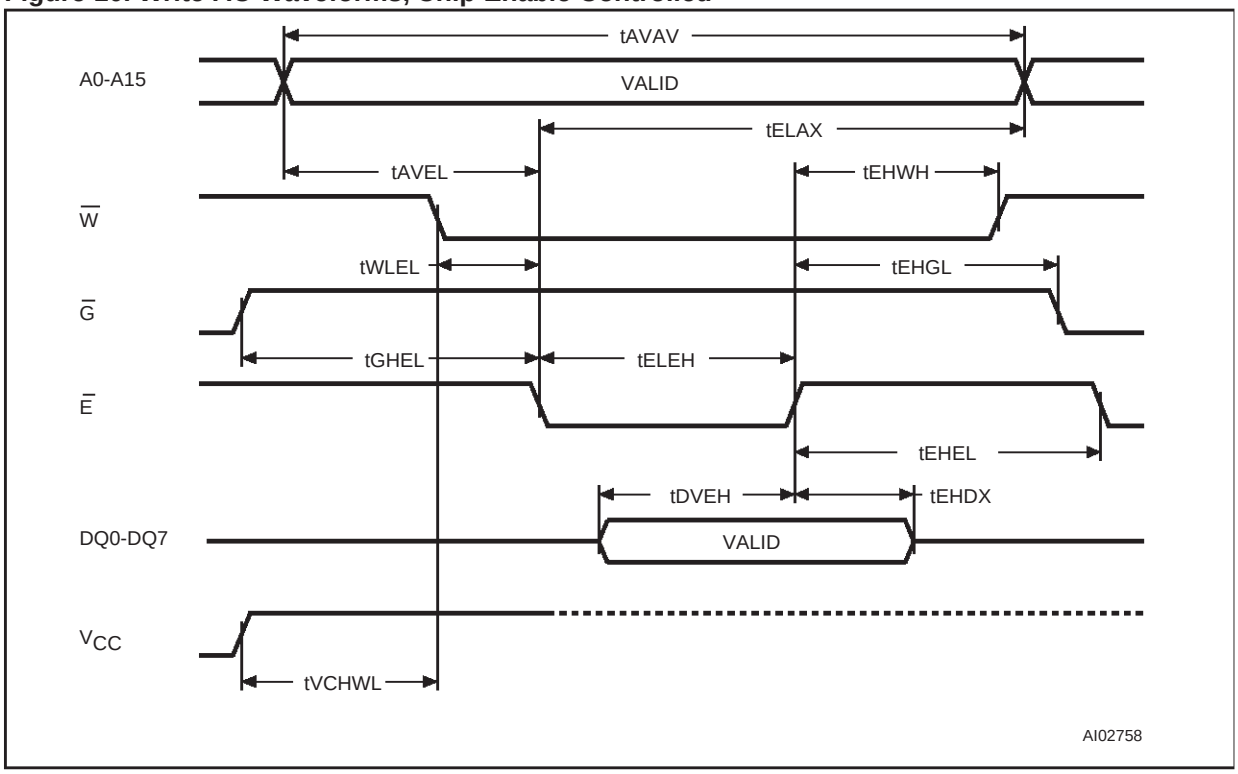
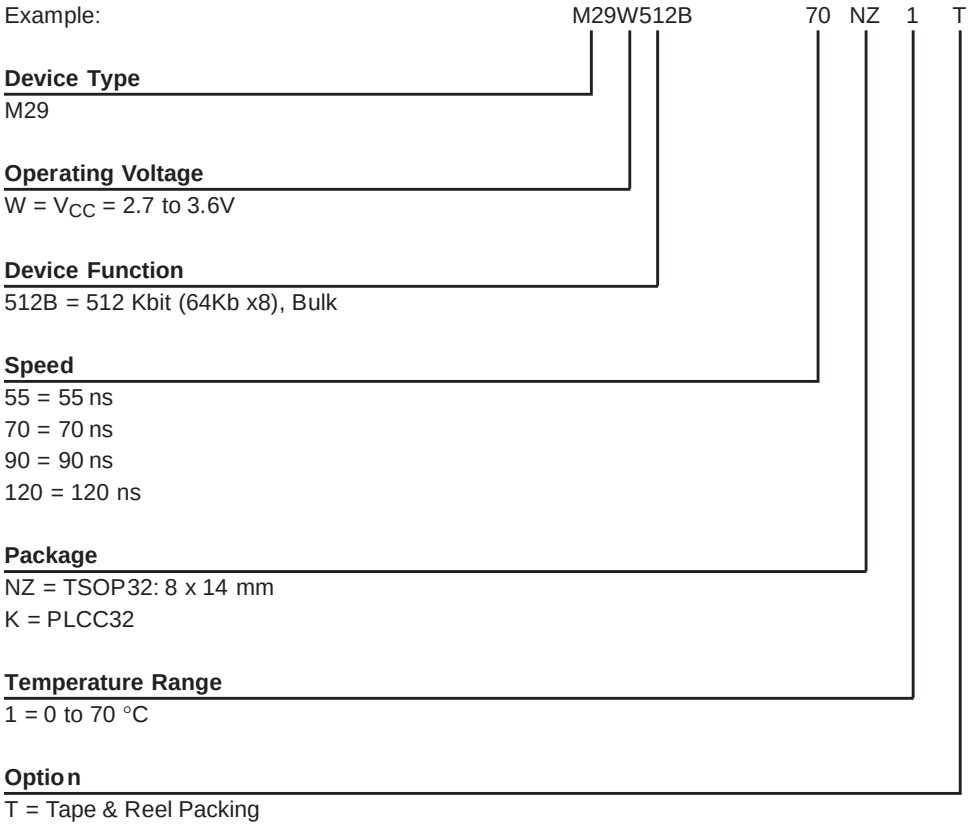


Table 13. Ordering Information Scheme



Note: The last two characters of the ordering code may be replaced by a letter code for preprogrammed parts, otherwise devices are shipped from the factory with the memory content bits erased to '1'.

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

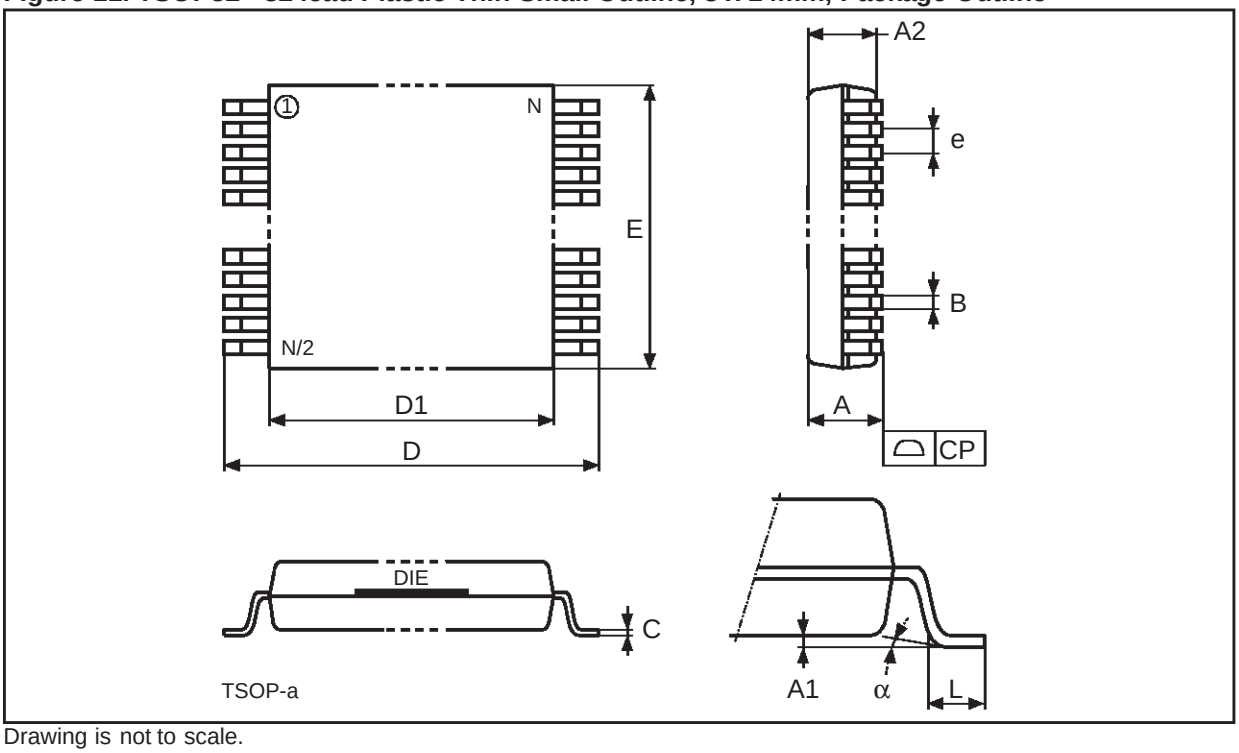
Table 14. Revision History

Date	Revision Details
July 1999	First Issue
03/09/00	Document type: from Preliminary Data to Data Sheet Status Register bit DQ5 clarification Data Polling Flowchart diagram change (Figure 4) Data Toggle Flowchart diagram change (Figure 5)

Table 15. TSOP32 - 32 lead Plastic Thin Small Outline, 8 x 14mm, Package Mechanical Data

Symbol	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.0472
A1		0.05	0.15		0.0020	0.0059
A2		0.95	1.05		0.0374	0.0413
B		0.17	0.27		0.0067	0.0106
C		0.10	0.21		0.0039	0.0083
D		13.80	14.20		0.5433	0.5591
D1		12.30	12.50		0.4843	0.4921
E		7.90	8.10		0.3110	0.3189
e	0.50	–	–	0.0197	–	–
L		0.50	0.70		0.0197	0.0276
α		0°	5°		0°	5°
N	32			32		
CP			0.10			0.0039

Figure 11. TSOP32 - 32 lead Plastic Thin Small Outline, 8 x 14mm, Package Outline

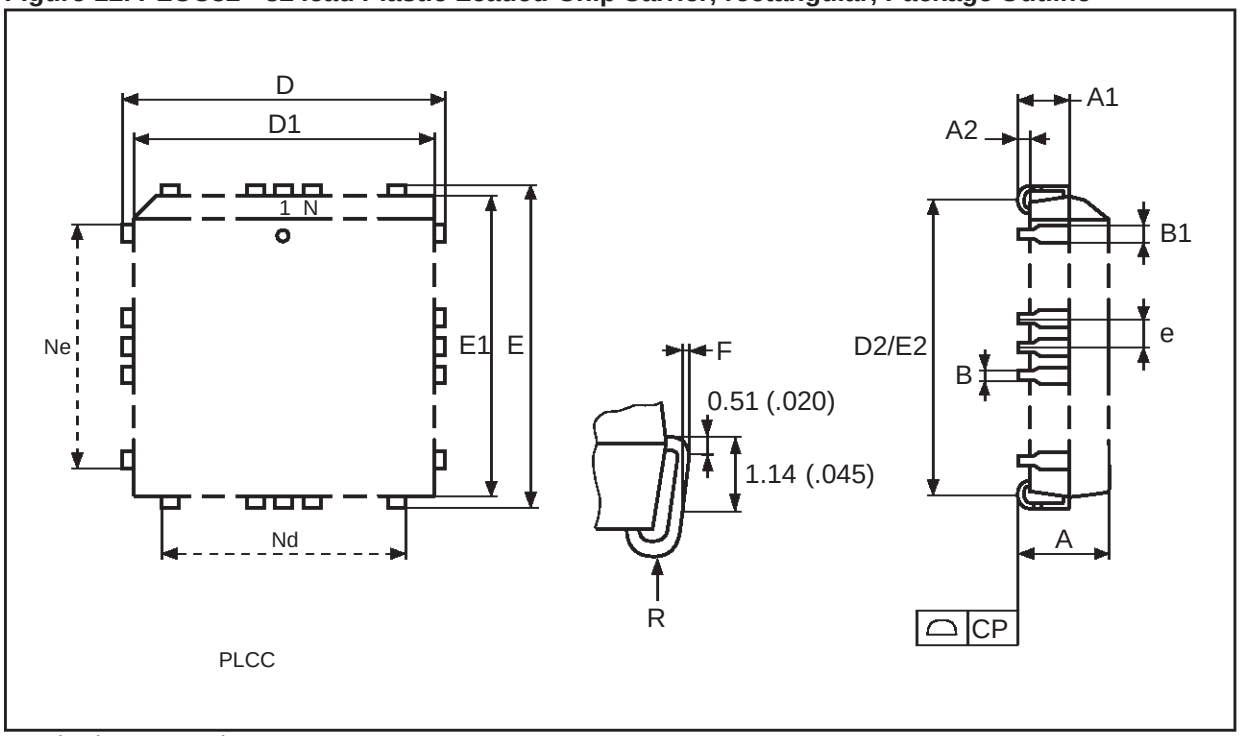


Drawing is not to scale.

Table 16. PLCC32 - 32 lead Plastic Leaded Chip Carrier, rectangular, Package Mechanical Data

Symbol	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.54	3.56		0.1000	0.1402
A1		1.52	2.41		0.0598	0.0949
A2			0.38			0.0150
B		0.33	0.53		0.0130	0.0209
B1		0.66	0.81		0.0260	0.0319
D		12.32	12.57		0.4850	0.4949
D1		11.35	11.56		0.4469	0.4551
D2		9.91	10.92		0.3902	0.4299
E		14.86	15.11		0.5850	0.5949
E1		13.89	14.10		0.5469	0.5551
E2		12.45	13.46		0.4902	0.5299
e	1.27	–	–	0.0500	–	–
F		0.00	0.25		0.0000	0.0098
R	0.89	–	–	0.0350	–	–
N	32			32		
Nd	7			7		
Ne	9			9		
CP			0.10			0.0039

Figure 12. PLCC32 - 32 lead Plastic Leaded Chip Carrier, rectangular, Package Outline



Drawing is not to scale.