AN1133
APPLICATION NOTE

90W SMPS FOR MONITORS WITH CONSTANT POWER LIMITING FUNCTION

by Claudio Adragna

Purpose of this note is to provide a brief summary of the specifications and the functionality of the application board implementing a 90W multioutput SMPS for multisynch monitors, based on the L5993, current mode PWM controller with "Constant Power" function.

Evaluation results are also presented so as to underline the benefits offered by the L5993 in such kind of SMPS where the wide range of operating frequency may cause the power throughput to far exceed the rated value under overload conditions.

Design Specifications

Table 1 summarises the electrical specification of the application. The complete electrical schematic is shown in fig. 1 and the bill of material is listed in Table 2.

Table 1. Design Specification

Input Voltage Range (V_{in})		88 to 264 Vac
Mains Frequency (f_L)		50/60 Hz
Maximum Output Power (P_{out})		90W
Outputs	Horizontal Deflection	V_{out} = 200V
		I_{out} = 0.325A
		Full load ripple = 1%
	Video Amplifier	V_{out} = 80V
		I_{out} = 0.125A
		Full load ripple = 1%
	Vertical Deflection	V_{out} = ±15V
		I_{out} = 0.33A
		Full load ripple = 1%
	Heater	V_{out} = 6.3V
		I_{out} = 0.8A
		Full load ripple = 2%
Switching Frequency in Normal Mode (f_{synch})		31 to 82kHz
Switching Frequency in Suspend / OFF mode (f_{osc})		21kHz
Target Efficiency (@ Pout =90W, Vin =88 ÷264 Vac) (η)		> 80%
Maximum Input Power (@ Pout = 0.5 W, Vin =88 ÷ 264 Vac)		≤ 2W

The selected topology is flyback. The operation mode (@ Pout = 90W) is either CCM (Continuous Conduction Mode) or DCM (Discontinuous Conduction Mode), depending on the synchronisation frequency and on the mains voltage. Since duty cycles greater than 50% are possible at low mains voltage, slope compensation has been provided to prevent subharmonic oscillations.

The application will benefit from the features of the L5993 PWM controller to provide an effective overpower protection over the entire operating frequency range. Without L5993's "Constant Power" function, if a load failure occurring when the system works at 31 kHz lets, say, 30% more power than the rated load pass, the power in excess may be 150% for a load failure occurring when the system works at 82 kHz. This would require a much more conservative design, with a considerable increase of size and cost of the whole power section of the SMPS. As shown also by the experimental results, this problem is completely solved with the ”Constant Power” functionality of the L5993.

Figure 1. 90W SMPS for Multisynch Monitors Electrical Schematic

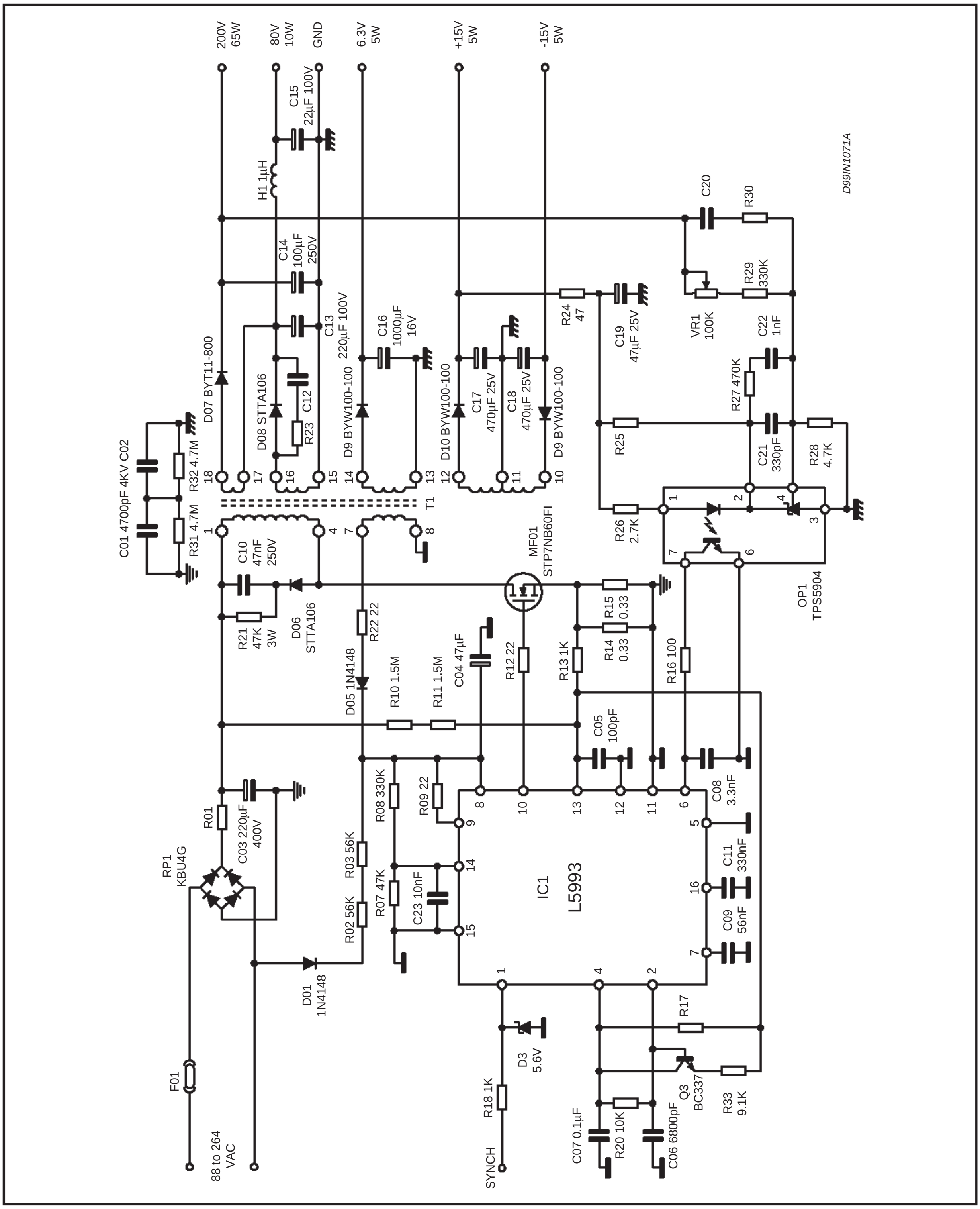


Table 2. Component List of the circuit of fig. 1.

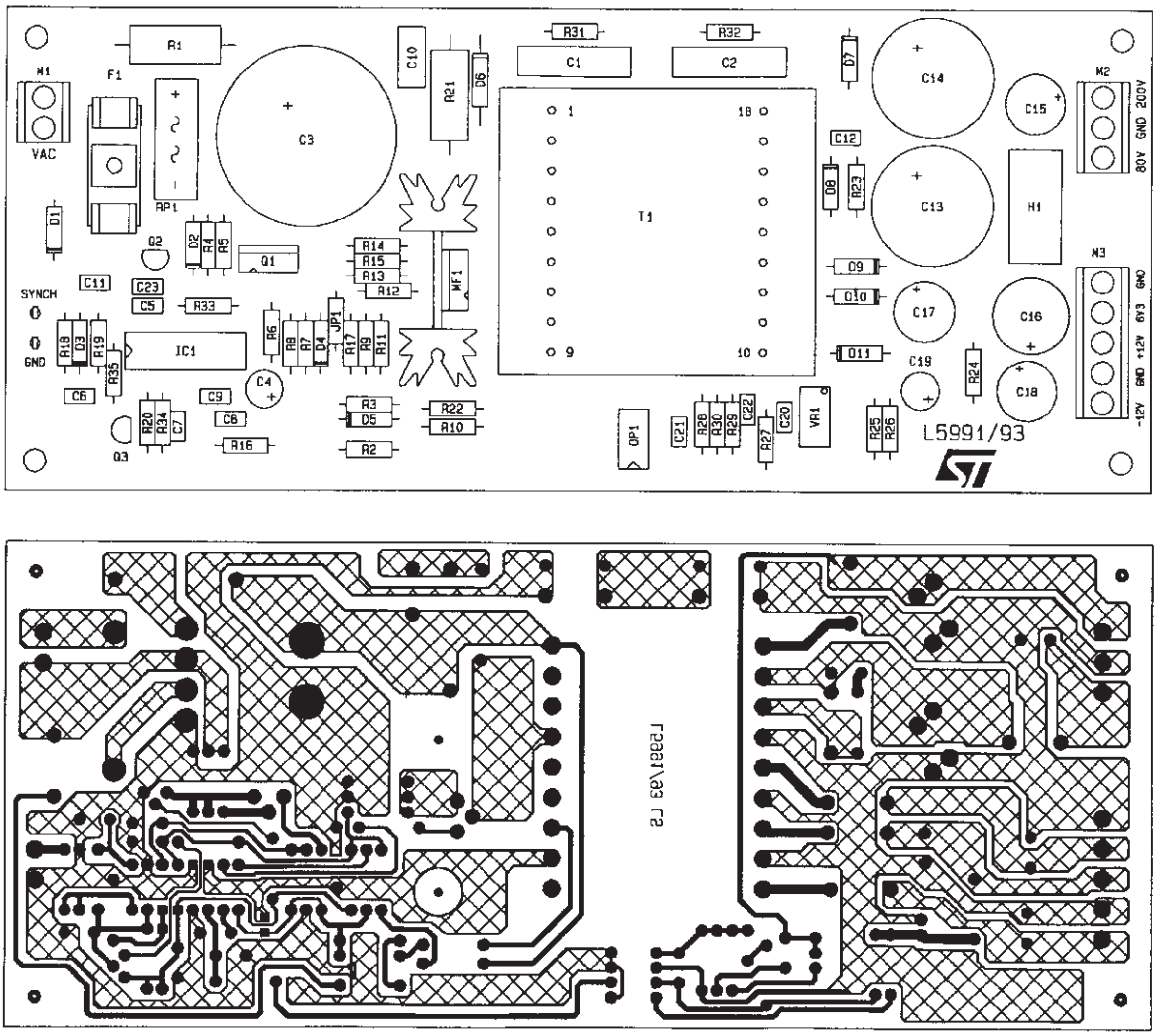
Symbol	Value	Note
R1		NOT USED (shorted)
R2, R3	56kΩ	
R7	47kΩ	
R8, R29	330kΩ	
R9, R12, R22	22Ω	
R10, R11	1.5MΩ	
R13, R18	1kΩ	
R14, R15	0.33Ω	metallic film
R16	100Ω	
R20	10kΩ	
R21	47kΩ	3W
R24	47Ω	
R26	2.7kΩ	
R27	470kΩ	
R28	4.7kΩ	
R31, R32	4.7MΩ	
R33	9.1kΩ	
VR1	100kΩ	multiturns, Bourns 3296W or equivalent
C1, C2	4.7nF	1kV
C3	220µF	400V, electrolytic, Panasonic TSUP or Roederstein EYS
C4, C19	47µF	25 V, electrolytic
C5	100pF	plastic film
C6	6.8nF	ceramic multilayer
C7	100nF	plastic film
C8	3.3nF	plastic film
C9	56nF	plastic film
C10	47nF	250V, polypropylene o polystyrene film (Siemens-Matsushita)
C11	330nF	plastic film
C13	220µF	100 V electrolytic, Roederstein EKE or equivalent
C14	100µF	250 V, electrolytic, Roederstein EKS or equivalent
C15	22µF	100 V, electrolytic, Roederstein EKE or equivalent
C16	1000µF	16V, electrolytic, Panasonic FA or equivalent
C17, C18	470µF	25 V, electrolytic, Panasonic HFZ or equivalent
C21	330pF	ceramic or plastic film
C22	1nF	ceramic or plastic film
C23	10nF	plastic film
D1, D5	1N4148	
D3	5.6V	Zener, 1/4 W
D6, D8	STTA106	ST, TurboSwitch
D7	BYT11-800	ST, Ultrafast
D9, D10, D11	BYW100-100	ST, Ultrafast
IC1	L5993	ST
T1	ETD4407	ITACOIL, see Table 3
OP1	TPS5904	TI
MF1	STP7NB60FI	ST
RP1	KBU4G	GI, or equivalent 4A rectifier bridge
Q3	BC337	
F1		5A fuse
H1	1µH	axial inductor
M1, M2, M3		connectors

Notes: - if not otherwise specified, all resistors are 1/4 W, 1%
- the MOSFET is provided with a 9.5 °C/W heatsink
- components indicated in the PCB and not quoted in table 2 are not assembled

Table 3. Transformer Specification (Part Number ETD4407, supplied by ITACOIL).

Core	Philips ETD44, 3C85 Material				
Bobbin	Horizontal mounting, 18 pins				
Air gap	≅ 1 mm for an inductance 1-4 of 380 µH				
Leakage inductance	< 10µH				
Windings Spec & Build	Winding	Wire	S-F	Turns	Notes
	Pri1	4xAWG29	2-4	19	
	Sec1	AWG25	17-18	48	
	Sec2	AWG25	15-16	32	
	Sec3	AWG25	13-14	3	Evenly spaced
	Sec4	AWG25	11-12	6	Bifiliar with Sec5
	Sec5	AWG26	10-11	6	Bifiliar with Sec4
	Pri2	4xAWG29	1-2	19	
	Aux	AWG29	8-7	8	Evenly spaced

Figure 2. PCB layout: Component side and bottom layer (top view); 1:1.33 scale



Application Board Functionality

The outstanding feature of this application board is the so-called Constant Power function, directly available from the L5993. The power capability of the converter has a strong dependence on the operating switching frequency: the overcurrent protection (pulse-by-pulse current limitation) does limit the peak primary current to a fixed value, but not the associated power throughput, which increases almost proportionally with the switching frequency. To achieve an effective overpower protection under all operating conditions, the L5993 automatically reduces the overcurrent protection setpoint when the switching frequency increases (and vice versa) so as to maintain the power throughput nearly constant in case of overload. The benefit is quite obvious: the designer will no longer be forced, for the sake of safety, to size the power stage of their SMPS considering a worst case heat dissipation relevant to a power level two or three times the rated load.

R10 and R11 provide a DC offset on L5993's current sense pin (13, ISEN), which depends on the supply input voltage with the aim of compensating L5993's delay to output. This reduces the increase of the overpower limit with the mains voltage. Actually there is an additional contribution from the slope compensation circuit (Q3 and R33), which adds a little offset (variable with the duty cycle) on the current sense pin as well.

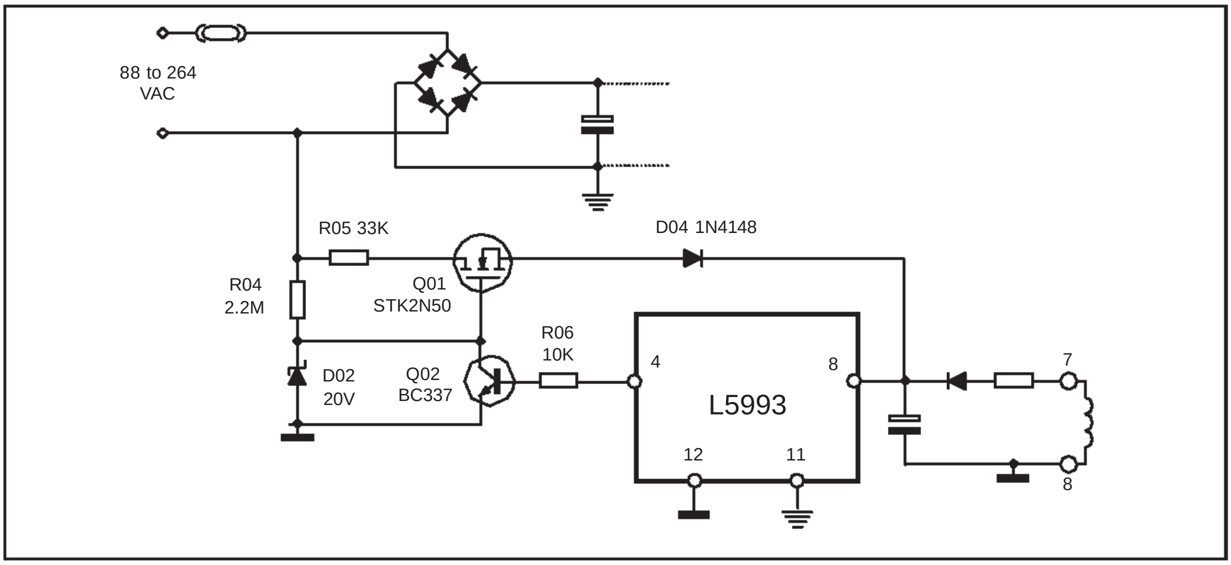
If the user would like to slightly adjust the way the overpower limit changes with frequency, he or she can add a further (fixed) DC offset (typically in the range 0-200 mV) on the current sense. This can be accomplished by means of R17, currently not used. The offset will be the partition of the reference voltage (pin 4, VREF) through R17 and R13.

A protection against output overvoltages (OVP) is available. It is realised by sensing the supply voltage of the L5993 (generated by the auxiliary winding and tracking the output voltage) through the divider R7-R8 and feeding this partition into pin 14 (DIS). The divider ratio is such that the OVP is tripped when the supply voltage exceeds 20V. This protection is particularly effective in case of feedback disconnection.

The new generation of SMPS for monitors is required to feature superior efficiency under light load conditions (SUSPEND and OFF modes) so as to be compliant with emerging standards concerning energy saving. High efficiency at light load is ensured by a low switching frequency (when the synch signal coming from the horizontal deflection circuits is missing the system works at the free-running frequency of the oscillator, set at 21 kHz) and by the low start-up and quiescent currents featured by the L5993. The low operating frequency minimises all losses related to switching, while the low consumption of the device minimises the power dissipated by the start-up and self-supply circuits.

The application board is supplied with a start-up circuit simply made of a dropping resistor (R2+R3) that draws current from upstream the bridge rectifier.

Figure 3 - Low-consumption start-up circuit (not currently implemented)



This circuit, really inexpensive, dissipates about 300 mW @ 264 Vac. The typical wake-up time is 2.8 s at 88 Vac and 0.8 s at 264 Vac. Should the wake-up time become an issue, a more expensive solution would be adopted. The PCB is also able to accommodate an active start-up circuit that, under the same conditions, dissipates less than 10 mW and provides 0.7 s and 0.2 s wake-up time respectively. The schematic is shown in fig. 3 (R2 and R3 will be removed).

A further improvement of light load efficiency could be achieved by replacing the RCD clamp (C10, R21) with a Transil. The suggested part is a 1.5KE150A. This slightly worsens efficiency at full load but allows to save about 200 mW, currently dissipated on R21, at light load.

At maximum load and minimum mains voltage the converter operates at about 55% duty cycle but no limitation is imposed on its maximum value: L5993's pin 3 (DC) is shorted to pin 4 (VREF). If desired, it is possible to set the maximum duty cycle by adding the divider R34-R35. Please refer to *Application Information* in L5993's datasheet for calculation of the voltage divider.

Application board evaluation: getting started

The AC input voltage, coming from an AC source ranging from 88 VRMS to 264 VRMS, will be applied to connector M1 (close to the top left-hand corner). The synchronisation signal (3.5 to 25V amplitude, 31 to 82 kHz frequency) will be applied between the "synch" and "gnd" pads, located on the left side of the PCB. The 200 VDC and 80 VDC outputs are located in connector M2 (top right-hand corner) while ±15 VDC and 6.3 VDC outputs are available at connector M3, near the bottom right-hand corner.

Full load applied when the synchronisation signal is missing will cause the system to go into overcurrent protection.

Like in any off-line circuit, extreme caution must be used when working with the application board because it contains dangerous and lethal potentials. The application must be tested with an isolation transformer connected between the AC mains and the input of the board to avoid any risk of electrical shock.

Application board evaluation: results

The following tables summarise some results of the bench evaluation.

Table 4. Full load measurements (f_{synch} = 31kHz)

V_{AC} [V]	88	110	160	220	264
Pin [W]	102.9	101.2	99.3	98.5	98.3
Vout [V]	199.6	199.6	199.6	199.6	199.6
	79.51	79.5	79.49	79.48	79.48
	14.32	14.31	14.3	14.29	14.3
	-14.42	-14.41	-14.4	-14.39	-14.39
	6.55	6.55	6.55	6.55	6.55
Pout [W]	89.56	89.55	89.53	88.43	88.43
η [%]	87	88.5	90.2	90.8	91
Load conditions: 200V: 0.325A; 80V: 600Ω; ±15V: 94Ω; 6.3V: 8Ω					

Table 5. Full load measurements (f_{synch} = 82kHz)

V_{AC} [V]	88	110	160	220	264
Pin [W]	102.3	100.2	98.9	98.5	98.2
Vout [V]	199.6	199.6	199.6	199.6	199.6
	79.35	79.42	79.42	79.42	79.4
	14.32	14.31	14.3	14.29	14.3
	-14.4	-14.41	-14.4	-14.39	-14.39
	6.58	6.63	6.65	6.65	6.63
Pout [W]	89.6	89.64	89.69	88.67	88.63
η [%]	87.6	89.5	90.7	91	91.3
Load conditions: 200V: 0.325A; 80V: 600Ω; ±15V: 94Ω; 6.3V: 8Ω					

Table 6. Consumption from the mains in Suspend mode (P_O = 5.5W)

V_{AC} [V]	88	110	160	220	264
Pin [W]	6.9	7	7	7.1	7.2
Load conditions: 200V: open; 80V: open; ±15V: 0.5W; 6.3V: 8Ω					

Table 7. Consumption from the mains in OFF mode (P_O = 0.5W)

V_{AC} [V]	88	110	160	220	264
Pin [W]	1.3	1.4	1.5	1.6	1.8
Pin [W] (*)	1.2	1.2	1.3	1.4	1.5
Load conditions: 200V: open; 80V: open; +15V: 0.5W; 6.3V: open (*) With the active start-up circuit of fig.3					

Table 8. Overpower limit

f_{synch} [kHz]		31	48	64	82
Pin [W]	V_{AC} = 88V	129	126	122	120
	V_{AC} = 160V	129	129	131	132
	V_{AC} = 264V	128	121	124	127
Overload conditions: 200V: 0.6A; other outputs loads: 80V: 600Ω; ±15V: 94Ω; 6.3V: 8Ω					

APPENDIX

Low-consumption modes management

The application board is not provided with the circuits that handle the loads in a monitor SMPS during Suspend and OFF modes. As a result, if the board is connected to a monitor unit "as is", the consumption from the mains will be significantly higher than the values shown in tables 6 and 7. In particular, it will not be possible to meet the "less than 3W" specification required by the current energy saving regulations in OFF mode.

This happens because the monitor's circuits, in particular those connected to the high voltage buses, are still powered and have some mA residual consumption, despite they are not operating. The actual load is then heavier than the one assumed in table 6 and 7, where the load conditions in OFF-mode are simulated, provided some "power management" circuit takes care of their reduction.

A popular solution used for cutting down the residual loads and minimize the power consumption in OFF mode is to reduce 8 to 10 times the voltage of all of the outputs, except the one that powers the µP governing the entire monitor operation, power management included.

In this way the voltage produced by the SMPS will not be enough to power monitor's circuits and their consumption will drop to zero. Additionally, the reflected voltage during switch OFF-time will be much lower, which will reduce switching and capacitive losses.

The above mentioned functionality can be achieved in a number of different ways. Figure A1 shows the application board schematic modified with the addition of a circuit (pointed out by the shaded areas) that does the job. A 5V linear regulator (L7805CP), which is supposed to supply the µP, has been added for completeness. The operation of the circuit can be described as follows.

When the OFF signal is pulled high, Q5 is turned on, the base of Q4 is grounded and Q4 is turned on as well. This connects the 80V winding and the 2.2µF capacitor, charged at 80V, to C17+C19 charged at 15V. Being the latter much bigger, the transient voltage change is negligible. The 4.7Ω resistor in series to Q4's emitter limits the current surge during the transient.

By turning Q5 on, the cathode of the TL431, typically at 11V in normal operation, is now forced to drop at about 4V by the 3.3V zener and the decoupling diode. Considering 1V drop across the photodiode and the drop on R26, which changes very little, the voltage on C17+C19 will be fixed at about 8.5V. The volts-per-turn across the windings will drop from 80 / 32 = 2.5 V/turn to 8.5/32 = 0.265 V/turn, that is nearly 10 times less. All of the outputs will be reduced by the same ratio (a higher value can be found because of capacitors peak charging due to load absence). The TL431 is cut out: it sees the drop of the 200V output and would try to correct this by increasing its cathode voltage, which is not possible because this is fixed by the 3.3V zener.

The reduction of winding voltages concerns the primary side as well: the voltage generated by the auxiliary winding drops to some 1V and is no longer able to power the L5993. To maintain circuit operation, a second auxiliary winding, stacked on the first one, has been added, with a turn number (40) such that in OFF mode it develops a voltage sufficient to power the L5993.

However, during normal operation the voltage it develops will be much higher (close to 120V). This is why Q6 has been added: during normal operation the first auxiliary winding develops more than 15V thus the base-emitter junction of Q6 is reverse biased and Q6 is cut off, thus blocking the high voltage. When entering OFF mode, Q6 is turned on (it does not work as a linear regulator) and lets the second auxiliary winding supply the L5993.

As Q5 is turned off because normal operation is to be resumed, also Q4 will be turned off and the output voltages will go back to their rated values after a transient similar to the initial power-up.

Table A1 shows the improvement offered by the voltage reduction circuit. A load condition similar to or slightly heavier than that of a real monitor (without any power management circuit) is assumed, and the consumption from the mains is shown with and without the additional circuit included in fig. A1.

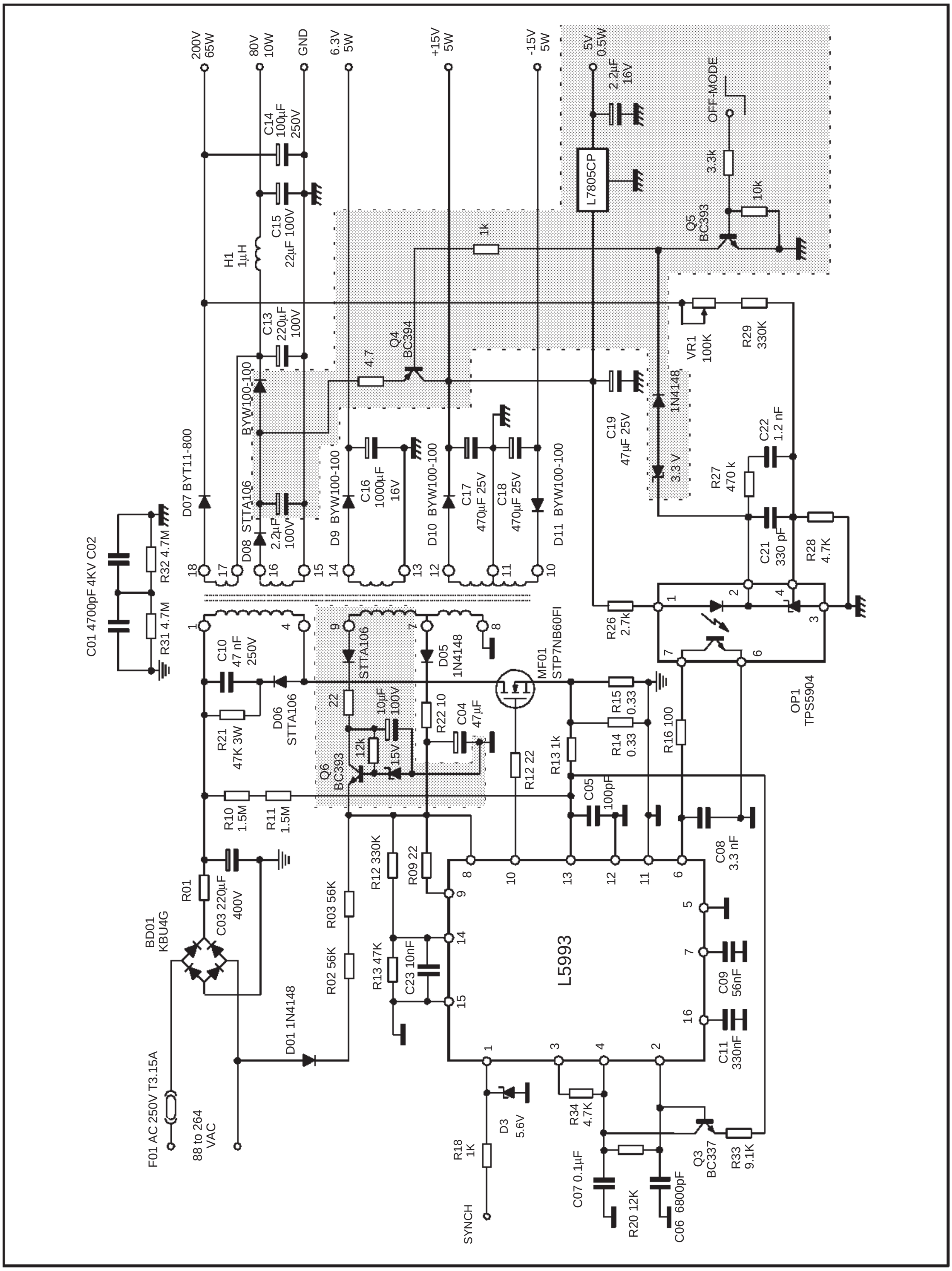
Table A1. Consumption from the mains in OFF mode.

V_{AC} [V]	88	110	160	220	264
Pin [W] (*)	4.3	4.4	4.6	4.8	4.9
Pin [W] (**)	2	2.1	2.2	2.4	2.5

Load conditions: 200V: 40 kΩ; 80V: 20 kΩ; +5V: 47Ω; other outputs open

(*) Without voltage reduction
(**) With voltage reduction

Figure A1. Application board Electrical Schematic with OFF-mode management.



Alternative Frequency Compensation Network

A method alternative to the one illustrated in the previous section for cutting down the residual loads is to physically disconnect the loads by means of series switches. In that case the outputs are actually open.

With this approach, if the application board is repeatedly subjected to quick power-off/power-on cycles during OFF mode, it may not start-up. In fact, being the load of the 200V output open, after a power off the output voltage decays very slowly. If the board is powered on again when the output capacitor is still almost fully charged, the output voltage will rise quickly and overshoot the regulated value. The PWM may be stopped so long - to allow the output voltage to decay to its correct value - that the L5993 loses its supply and goes into undervoltage lockout. Next, the L5993 is restarted by R2+R3, the sequence recurs and the system gets stuck in this on-off cycle.

To avoid this, it is recommended to use the other feedback configuration provided in the PCB, which makes use of C20 and R30. As shown in figure A2, in that case C22 and R27 will be omitted and the value of C21 will be changed. C20 provides an anticipatory effect that prevents the overshoot and the resulting vicious circle above described.

Figure A2. Alternative compensation network to be used with switch-opened loads. Parts added or modified are in bold italics.