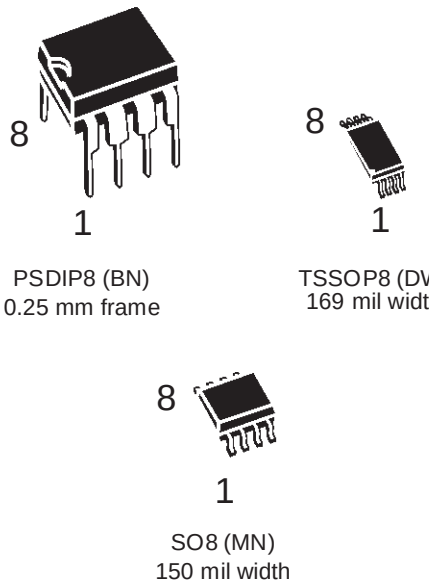
M95040
M95020, M95010

4/2/1 Kbit Serial SPI Bus EEPROM With High Speed Clock

PRELIMINARY DATA

- Compatible with SPI Bus Serial Interface (Positive Clock SPI Modes)
- Single Supply Voltage:
  - 4.5V to 5.5V for M950x0
  - 2.5V to 5.5V for M950x0-W
  - 1.8V to 3.6V for M950x0-R
- 5 MHz Clock Rate (maximum)
- Status Register
- BYTE and PAGE WRITE (up to 16 Bytes)
- Self-Timed Programming Cycle
- Adjustable Size Read-Only EEPROM Area
- Enhanced ESD Protection
- More than 1,000,000 Erase/Write Cycles
- More than 40 Year Data Retention



DESCRIPTION

These SPI-compatible electrically erasable programmable memory (EEPROM) devices are organized as 512 x 8 bits, 256 x 8 bits and 128 x 8 bits (M95040, M95020, M95010). They operate down to 2.5 V (for the -W version of each device), and down to 1.8 V (for the -R version of each device).

Table 1. Signal Names

C	Serial Clock
D	Serial Data Input
Q	Serial Data Output
$\overline{S}$	Chip Select
$\overline{W}$	Write Protect
$\overline{HOLD}$	Hold
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

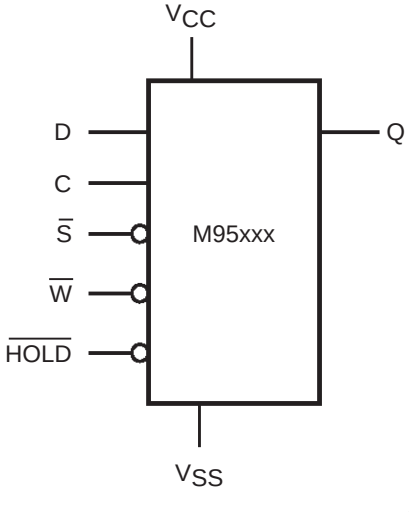


Figure 2A. DIP Connections

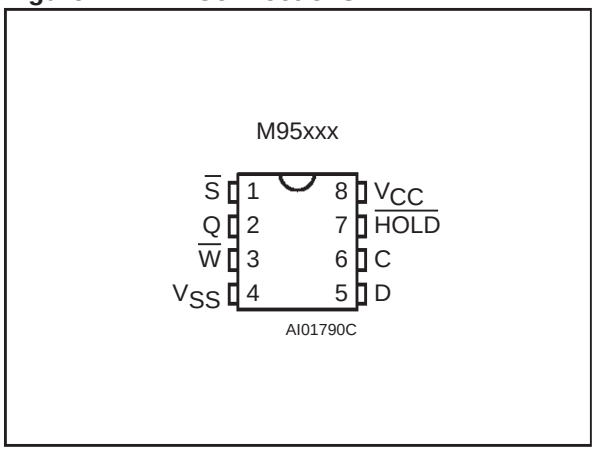
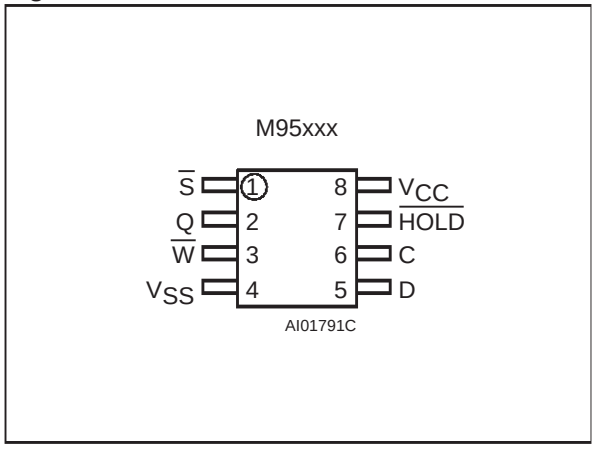


Figure 2B. SO and TSSOP Connections



The M95040 and M95020, M95010 are available in Plastic Dual-in-Line, Plastic Small Outline and Thin Shrink Small Outline packages.

Each memory device is accessed by a simple serial interface that is SPI-compatible. The bus signals are C, D and Q, as shown in Table 1 and Figure 3.

The device is selected when the chip select input ($\overline{S}$) is held low. Communications with the chip can be interrupted using the hold input ($\overline{HOLD}$). Write operations are disabled by the write protect input ($\overline{W}$).

SIGNAL DESCRIPTION

Serial Output (Q)

The output pin is used to transfer data serially out of the Memory. Data is shifted out on the falling edge of the serial clock.

Serial Input (D)

The input pin is used to transfer data serially into the device. Instructions, addresses, and the data to be written, are each received this way. Input is latched on the rising edge of the serial clock.

Serial Clock (C)

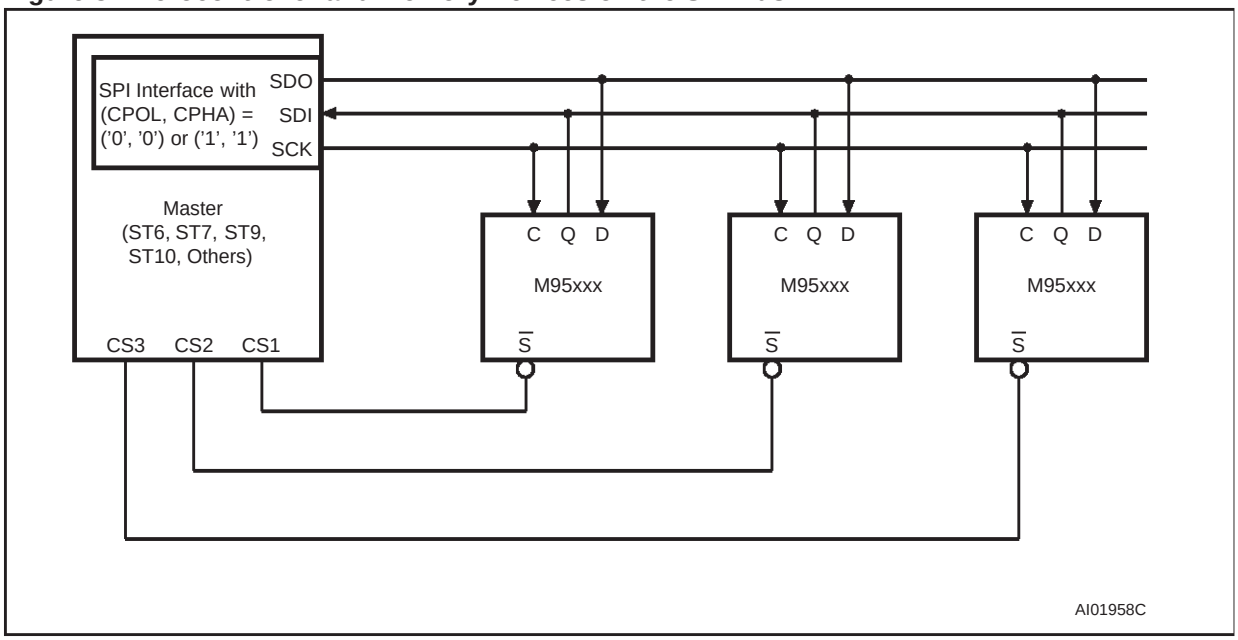
The serial clock provides the timing for the serial interface (as shown in Figure 4). Instructions, addresses, or data are latched, from the input pin,

Table 2. Absolute Maximum Ratings [1]

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature		-40 to 125	°C
T_{STG}	Storage Temperature		-65 to 150	°C
T_{LEAD}	Lead Temperature during Soldering	PSDIP8: 10 sec SO8: 40 sec TSSOP8: t.b.c.	260 215 t.b.c.	°C
V_O	Output Voltage Range		-0.3 to V_{CC}+0.6	V
V_I	Input Voltage Range		-0.3 to 6.5	V
V_{CC}	Supply Voltage Range		-0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) [2]		4000	V
	Electrostatic Discharge Voltage (Machine model) [3]		400	V

Note: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the ST SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100 pF, 1500 Ω)
3. EIAJ IC-121 (Condition C) (200pF, 0W).

Figure 3. Microcontroller and Memory Devices on the SPI Bus



on the rising edge of the clock input. The output data on the Q pin changes state after the falling edge of the clock input.

Chip Select ($\overline{S}$)

When $\overline{S}$ is high, the memory device is deselected, and the Q output pin is held in its high impedance state. Unless an internal write operation is underway, the memory device is placed in its stand-by power mode.

After power-on, a high-to-low transition on $\overline{S}$ is required prior to the start of any operation.

Write Protect ($\overline{W}$)

This pin is for hardware write protection. When $\overline{W}$ is low, writes to the device are disabled, but all other operations remain enabled. When $\overline{W}$ is high, write operations are enabled. If $\overline{W}$ goes low at any time before the last bit, D0, of the data stream, the write enable latch is reset, thus preventing the write from taking effect. No action on $\overline{W}$ or on the write enable latch can interrupt a write cycle which has commenced, though.

Hold ($\overline{HOLD}$)

The $\overline{HOLD}$ pin is used to pause the serial communications between the SPI memory and controller, without losing bits that have already been decoded in the serial sequence. For a hold condition to occur, the memory device must already have been selected ($\overline{S}$ = 0). The hold condition starts when the $\overline{HOLD}$ pin is held low while the clock pin (C) is also low (as shown in Figure 14).

During the hold condition, the Q output pin is held in its high impedance state, and the levels on the input pins (D and C) are ignored by the memory device.

It is possible to deselect the device when it is still in the hold state, thereby resetting whatever transfer had been in progress. The memory remains in the hold state as long as the $\overline{HOLD}$ pin is low. To restart communication with the device, it is necessary both to remove the hold condition (by taking $\overline{HOLD}$ high) and to select the memory (by taking $\overline{S}$ low).

The Memory can be driven by a microcontroller with its SPI peripheral running in either of the two following modes: (CPOL, CPHA) = ('0','0') or (CPOL,CPHA) = ('1','1').

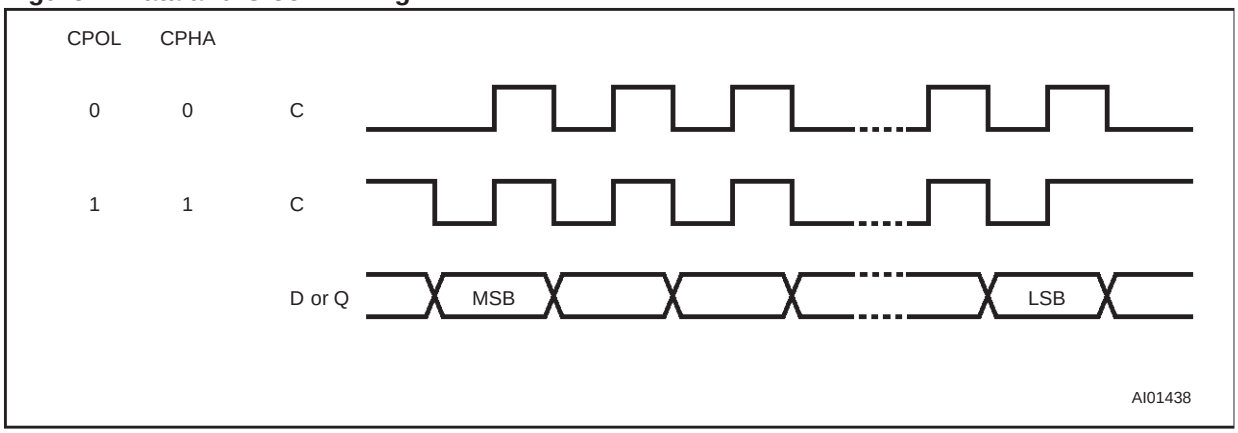
For these two modes, input data is latched in by the low to high transition of clock C, and output data is available from the high to low transition of Clock (C).

The difference between (CPOL, CPHA) = (0, 0) and (CPOL, CPHA) = (1, 1) is the stand-by polarity: C remains at '0' for (CPOL, CPHA) = (0, 0) and C remains at '1' for (CPOL, CPHA) = (1, 1) when there is no data transfer.

OPERATIONS

All instructions, addresses and data are shifted serially in and out of the chip. The most significant bit is presented first, with the data input (D) sampled on the first rising edge of the clock (C) after the chip select ($\overline{S}$) goes low.

Figure 4. Data and Clock Timing



Every instruction starts with a single-byte code, as summarized in Table 3. This code is entered via the data input (D), and latched on the rising edge of the clock input (C). To enter an instruction code, the product must have been previously selected ($\overline{S}$ held low). If an invalid instruction is sent (one not contained in Table 3), the chip automatically deselects itself.

Write Enable (WREN) and Write Disable (WRDI)

The write enable latch, inside the memory device, must be set prior to each WRITE and WRSR operation. The WREN instruction (write enable) sets this latch, and the WRDI instruction (write disable) resets it.

Table 3. Instruction Set

Instruction	Description	Instruction Format
WREN	Set Write Enable Latch	0000 X110
WRDI	Reset Write Enable Latch	0000 X100
RDSR	Read Status Register	0000 X101
WRSR	Write Status Register	0000 X001
READ	Read Data from Memory Array	0000 $A_8$011
WRITE	Write Data to Memory Array	0000 $A_8$010

Note: 1. A8 = 1 for the upper page on the M95040, and 0 for the lower page, and is Don't Care for other devices.
2. X = Don't Care.

Table 4. Status Register Format

b7							b0
1	1	1	1	BP1	BP0	WEL	WIP

Note: 1. BP1 and BP0 are read and write bits.
2. WEL and WIP are read only bits.
3. b7 to b4 are read only bits.

The latch becomes reset by any of the following events:

– Power on
– WRDI instruction completion
– WRSR instruction completion
– WRITE instruction completion
– the $\overline{W}$ pin is held low.

As soon as the WREN or WRDI instruction is received, the memory device first executes the instruction, then enters a wait mode until the device is deselected.

Read Status Register (RDSR)

The RDSR instruction allows the status register to be read, and can be sent at any time, even during a Write operation. Indeed, when a Write is in progress, it is recommended that the value of the Write-In-Progress (WIP) bit be checked. The value in the WIP bit (whose position in the status register is shown in Table 4) can be polled, before sending a new WRITE instruction.

The Write-In-Process (WIP) bit is read-only, and indicates whether the memory is busy with a Write operation. A '1' indicates that a write is in progress, and a '0' that no write is in progress.

The Write Enable Latch (WEL) bit indicates the status of the write enable latch. It, too, is read-only. Its value can only be changed by one of the events listed in the previous paragraph, or as a result of executing WREN or WRDI instruction. It cannot be changed using a WRSR instruction. A '1' indicates that the latch is set (the forthcoming Write instruction will be executed), and a '0' that it is reset (and any forthcoming Write instructions will be ignored).

The Block Protect (BP0 and BP1) bits indicate the amount of the memory that is to be write-protected. These two bits are non-volatile. They are set using a WRSR instruction.

Figure 5. RDSR: Read Status Register Sequence

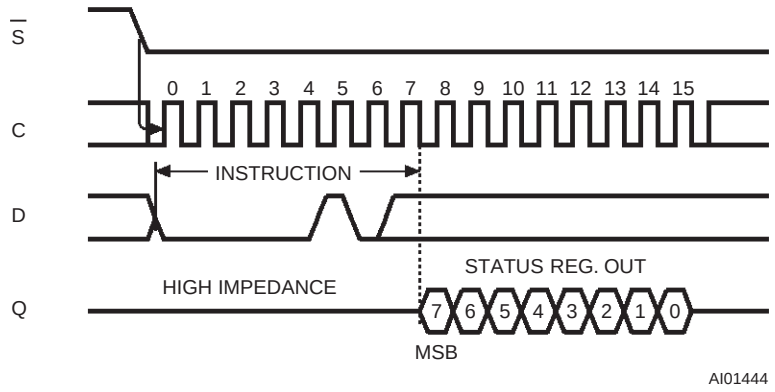


Figure 6. Block Diagram

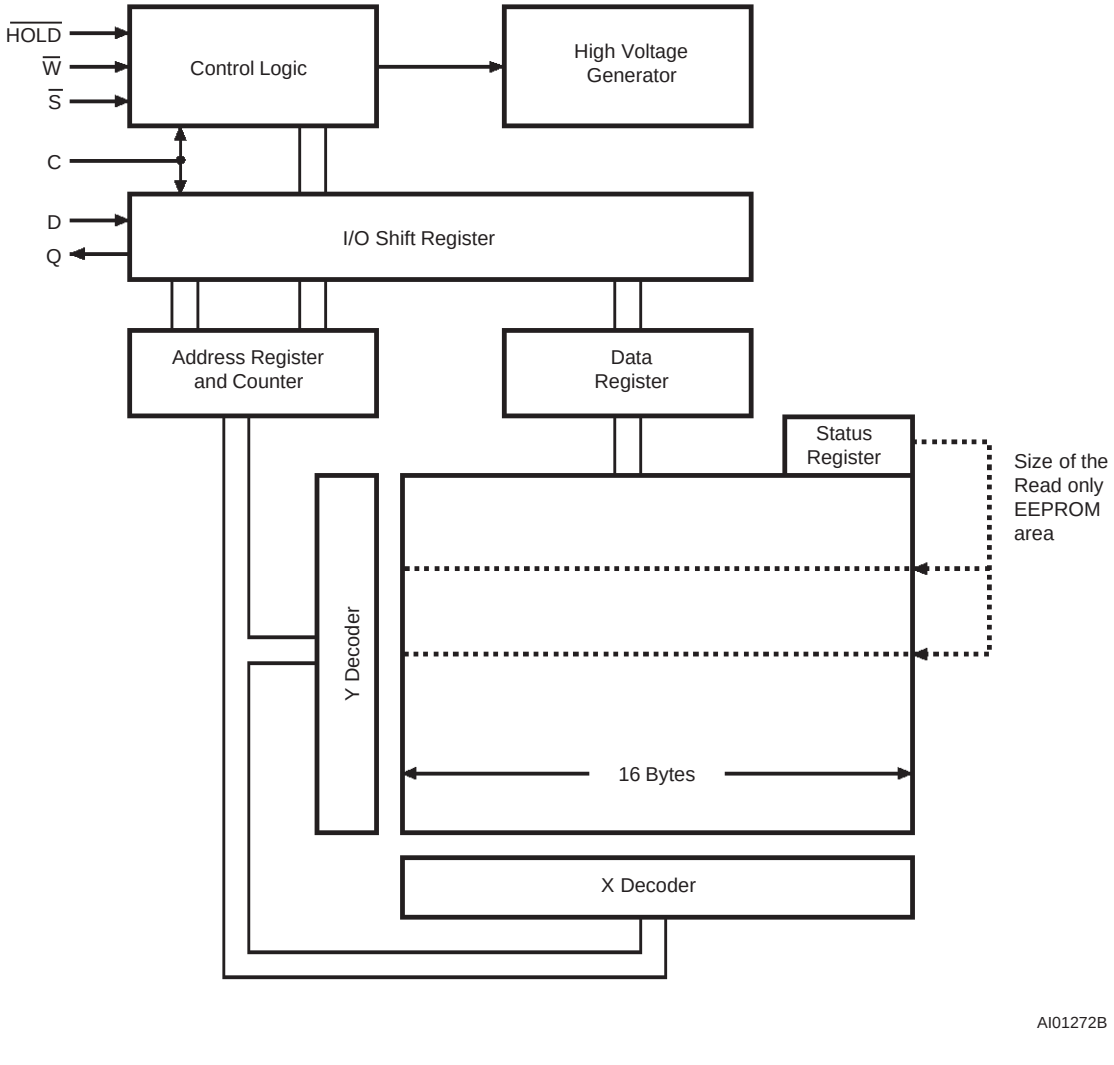


Table 5. Write Protected Block Size

Status Register Bits		Protected Block	Array Addresses Protected		
BP1	BP0		M95040	M95020	M95010
0	0	none	none	none	none
0	1	Upper quarter	180h - 1FFh	C0h - FFh	060h - 7Fh
1	0	Upper half	100h - 1FFh	80h - FFh	040h - 7Fh
1	1	Whole memory	000h - 1FFh	00h - FFh	000h - 7Fh

During a Write operation (whether it be to the memory area or to the status register), all bits of the status register remain valid, and can be read using the RDSR instruction. However, during a Write operation, the values of the non-volatile bits (BP0, BP1) become frozen at a constant value. The updated value of these bits becomes available when a new RDSR instruction is executed, after completion of the write cycle. On the other hand, the two read-only bits (WEL, WIP) are dynamically updated during internal write cycles. Using this facility, it is possible to poll the WIP bit to detect the end of the internal write cycle.

Write Status Register (WRSR)

The format of the WRSR instruction is shown in Figure 7. After the instruction and the eight bits of the status register have been latched-in, the internal Write cycle is triggered by the rising edge of the $\overline{S}$ line. This must occur after the falling edge of the 16th clock pulse, and before the rising edge of the 17th clock (as indicated in Figure 7), otherwise the internal write sequence is not performed.

The WRSR instruction is used to select the size of memory area that is to be write-protected.

The BP1 and BP0 bits of the status register have the appropriate value (see Table 5) written into them after the contents of the protected area of the EEPROM have been written.

The initial delivery state of the BP1 and BP0 bits is 00, indicating a write-protection size of 0.

Read Operation

The chip is first selected by holding $\overline{S}$ low. The serial one byte read instruction is followed by a one byte address (A7-A0), each bit being latched-in during the rising edge of the clock (C). The most significant bit, A8, of the address is incorporated as bit b3 of the instruction byte, as shown in Table 3.

The data stored in the memory, at the selected address, is shifted out on the Q output pin. Each bit is shifted out during the falling edge of the clock (C) as shown in Figure 8. The internal address counter is automatically incremented to the next higher address after each byte of data has been shifted out. The data stored in the memory, at the next address, can be read by successive clock pulses. When the highest address is reached, the address counter rolls over to “0000h”, allowing the read cycle to be continued indefinitely. The read operation is terminated by deselecting the chip.

Figure 7. WRSR: Write Status Register Sequence

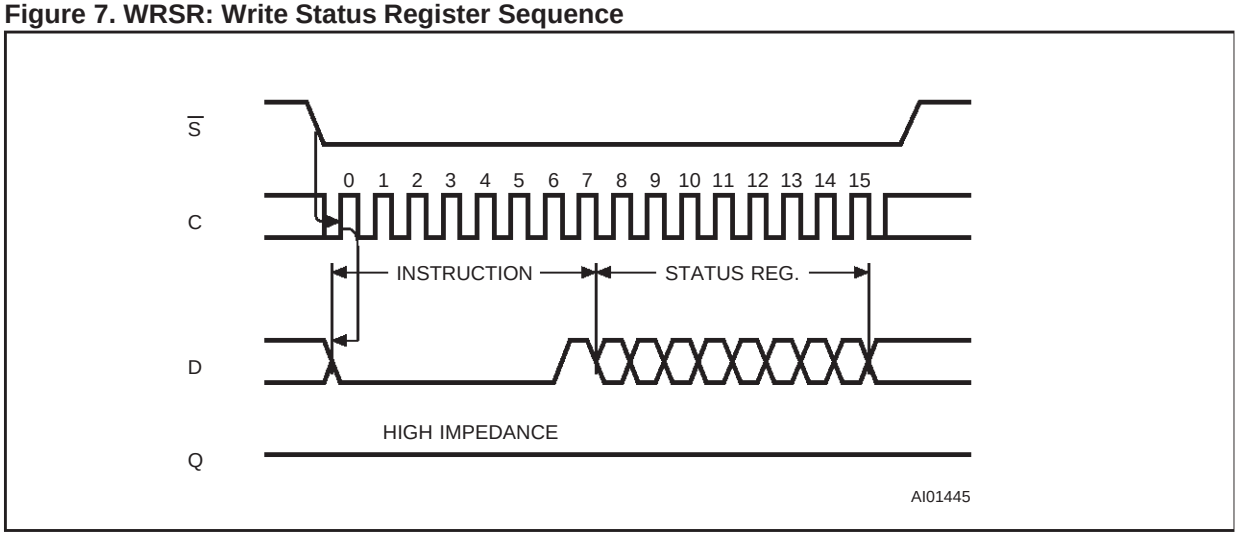
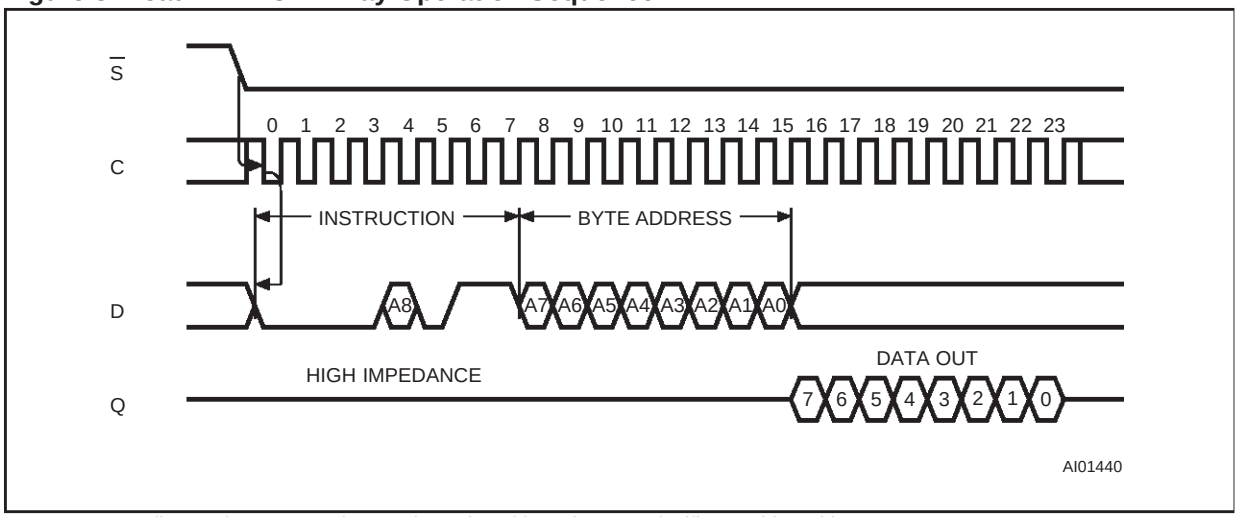


Figure 8. Read EEPROM Array Operation Sequence



Note: 1. Depending on the memory size, as shown in Table 6, the most significant address bits are Don't Care.

Table 6. Address Range Bits

Device	M95040	M95020	M95010
Address Bits	A8-A0	A7-A0	A6-A0

The chip can be deselected at any time during data output. If a read instruction is received during a write cycle, it is rejected, and the memory device deselects itself.

Byte Write Operation

Before any write can take place, the WEL bit must be set, using the WREN instruction. The write state is entered by selecting the chip, issuing two bytes of instruction and address, and one byte of data. Chip Select ($\overline{S}$) must remain low throughout the operation, as shown in Figure 10. The product must be deselected just after the eighth bit of the data byte has been latched in, as shown in Figure 10, otherwise the write process is cancelled. As soon as the memory device is deselected, the self-timed internal write cycle is initiated. While the write is in progress, the status register may be read to check the status of the BP1, BP0, WEL and WIP bits. In particular, WIP contains a '1' during the self-timed write cycle, and a '0' when the cycle is complete, (at which point the write enable latch is also reset).

Page Write Operation

A maximum of 16 bytes of data can be written during one Write time, t_W, provided that they are all to the same page (see Figure 6). The Page Write operation is the same as the Byte Write operation, except that instead of deselecting the device after the first byte of data, up to 15 additional bytes can be shifted in (and then the device is deselected after the last byte).

Any address of the memory can be chosen as the first address to be written. If the address counter reaches the end of the page (an address of the

Figure 9. Write Enable Latch Sequence

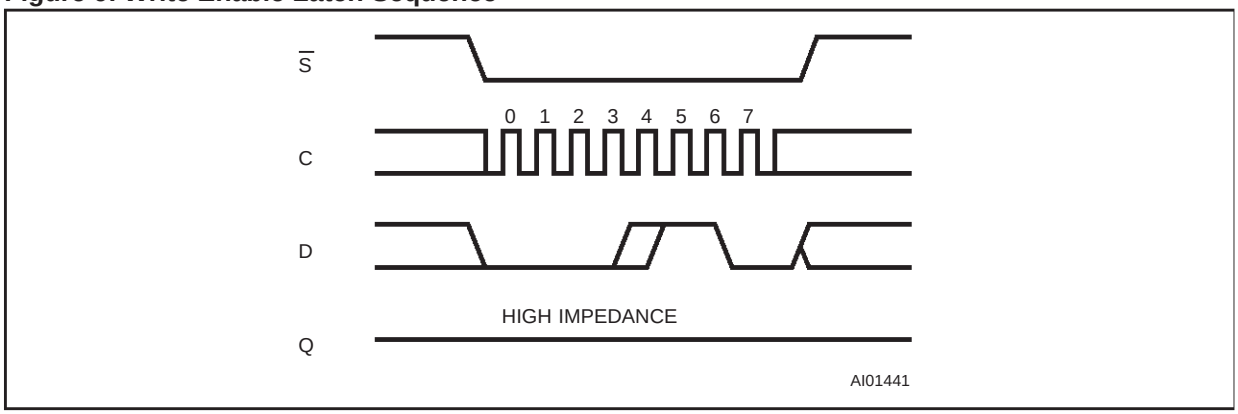
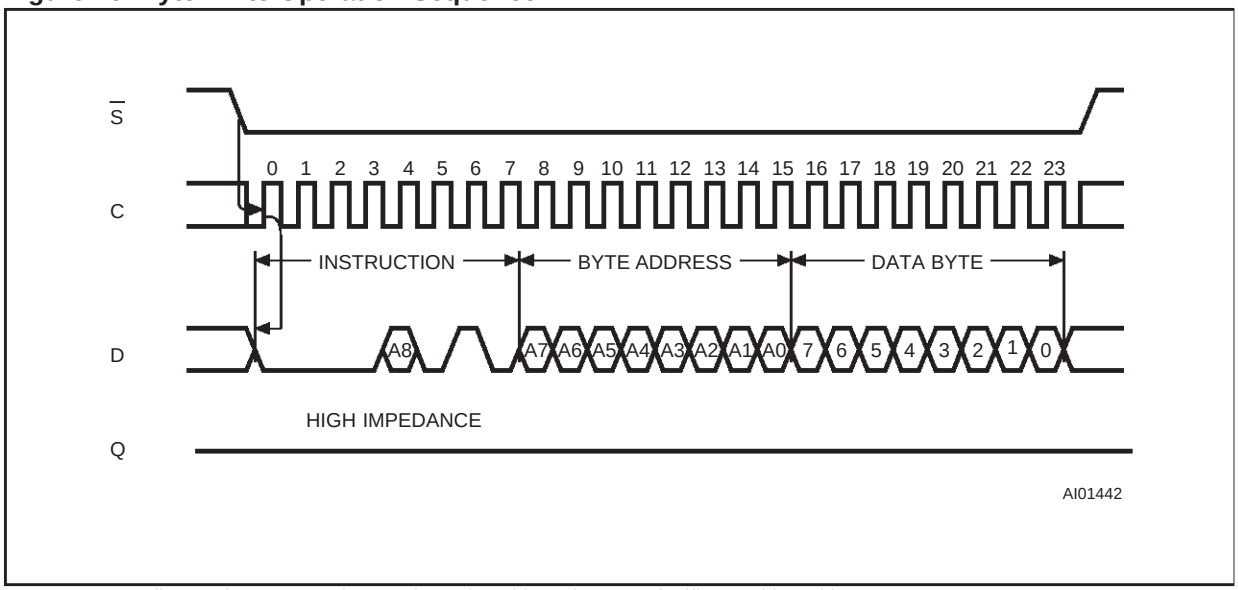
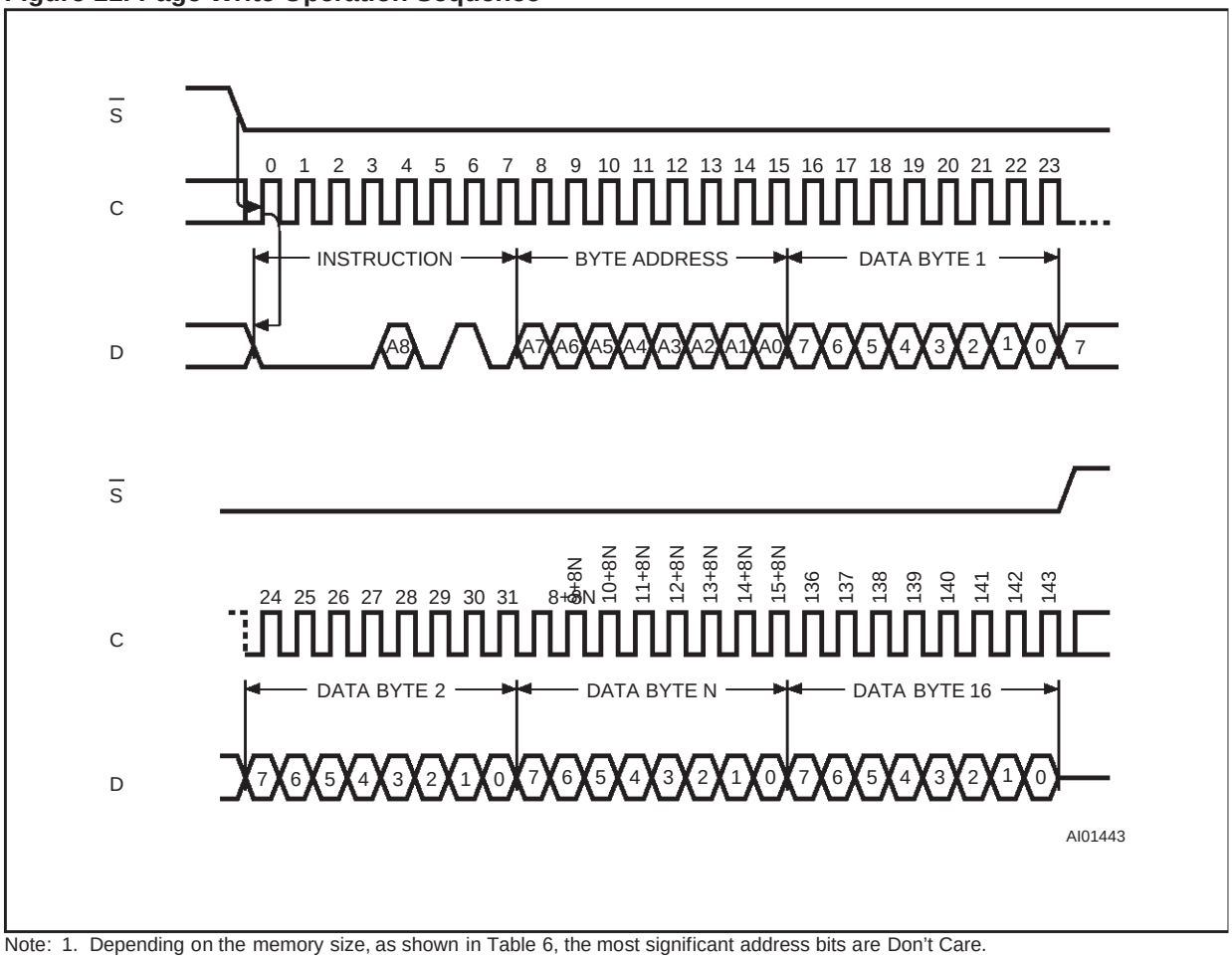


Figure 10. Byte Write Operation Sequence



Note: 1. Depending on the memory size, as shown in Table 6, the most significant address bits are Don't Care.

Figure 11. Page Write Operation Sequence



Note: 1. Depending on the memory size, as shown in Table 6, the most significant address bits are Don't Care.

form xxxx 1111) and the clock continues, the counter rolls over to the first address of the same page (xxxx 0000) and over-writes any previously written data.

As before, the Write cycle only starts if the $\overline{S}$ transition occurs just after the eighth bit of the last data byte has been received, as shown in Figure 11.

DATA PROTECTION AND PROTOCOL SAFETY

To protect the data in the memory from inadvertent corruption, the memory device only responds to correctly formulated commands. The main security measures can be summarized as follows:

– The WEL bit is reset at power-up.
– $\overline{S}$ must rise after the eighth clock count (or multiple thereof) in order to start a non-volatile write cycle (in the memory array or in the status register).
– Accesses to the memory array are ignored during the non-volatile programming cycle, and the programming cycle continues unaffected.
– After execution of a WREN, WRDI, or RDSR instruction, the chip enters a wait state, and waits to be deselected.
– Invalid $\overline{S}$ and $\overline{HOLD}$ transitions are ignored.

POWER ON STATE

After power-on, the memory device is in the following state:

– low power stand-by state
– deselected (after power-on, a high-to-low transition is required on the $\overline{S}$ input before any operations can be started).
– not in the hold condition
– the WEL bit is reset
– the BP1 and BP0 bits of the status register are unchanged from the previous power-down (they are non-volatile bits).

INITIAL DELIVERY STATE

The device is delivered with the memory array in a fully erased state (all data set at all 1s or FFh). The status register bits are initialized to 00h, as shown in Table 7.

Table 7. Initial Status Register Format

b7							b0
1	1	1	1	0	0	0	0

Table 8. Input Parameters[1] (T_A = 25 °C, f = 5 MHz)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
C_{OUT}	Output Capacitance (Q)			8	pF
C_{IN}	Input Capacitance (D)			8	pF
	Input Capacitance (other pins)			6	pF

Note: 1. Sampled only, not 100% tested.

Table 9. DC Characteristics
(T_A = –40 to 85 °C or –40 to 125 °C; V_{CC} = 4.5 to 5.5 V)
(T_A = –40 to 85 °C; V_{CC} = 2.5 to 5.5 V)
(T_A = –20 to 85 °C; V_{CC} = 1.8 to 3.6 V)

Symbol	Parameter	Voltage Range	Temp. Range	Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current	all	all			± 2	µA
I_{LO}	Output Leakage Current	all	all			± 2	µA
I_{CC}	Supply Current	4.5-5.5	6	C = 0.1V_{CC}/0.9V_{CC} , at 5 MHz, V_{CC} = 5 V, Q = open		5	mA
		4.5-5.5	3	C = 0.1V_{CC}/0.9V_{CC} , at 2 MHz, V_{CC} = 5 V, Q = open		5	mA
		2.5-5.5	6	C = 0.1V_{CC}/0.9V_{CC} , at 2 MHz, V_{CC} = 2.5 V, Q = open		2	mA
		1.8-3.6	5	C = 0.1V_{CC}/0.9V_{CC} , at 1 MHz, V_{CC} = 1.8 V, Q = open		2	mA
I_{CC1}	Supply Current (Stand-by)	4.5-5.5	6	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC} , V_{CC} = 5 V		10	µA
		4.5-5.5	3	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC} , V_{CC} = 5 V		10	µA
		2.5-5.5	6	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC} , V_{CC} = 2.5 V		2	µA
		1.8-3.6	5	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC} , V_{CC} = 1.8 V		2	µA
V_{IL}	Input Low Voltage	all	all		– 0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage	all	all		0.7 V_{CC}	V_{CC}+1	V
V_{OL}[1]	Output Low Voltage	4.5-5.5	6	I_{OL} = 2 mA, V_{CC} = 5 V		0.4	V
		4.5-5.5	3	I_{OL} = 2 mA, V_{CC} = 5 V		0.4	V
		2.5-5.5	6	I_{OL} = 1.5 mA, V_{CC} = 2.5 V		0.4	V
		1.8-3.6	5	I_{OL} = 0.15 mA, V_{CC} = 1.8 V		0.3	V
V_{OH}[1]	Output High Voltage	4.5-5.5	6	I_{OH} = –2 mA, V_{CC} = 5 V	0.8 V_{CC}		V
		4.5-5.5	3	I_{OH} = –2 mA, V_{CC} = 5 V	0.8 V_{CC}		V
		2.5-5.5	6	I_{OH} = –0.4 mA, V_{CC} = 2.5 V	0.8 V_{CC}		V
		1.8-3.6	5	I_{OH} = –0.1 mA, V_{CC} = 1.8 V	0.8 V_{CC}		V

Note: 1. For all 5V range devices, the device meets the output requirements for both TTL and CMOS standards.

Table 10A. AC Characteristics

Symbol	Alt.	Parameter	M95040, M95020, M95010				Unit
			V_{CC}=4.5 to 5.5 V T_A=–40 to 85°C		V_{CC}=4.5 to 5.5 V T_A=–40 to 125°C		
			Min	Max	Min	Max	
f_C	f_{SCK}	Clock Frequency	D.C.	5	D.C.	2	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ Active Setup Time	90		200		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ Not Active Setup Time	90		200		ns
t_{SHSL}	t_{CS}	$\overline{S}$ Deselect Time	100		200		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ Active Hold Time	90		200		ns
t_{CHSL}		$\overline{S}$ Not Active Hold Time	90		200		ns
t_{CH} [1]	t_{CLH}	Clock High Time	90		200		ns
t_{CL} [1]	t_{CLL}	Clock Low Time	90		200		ns
t_{CLCH} [2]	t_{RC}	Clock Rise Time		1		1	µs
t_{CHCL} [2]	t_{FC}	Clock Fall Time		1		1	µs
t_{DVCH}	t_{DSU}	Data In Setup Time	20		40		ns
t_{CHDX}	t_{DH}	Data In Hold Time	30		50		ns
t_{DLDH} [2]	t_{RI}	Data In Rise Time		1		1	µs
t_{DHDL} [2]	t_{FI}	Data In Fall Time		1		1	µs
t_{HHCH}	t_{CD}	Clock Low Hold Time after $\overline{HOLD}$ not Active	70		140		ns
t_{HLCH}		Clock Low Hold Time after $\overline{HOLD}$ Active	40		90		ns
t_{CLHL}		Clock Low Set-up Time before $\overline{HOLD}$ Active	0		0		ns
t_{CLHH}		Clock Low Set-up Time before $\overline{HOLD}$ not Active	0		0		ns
t_{SHQZ} [2]	t_{DIS}	Output Disable Time		100		250	ns
t_{CLQV}	t_V	Clock Low to Output Valid		60		150	ns
t_{CLQX}	t_{HO}	Output Hold Time	0		0		ns
t_{QLQH} [2]	t_{RO}	Output Rise Time		50		100	ns
t_{QHQL} [2]	t_{FO}	Output Fall Time		50		100	ns
t_{HHQX} [2]	t_{LZ}	$\overline{HOLD}$ High to Output Low-Z		50		100	ns
t_{HLQZ} [2]	t_{HZ}	$\overline{HOLD}$ Low to Output High-Z		100		250	ns
t_W	t_{WC}	Write Time		10		10	ms

Note: 1. $t_{CH} + t_{CL} \geq 1 / f_C$.
2. Value guaranteed by characterization, not 100% tested in production.

Table 10B. AC Characteristics

Symbol	Alt.	Parameter	M950x0-W		M950x0-R		Unit
			V_{CC}=2.5 to 5.5 V T_A=–40 to 85°C		V_{CC}=1.8 to 3.6 V T_A=–20 to 85°C		
			Min	Max	Min	Max	
f_C	f_{SCK}	Clock Frequency	D.C.	2	D.C.	1	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ Active Setup Time	200		400		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ Not Active Setup Time	200		400		ns
t_{SHSL}	t_{CS}	$\overline{S}$ Deselect Time	200		300		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ Active Hold Time	200		400		ns
t_{CHSL}		$\overline{S}$ Not Active Hold Time	200		400		ns
t_{CH} [1]	t_{CLH}	Clock High Time	200		400		ns
t_{CL} [1]	t_{CLL}	Clock Low Time	200		400		ns
t_{CLCH} [2]	t_{RC}	Clock Rise Time		1		1	µs
t_{CHCL} [2]	t_{FC}	Clock Fall Time		1		1	µs
t_{DVCH}	t_{DSU}	Data In Setup Time	40		60		ns
t_{CHDX}	t_{DH}	Data In Hold Time	50		100		ns
t_{DLDH} [2]	t_{RI}	Data In Rise Time		1		1	µs
t_{DHDL} [2]	t_{FI}	Data In Fall Time		1		1	µs
t_{HHCH}	t_{CD}	Clock Low Hold Time after $\overline{HOLD}$ not Active	140		350		ns
t_{HLCH}		Clock Low Hold Time after $\overline{HOLD}$ Active	90		200		ns
t_{CLHL}		Clock Low Set-up Time before $\overline{HOLD}$ Active	0		0		ns
t_{CLHH}		Clock Low Set-up Time before $\overline{HOLD}$ not Active	0		0		ns
t_{SHQZ} [2]	t_{DIS}	Output Disable Time		250		500	ns
t_{CLQV}	t_V	Clock Low to Output Valid		150		380	ns
t_{CLQX}	t_{HO}	Output Hold Time	0		0		ns
t_{QLQH} [2]	t_{RO}	Output Rise Time		100		200	ns
t_{QHQL} [2]	t_{FO}	Output Fall Time		100		200	ns
t_{HHQX} [2]	t_{LZ}	$\overline{HOLD}$ High to Output Low-Z		100		250	ns
t_{HLQZ} [2]	t_{HZ}	$\overline{HOLD}$ Low to Output High-Z		250		500	ns
t_W	t_{WC}	Write Time		10		10	ms

Note: 1. $t_{CH} + t_{CL} \geq 1 / f_C$.
2. Value guaranteed by characterization, not 100% tested in production.

Table 11. AC Measurement Conditions

Input Rise and Fall Times	≤ 50 ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$
Output Load	C_L = 100 pF

Note: 1. Output Hi-Z is defined as the point where data is no longer driven.

Figure 12. AC Testing Input Output Waveforms

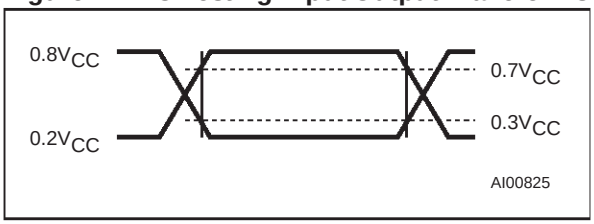


Figure 13. Serial Input Timing

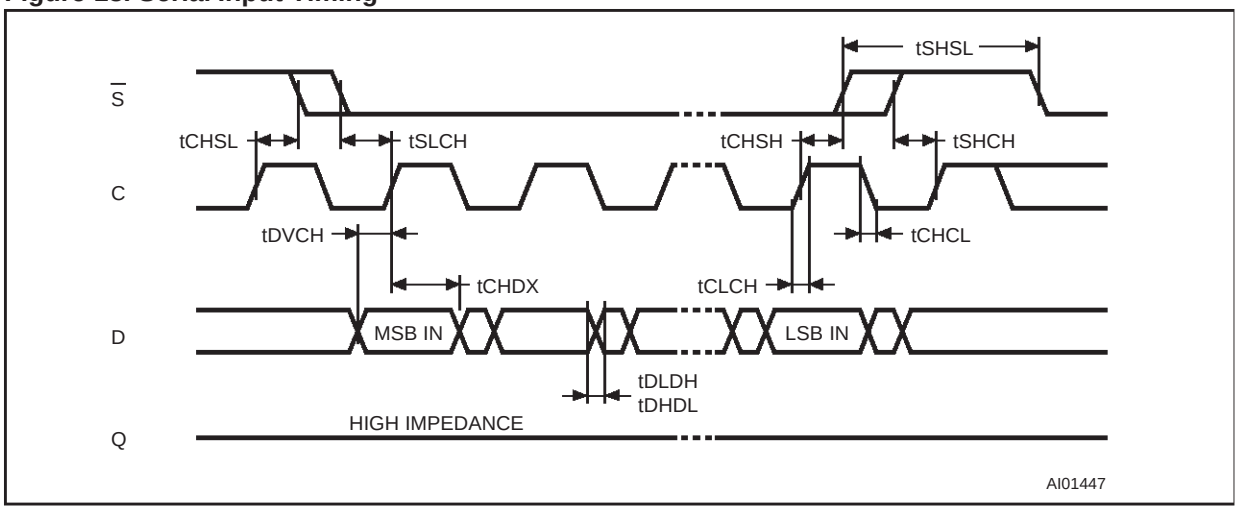


Figure 14. Hold Timing

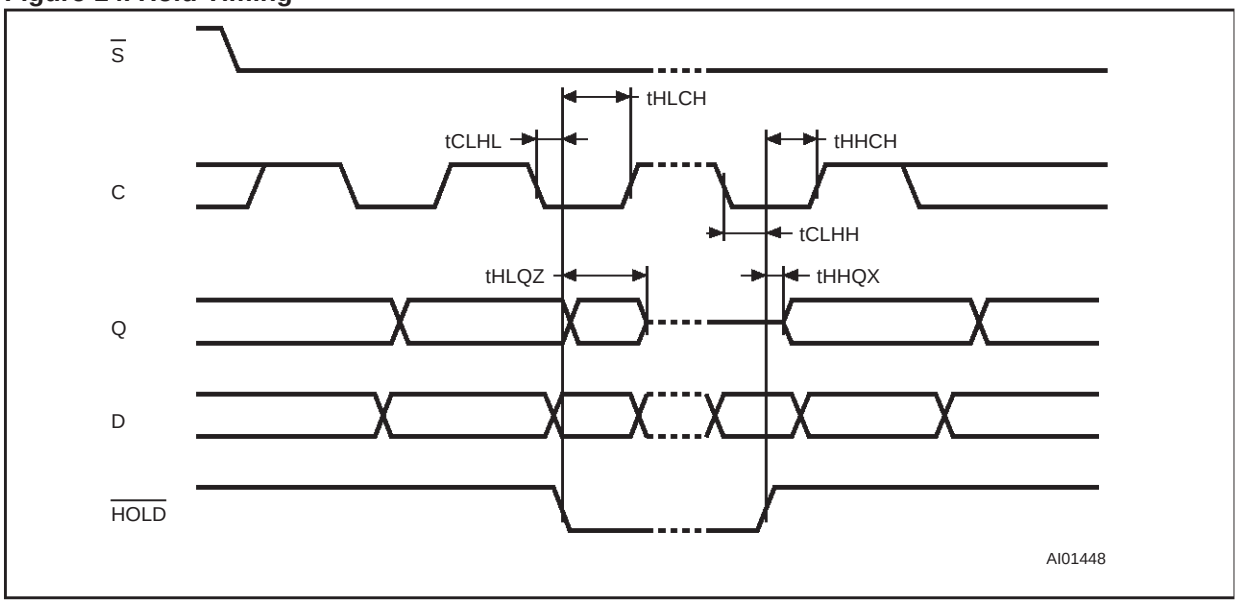
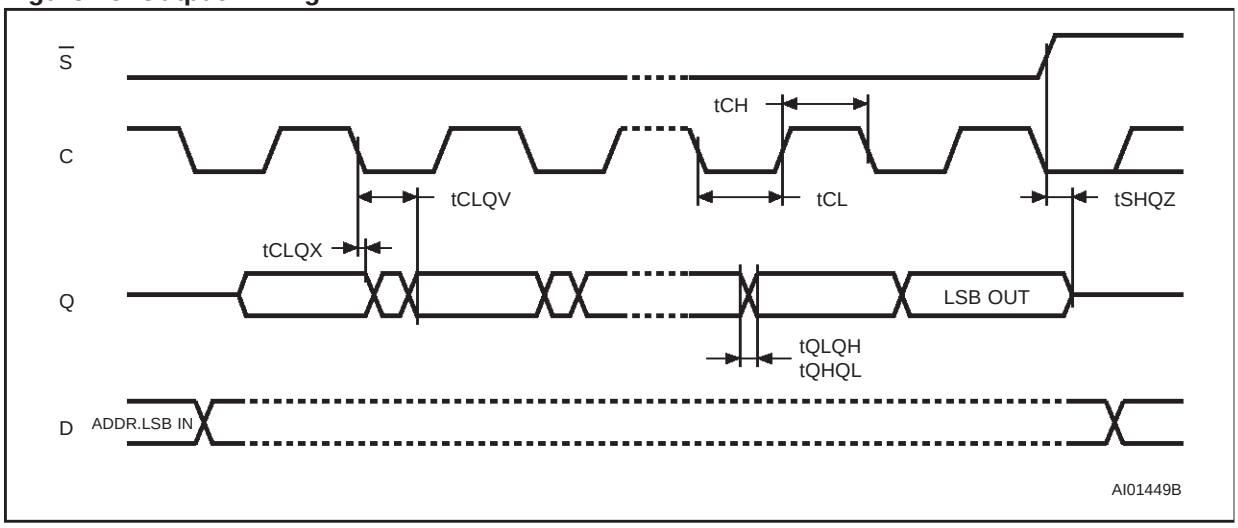


Figure 15. Output Timing



ORDERING INFORMATION

The notation used for the device number is as shown in Table 12. For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

Table 12. Ordering Information Scheme

Example: M95040 – W MN 6 TR

Memory Capacity[3]

040	4 Kbit (512 x 8) with positive clock strobe
020	2 Kbit (256 x 8) with positive clock strobe
010	1 Kbit (128 x 8) with positive clock strobe

Operating Voltage

blank	4.5 V to 5.5 V
W	2.5 V to 5.5 V
R[2]	1.8 V to 3.6 V

Option

TR	Tape and Reel Packing

Temperature Range

5	–20 °C to 85 °C
6	–40 °C to 85 °C
3[1]	–40 °C to 125 °C

Package

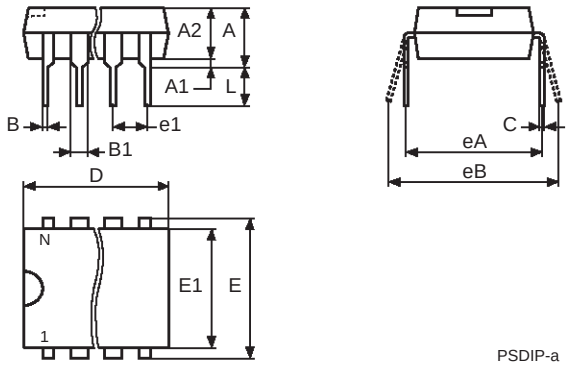
BN	PSDIP8 (0.25 mm frame)
MN	SO8 (150 mil width)
DW	TSSOP8 (169 mil width)

Note: 1. Temperature range available only on request, in V_{CC} range 4.5 V to 5.5 V only.
2. The -R version (V_{CC} range 1.8 V to 3.6 V) only available in temperature range 5.
3. All devices use a positive clock strobe: Data In is strobed on the rising edge of the clock (C) and Data Out is synchronized from the falling edge of the clock.

Table 13. PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N	8			8		

Figure 16. PSDIP8 (BN)

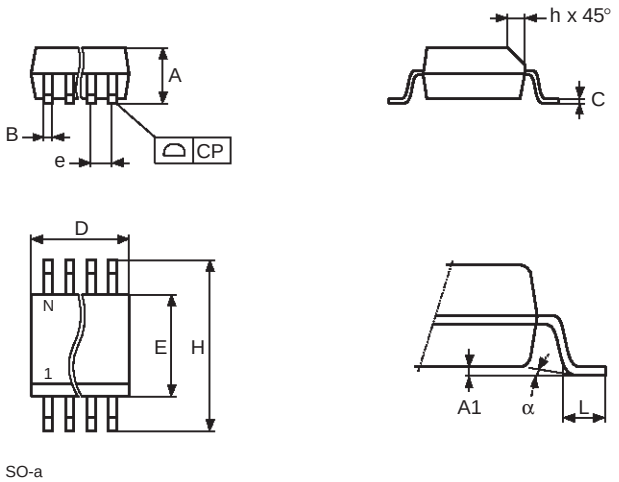


Note: 1. Drawing is not to scale.

Table 14. SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004

Figure 17. SO8 narrow (MN)

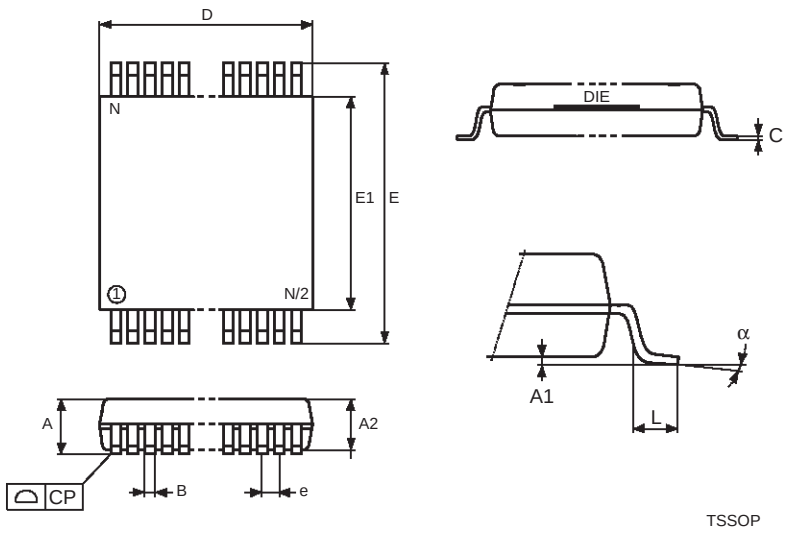


Note: 1. Drawing is not to scale.

Table 15. TSSOP8 - 8 lead Thin Shrink Small Outline

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			1.10			0.043
A1		0.05	0.15		0.002	0.006
A2		0.85	0.95		0.033	0.037
B		0.19	0.30		0.007	0.012
C		0.09	0.20		0.004	0.008
D		2.90	3.10		0.114	0.122
E		6.25	6.50		0.246	0.256
E1		4.30	4.50		0.169	0.177
e	0.65	–	–	0.026	–	–
L		0.50	0.70		0.020	0.028
α		0°	8°		0°	8°
N	8			8		
CP			0.08			0.003

Figure 18. TSSOP8 (DW)



Note: 1. Drawing is not to scale.

Table 16. Revision History

Date	Description of Revision
10-May-2000	s/issuing three bytes/issuing two bytes/ in the 2nd sentence of the Byte Write Operation