



# STP10NB50 STP10NB50FP

## N - CHANNEL 500V - 0.55Ω - 10.6A - TO-220/TO-220FP PowerMESH™ MOSFET

TYPE	V <sub>DSS</sub>	R <sub>D(on)</sub>	I <sub>D</sub>
STP10NB50	500 V	< 0.60 Ω	10.6 A
STP10NB50FP	500 V	< 0.60 Ω	10.6 A

- TYPICAL R<sub>D(on)</sub> = 0.55 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- VERY LOW INTRINSIC CAPACITANCES
- GATE CHARGE MINIMIZED

### DESCRIPTION

Using the latest high voltage MESH OVERLAY™ process, STMicroelectronics has designed an advanced family of power MOSFETs with outstanding performances. The new patent pending strip layout coupled with the Company's proprietary edge termination structure, gives the lowest R<sub>D(on)</sub> per area, exceptional avalanche and dv/dt capabilities and unrivalled gate charge and switching characteristics.

### APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SWITCH MODE POWER SUPPLIES (SMPS)
- DC-AC CONVERTERS FOR WELDING EQUIPMENT AND UNINTERRUPTIBLE POWER SUPPLIES AND MOTOR DRIVE

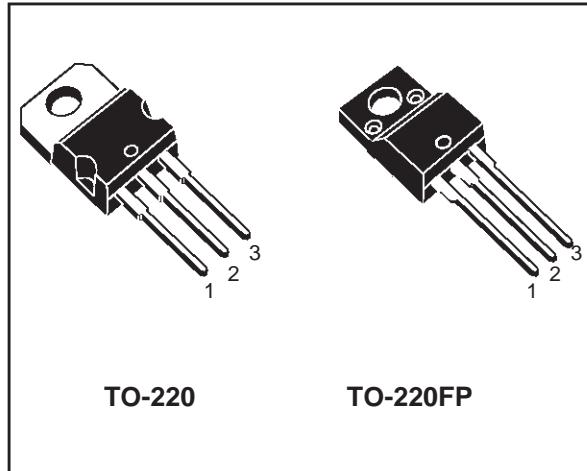
### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		STP10NB50	STP10NB50FP	
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	500	500	V
V <sub>DGR</sub>	Drain-gate Voltage (R <sub>GS</sub> = 20 kΩ)	500	500	V
V <sub>GS</sub>	Gate-source Voltage	± 30	± 30	V
I <sub>D</sub>	Drain Current (continuous) at T <sub>c</sub> = 25 °C	10.6	10.6(*)	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>c</sub> = 100 °C	6.4	6.4(*)	A
I <sub>DM(•)</sub>	Drain Current (pulsed)	42.4	42.4	A
P <sub>tot</sub>	Total Dissipation at T <sub>c</sub> = 25 °C	135	40	W
	Derating Factor	1.08	0.32	W/°C
dv/dt(1)	Peak Diode Recovery voltage slope	4.5	4.5	V/ns
V <sub>ISO</sub>	Insulation Withstand Voltage (DC)	—	2000	V
T <sub>stg</sub>	Storage Temperature	-65 to 150		°C
T <sub>j</sub>	Max. Operating Junction Temperature	150		°C

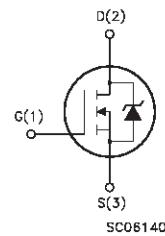
(•) Pulse width limited by safe operating area

(1) I<sub>SD</sub> ≤ 10.6 A, di/dt ≤ 200 A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>j</sub> ≤ T<sub>JMAX</sub>

(\*) Limited only by maximum temperature allowed



### INTERNAL SCHEMATIC DIAGRAM



## STP10NB50 STP10NB50FP

### THERMAL DATA

			TO-220	TO-220FP	
R <sub>thj-case</sub>	Thermal Resistance Junction-case	Max	0.93	3.12	°C/W
R <sub>thj-amb</sub> R <sub>thc-sink</sub>	Thermal Resistance Junction-ambient Thermal Resistance Case-sink	Max Typ	62.5 0.5	300	°C/W °C/W °C
T <sub>I</sub>	Maximum Lead Temperature For Soldering Purpose				

### AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I <sub>AR</sub>	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T <sub>j</sub> max)	10.6	A
E <sub>AS</sub>	Single Pulse Avalanche Energy (starting T <sub>j</sub> = 25 °C, I <sub>D</sub> = I <sub>AR</sub> , V <sub>DD</sub> = 50 V)	550	mJ

### ELECTRICAL CHARACTERISTICS (T<sub>case</sub> = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown Voltage	I <sub>D</sub> = 250 μA V <sub>GS</sub> = 0	500			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max Rating V <sub>DS</sub> = Max Rating T <sub>c</sub> = 125 °C			1 50	μA μA
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 30 V			± 100	nA

ON (\*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> I <sub>D</sub> = 250 μA	3	4	5	V
R <sub>D(on)</sub>	Static Drain-source On Resistance	V <sub>GS</sub> = 10V I <sub>D</sub> = 5.3 A		0.55	0.60	Ω
I <sub>D(on)</sub>	On State Drain Current	V <sub>DS</sub> > I <sub>D(on)</sub> × R <sub>D(on)max</sub> V <sub>GS</sub> = 10 V	10.6			A

### DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub> (*)	Forward Transconductance	V <sub>DS</sub> > I <sub>D(on)</sub> × R <sub>D(on)max</sub> I <sub>D</sub> = 5.3 A	5	8		S
C <sub>iss</sub> C <sub>oss</sub> C <sub>rss</sub>	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V <sub>DS</sub> = 25 V f = 1 MHz V <sub>GS</sub> = 0		1480 210 25		pF pF pF

**ELECTRICAL CHARACTERISTICS (continued)**

## SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on Time Rise Time	$V_{DD} = 250 \text{ V}$ $I_D = 5.3 \text{ A}$ $R_G = 4.7 \Omega$ $V_{GS} = 10 \text{ V}$ (see test circuit, figure 3)		25 13	14 20	ns ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 160 \text{ V}$ $I_D = 10 \text{ A}$ $V_{GS} = 10 \text{ V}$		38 10 17	49	nC nC nC

## SWITCHING OFF

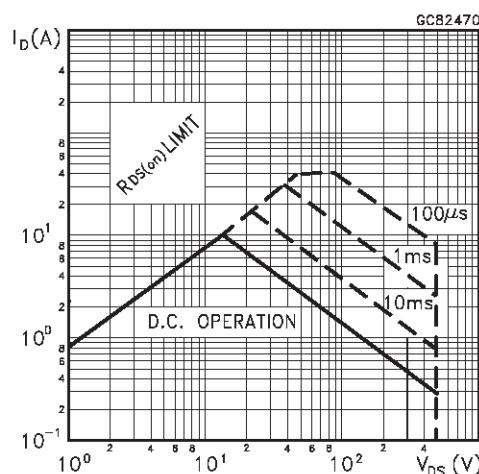
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(V_{off})}$ $t_f$ $t_c$	Off-voltage Rise Time Fall Time Cross-over Time	$V_{DD} = 160 \text{ V}$ $I_D = 10 \text{ A}$ $R_G = 4.7 \Omega$ $V_{GS} = 10 \text{ V}$ (see test circuit, figure 5)		13 15 25	11 14 28	ns ns ns

## SOURCE DRAIN DIODE

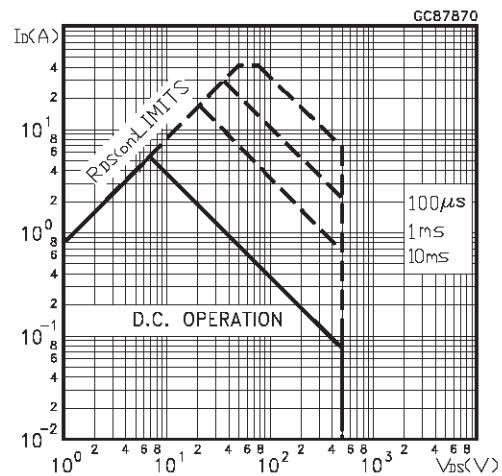
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM}(\bullet)$	Source-drain Current Source-drain Current (pulsed)				10.6 42.4	A A
$V_{SD} (\ast)$	Forward On Voltage	$I_{SD} = 10.6 \text{ A}$ $V_{GS} = 0$			1.6	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 10.6 \text{ A}$ $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 50 \text{ V}$ $T_j = 150^\circ\text{C}$ (see test circuit, figure 5)		560 4.9 17.5		ns nC A

(\*) Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %( $\bullet$ ) Pulse width limited by safe operating area

## Safe Operating Area

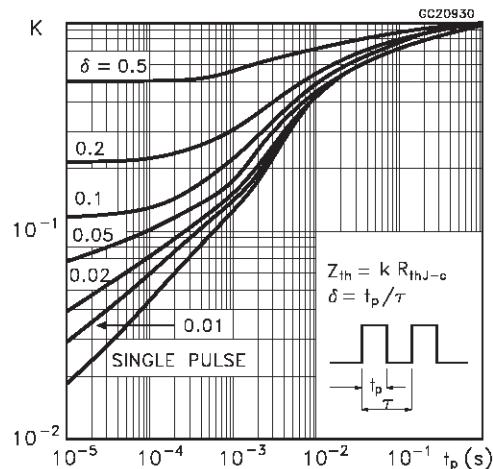


## Safe Operating Area for TO-220FP

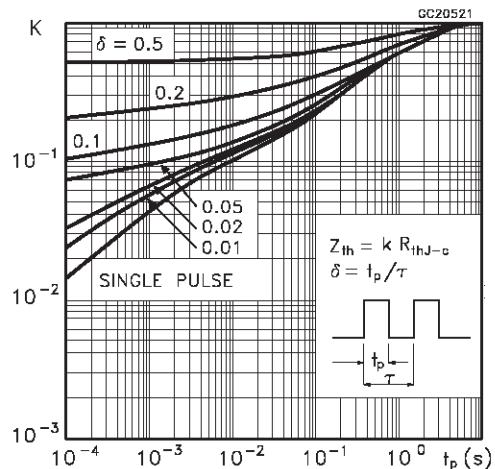


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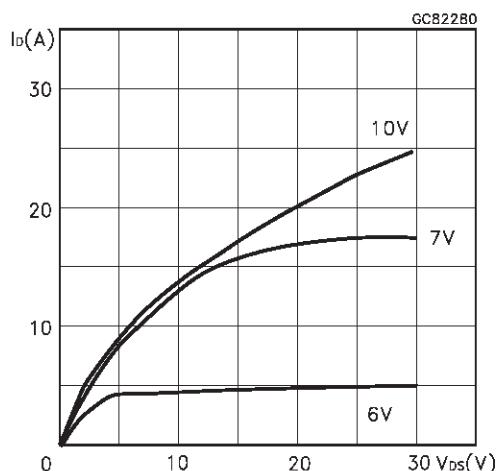
Thermal Impedance for TO-220



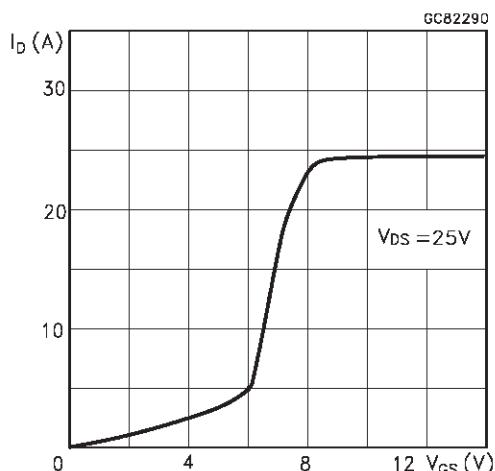
Thermal Impedance for TO-220FP



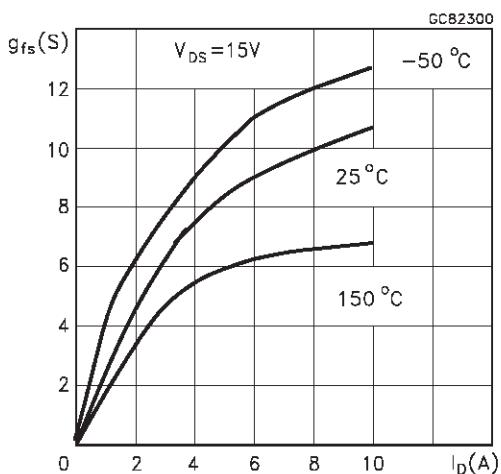
Output Characteristics



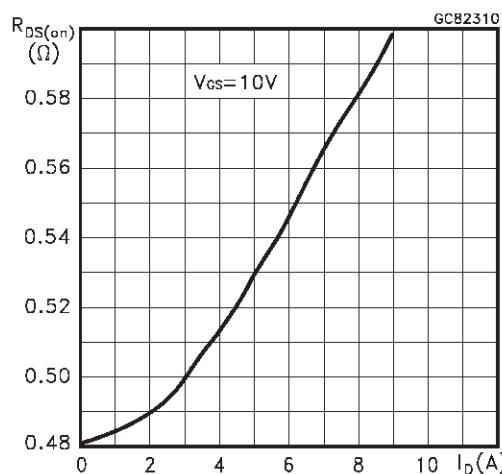
Transfer Characteristics



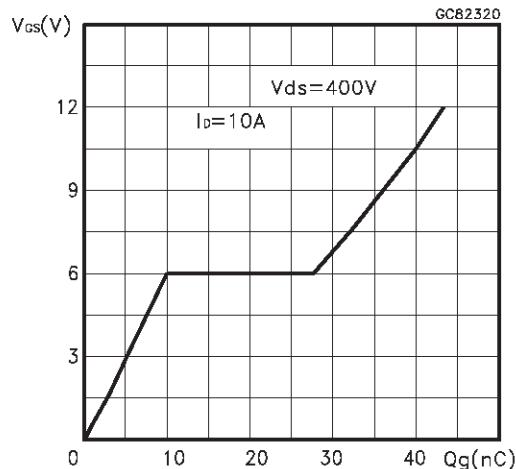
Transconductance



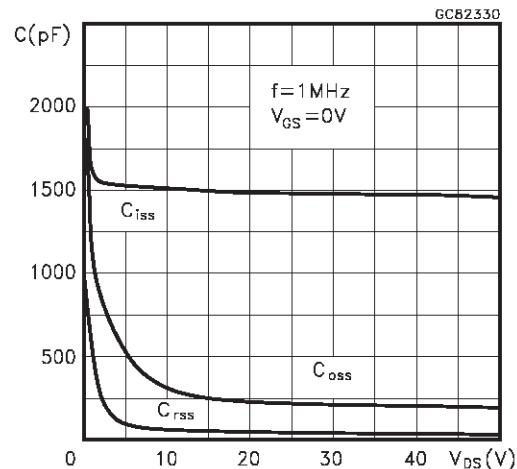
Static Drain-source On Resistance



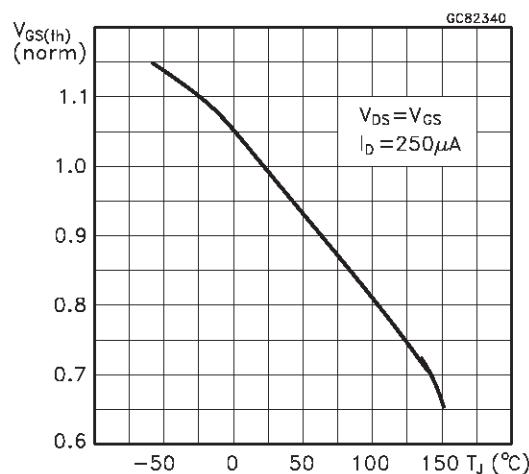
Gate Charge vs Gate-source Voltage



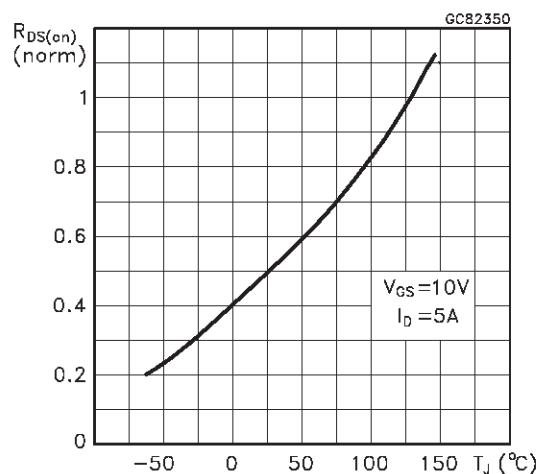
Capacitance Variations



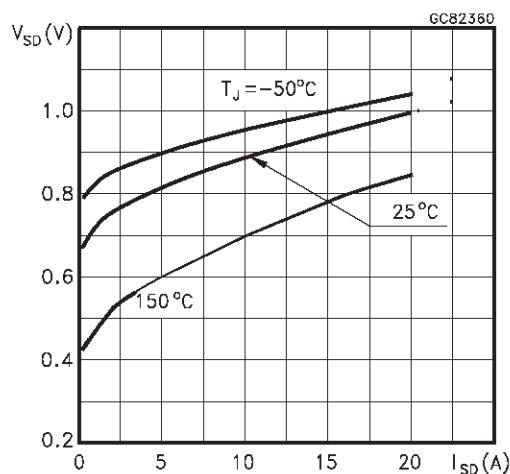
Normalized Gate Threshold Voltage vs Temperature



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

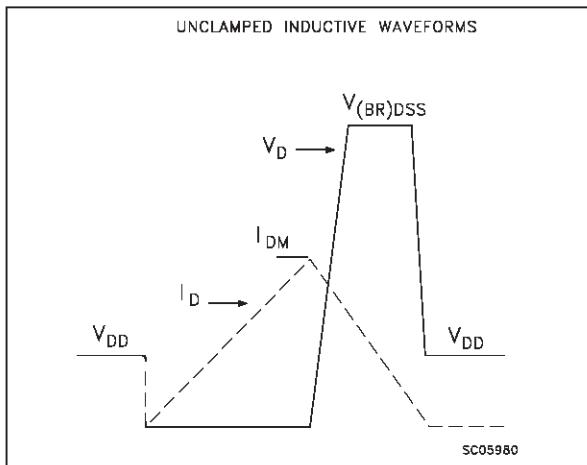


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**Fig. 1:** Unclamped Inductive Load Test Circuit



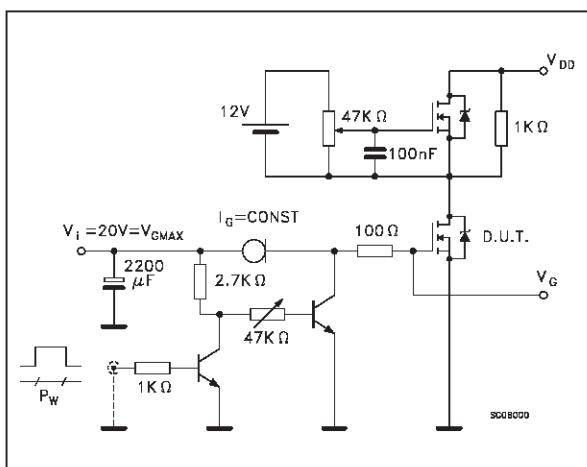
**Fig. 2:** Unclamped Inductive Waveform



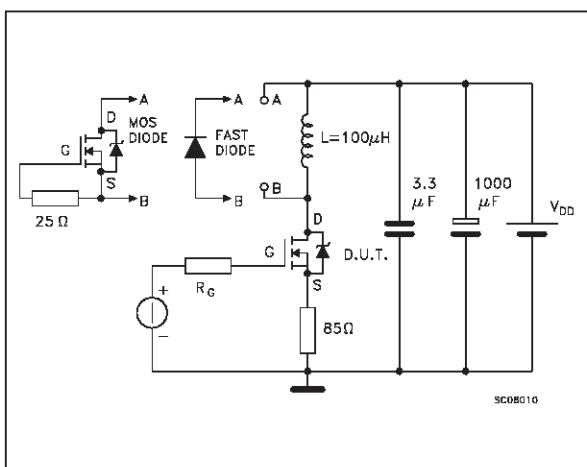
**Fig. 3:** Switching Times Test Circuits For Resistive Load



**Fig. 4:** Gate Charge test Circuit

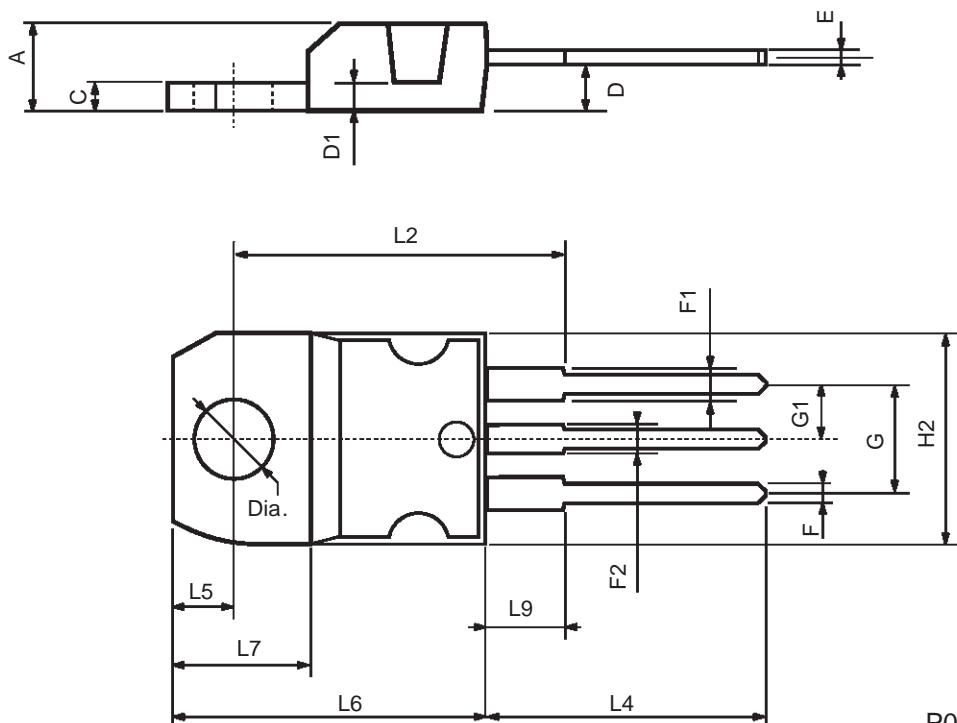


**Fig. 5:** Test Circuit For Inductive Load Switching And Diode Recovery Times



## TO-220 MECHANICAL DATA

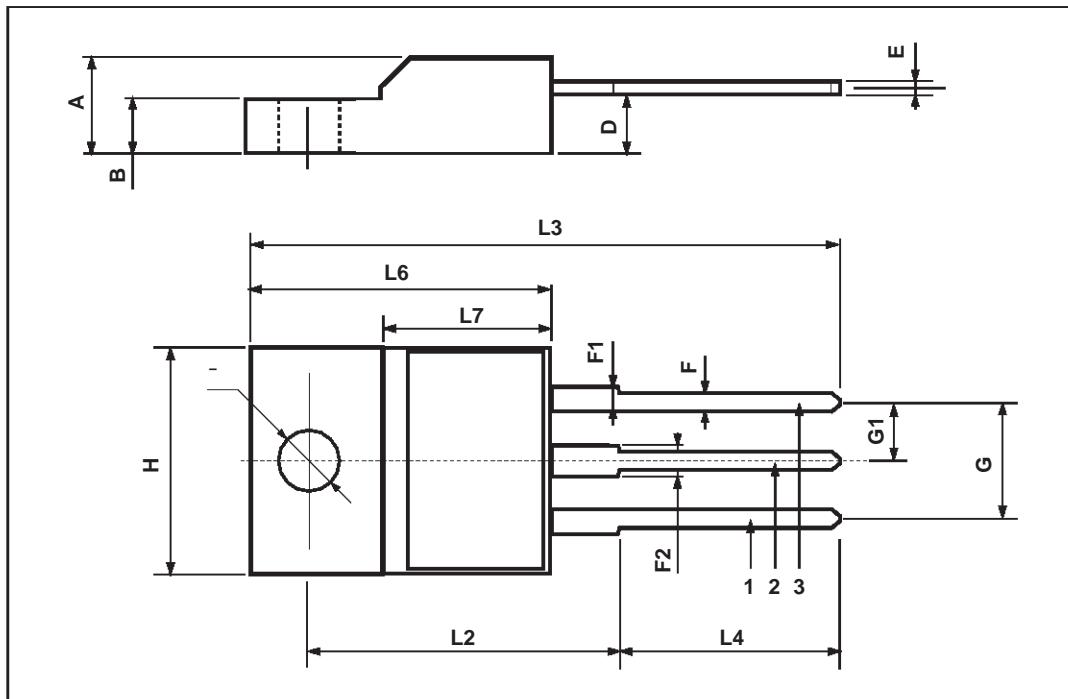
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
D1		1.27			0.050	
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.2		6.6	0.244		0.260
L9	3.5		3.93	0.137		0.154
DIA.	3.75		3.85	0.147		0.151



P011C

**TO-220FP MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	0.385		0.417
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



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