QRR9804
QUALITY & RELIABILITY REPORT

January 1998 to December 1998 - EPROM, Flash Memory, EEPROM and NVRAM Products

INTRODUCTION

STMicroelectronics manufactures a wide range of memory types which include:

Non-volatile memories: Flash memory, UV EPROM, OTP EPROM and EEPROMs. EPROM products are manufactured in both 1.5µ NMOS and 0.8 to 0.6µ CMOS technology; Flash memories in 1.2 to 0.6µ CMOS technology; OTP EPROMs in 0.8 to 0.6µ and EEPROMs in 1.2 to 0.6µ CMOS technology.

Packages for non-volatile memories include both ceramic FDIP and plastic PDIP, PLCC, SO and TSOP.

Non-volatile RAM: ZEROPOWER and TIMEKEEPER ranges are manufactured in 1.2-0.7µ HCMOS technology.

Packages for ZEROPOWER and TIMEKEEPER products use a modified PDIP or SO with an additional "top hat" assembly mounted above and containing a Lithium battery and optionally a quartz crystal. The battery and crystal are sealed in the plastic cap with a plastic resin.

The results presented in this quarterly report cover the tests made from January 1998 to December 1998. Regular reports are issued each quarter with the last years cumulative results.

Director of
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Quality Control & Reliability

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Find the report to the ST web site at **www.st.com**

CONTENT

Table 1. Final Average Outgoing Quality (AOQ)
January 1998 to December 1998

Process	Electrical ppm				Visual ppm			
	1Q98	2Q98	3Q98	4Q98	1Q98	2Q98	3Q98	4Q98
UV EPROM								
CMOS	20	18	7	4	13	19	12	9
NMOS	0	20	0	0	20	20	20	0
OTP EPROM								
CMOS	20	20	19	14	10	8	6	5
FLASH								
CMOS	2	3	9	8	6	6	5	12
NVRAM								
CMOS	0	0	0	0	3	3	0	0
EEPROM								
CMOS	2	4	7	3	8	8	2	7

Table 2. Failure Rate Predictions (Fit)
January 1998 to December 1998

Process	Actual Device hrs		Temperature Activation Energy (eV)	Voltage Acceleration Factor	Equivalent hrs 55 °C (x 10^6)	Life Test Failure	Failure Rate (Fit) Confidence Level	
	Dev. hrs (x 10^6)	Temp. (°C)					60%	90%
UV EPROM								
CMOS E5 -35%	2.206	140	0.6	4.0	605	0	1.5	3.8
CMOS E6 - DM	1.770	140	0.6	4.0	488	0	1.9	4.7
CMOS E6 -10%	3.655	140	0.6	4.0	1,002	0	0.9	2.3
OTP EPROM								
CMOS E5 -35%	2.480	140	0.6	4.0	642	0	1.4	3.6
FLASH								
CMOS T5 -20%	2.551	140	0.6	4.0	661	0	1.3	3.4
CMOS T6	20.058	140	0.6	4.6	5,979	0	0.15	0.38
EEPROM								
CMOS F4S	3.002	140	0.6	3.0	706	0	1.3	3.3
CMOS F6SP	1.731	140	0.6	4.6	624	0	1.6	4.0
NVRAM								
HCMOS S3	1.657	100	0.7	64	2,121	1	0.95	1.8
HCMOS 4DZ	2.215	125	0.7	6.0	1,023	0	0.9	2.2

Table 3. NMOS E3/1.5µm Process UV EPROM Reliability Data, Die Related Tests
January 1998 to December 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M2764A		M27256	
			Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,				
		– 48 hrs	1,020	0	315	0
		– 168 hrs	770	0	-	-
		– 500 hrs	690	0	-	-
		– 1000 hrs	620	0	-	-
Retention Bake	1008	250°C,				
		– 48 hrs	770	0	-	-
		– 168 hrs	770	0	-	-
		– 500 hrs	690	0	-	-

Table 4. CMOS E5/0.8µm Process UV EPROM Reliability Data, Die Related Tests
January 1998 to December 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C64A	
			Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,		
		– 48 hrs	542	0
		– 168 hrs	80	0
		– 500 hrs	80	0
		– 1000 hrs	80	0
Retention Bake	1008	250°C,		
		– 48 hrs	80	0
		– 168 hrs	80	0
		– 500 hrs	80	0

Table 5A. CMOS E5/0.6µm Process (-35% upgrade) UV EPROM Reliability Data, Die Related Tests
January 1998 to December 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C256 (D) M87C257 (D)		M27C512 (D)		M27C1001 (D)		M27C1024 (D)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,								
		– 48 hrs	4,246	0	3,864	0	-	-	-	-
		– 168 hrs	550	0	630	0	-	-	-	-
		– 500 hrs	550	0	550	0	-	-	-	-
		– 1000 hrs	480	0	550	0	-	-	-	-
Retention Bake	1008	250°C,								
		– 48 hrs	550	0	630	0	-	-	-	-
		– 168 hrs	550	0	630	0	-	-	-	-
		– 500 hrs	550	0	550	0	-	-	-	-
		– 1000 hrs	-	-	-	-	-	-	-	-

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 5B. CMOS E5/0.6µm Process (-35% upgrade) UV EPROM Reliability Data, Die Related Tests
January 1998 to December 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C2001 (D)		M27C4002 (D)		M27C801 (D)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,						
		– 48 hrs	160	0	157	0	8,322	0
		– 168 hrs	160	0	80	0	160	0
		– 500 hrs	160	0	80	0	160	0
		– 1000 hrs	160	0	80	0	160	0
Retention Bake	1008	250°C,						
		– 48 hrs	160	0	80	0	160	0
		– 168 hrs	160	0	80	0	160	0
		– 500 hrs	160	0	80	0	160	0
		– 1000 hrs	-	-	-	-	-	-

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 6. CMOS E6/0.6µm Process (-10% upgrade) UV EPROM Reliability Data, Die Related Tests
January 1998 to December 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C1001 (F)		M27C1024 (F)		M27C2001 (F)		M27C4001 (F)		M27C4002 (F)		M27C801 (F)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,												
		– 48 hrs	2,397	0	534	0	1,863	0	1,857	0	550	0	16,339	0
		– 168 hrs	850	0	380	0	470	0	310	0	550	0	470	0
		– 500 hrs	850	0	380	0	390	0	160	0	470	0	390	0
		– 1000 hrs	780	0	380	0	390	0	160	0	470	0	390	0
Retention Bake	1008	250°C,												
		– 48 hrs	850	0	380	0	470	0	310	0	550	0	470	0
		– 168 hrs	850	0	380	0	470	0	310	0	550	0	470	0
		– 500 hrs	850	0	380	0	390	0	160	0	470	0	390	0
		– 1000 hrs	-	-	-	-	-	-	-	-	-	-	-	-

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 7. CMOS E6DM/0.6µm Process UV EPROM Reliability Data, Die Related Tests
January 1998 to December 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C4001 (F)		M27C800 (F)		M27C160 (F)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,						
		– 48 hrs	394	0	8,036	0	11,006	0
		– 168 hrs	240	0	320	0	380	0
		– 500 hrs	240	0	320	0	380	0
		– 1000 hrs	240	0	320	0	380	0
Retention Bake	1008	250°C,						
		– 48 hrs	240	0	320	0	380	0
		– 168 hrs	240	0	320	0	380	0
		– 500 hrs	240	0	320	0	380	0
		– 1000 hrs	-	-	-	-	-	-

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 8. UV EPROM Reliability Data, Package Related Tests (Ceramic Frit-Seal)
January 1998 to December 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	Samp.	Fail
Temperature Cycling	1010	–65 to 150°C, – 100 cycles – 500 cycles – 1000 cycles	 3,645 3,645 3,355	 0 0 0
– Fine Leak – Gross Leak	1014 1014	Test Condition A1 Test Condition C1		
Solderability	2003	245°C, 5sec, Precondition Steam, 1hr	1,100	0
Resistance to Solvents	2015	4 Solvent Solutions	240	0
Lead Integrity	2004	Test Condition B2 (lead fatigue)	176	0
– Fine Leak – Gross Leak	1014 1014	Test Condition A1 Test Condition C1		

Table 9A. CMOS E5/0.6µm Process (–35% Upgrade) OTP EPROM Reliability Data, Die Related Tests
January 1998 to December 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C256 (D) M87C257 (D)		M27C512 (D)		M27C516 (D)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,						
		– 168 hrs	330	0	810	0	480	0
		– 500 hrs	270	0	750	0	480	0
		– 1000 hrs	220	0	700	0	480	0
Retention Bake	1008	150°C,						
		– 168 hrs	330	0	810	0	480	0
		– 500 hrs	270	0	750	0	480	0
		– 1000 hrs	220	0	700	0	480	0
		– 2000 hrs	-	-	-	-	-	-

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 9B. CMOS E5/0.6µm Process (–35% Upgrade) OTP EPROM Reliability Data, Die Related Tests
January 1998 to December 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C1001 (D)		M27C1024 (D)		M27C2001 (D)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,						
		– 168 hrs	300	0	300	0	410	0
		– 500 hrs	300	0	300	0	410	0
		– 1000 hrs	300	0	300	0	410	0
Retention Bake	1008	150°C,						
		– 168 hrs	300	0	300	0	410	0
		– 500 hrs	300	0	300	0	410	0
		– 1000 hrs	300	0	300	0	410	0
		– 2000 hrs	-	-	-	-	-	-

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 10A. CMOS E5/0.6µm Process (–35% Upgrade) OTP EPROM Reliability Data, Package Related Tests
January 1998 to December 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C256 (D) M87C257 (D)		M27C512 (D)		M27C516 (D)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,						
		– 168 hrs	330	0	810	0	480	0
		– 500 hrs	270	0	750	0	480	0
		– 1000 hrs	220	0	700	0	480	0
		– 2000 hrs	-	-	-	-	-	-
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,						
		– 48 hrs	140	0	335	0	200	0
		– 96 hrs	140	0	335	0	200	0
		– 168 hrs	110	0	260	0	175	0
		– 240 hrs	65	0	90	0	75	0
Pressure Pot		121°C, 2Atm,						
		– 48 hrs	330	0	750	0	480	0
		– 96 hrs	330	0	750	0	480	0
		– 168 hrs	330	0	750	0	480	0
		– 240 hrs	270	0	750	0	480	0
Temperature Cycling	1010	–65 to 150°C,						
		– 100 cycles	217	0	640	0	480	0
		– 500 cycles	217	0	640	0	480	0
		– 1000 cycles	217	0	640	0	480	0
Solderability								
– PLCC/TSOP Packages	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	(See cumulative data on Table 10B)					
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	(See cumulative data on Table 10B)					
Resistance to solvents	2015	4 Solvent Solutions	(See cumulative data on Table 10B)					

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 10B. CMOS E5/0.6µm Process (–35% Upgrade) OTP EPROM Reliability Data, Package Related Tests
January 1998 to December 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C1001 (D)		M27C1024 (D)		M27C2001 (D)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,						
		– 168 hrs	300	0	300	0	410	0
		– 500 hrs	300	0	300	0	410	0
		– 1000 hrs	300	0	300	0	410	0
		– 2000 hrs	-	-	-	-	-	-
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,						
		– 48 hrs	105	0	125	0	175	0
		– 96 hrs	105	0	125	0	175	0
		– 168 hrs	75	0	75	0	95	0
		– 240 hrs	25	0	25	0	70	0
Pressure Pot		121°C, 2Atm,						
		– 48 hrs	300	0	300	0	410	0
		– 96 hrs	300	0	300	0	410	0
		– 168 hrs	300	0	300	0	410	0
		– 240 hrs	300	0	300	0	410	0
Temperature Cycling	1010	–65 to 150°C,						
		– 100 cycles	300	0	300	0	410	0
		– 500 cycles	300	0	300	0	410	0
		– 1000 cycles	300	0	300	0	410	0
Solderability								
– PLCC/TSOP Packages	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	Cumulative Sample/Fail = 775/0					
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	Cumulative Sample/Fail = 105/0					
Resistance to solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 292/0					

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 11. CMOS E6/0.6µm Process (–10% Upgrade) OTP EPROM Reliability Data, Die Related Tests
January 1998 to December 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C1001 (F)		M27C1024 (F)		M27C2001 (F)		M27C4001 (F)		M27C4002 (F)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,										
		– 168 hrs	950	0	210	0	50	0	110	0	160	0
		– 500 hrs	780	0	150	0	50	0	50	0	100	0
		– 1000 hrs	730	0	100	0	-	-	-	-	100	0
Retention Bake	1008	150°C,										
		– 168 hrs	1,050	0	100	0	50	0	110	0	160	0
		– 500 hrs	880	0	150	0	50	0	50	0	100	0
		– 1000 hrs	830	0	210	0	-	-	-	-	100	0
		– 2000 hrs	-	-	-	-	-	-	-	-	-	-

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 12. CMOS E6/0.6µm Process (–10% Upgrade) OTP EPROM Reliability Data, Package Related Tests
January 1998 to December 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C1001 (F)		M27C1024 (F)		M27C2001 (F)		M27C4001 (F)		M27C4002 (F)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,										
		– 168 hrs	1,050	0	210	0	50	0	110	0	160	0
		– 500 hrs	880	0	150	0	50	0	50	0	100	0
		– 1000 hrs	830	0	100	0	-	-	-	-	100	0
		– 2000 hrs	-	-	-	-	-	-	-	-	-	-
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,										
		– 48 hrs	440	0	85	0	20	0	45	0	65	0
		– 96 hrs	440	0	85	0	20	0	45	0	65	0
		– 168 hrs	235	0	40	0	-	-	-	-	65	0
		– 240 hrs	90	0	-	-	-	-	-	-	40	0
Pressure Pot		121°C, 2Atm,										
		– 48 hrs	880	0	150	0	50	0	50	0	100	0
		– 96 hrs	880	0	150	0	50	0	50	0	100	0
		– 168 hrs	880	0	150	0	50	0	50	0	100	0
		– 240 hrs	870	0	100	0	50	0	-	-	100	0
Temperature Cycling	1010	–65 to 150°C,										
		– 100 cycles	756	0	150	0	50	0	50	0	100	0
		– 500 cycles	756	0	150	0	50	0	50	0	100	0
		– 1000 cycles	706	0	100	0	-	-	-	-	100	0
Solderability			Cumulative Sample/Fail = 240/0									
– PLCC Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs										
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs										
Resistance to solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 76/0									

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 13. CMOS E6DM/0.6µm Process OTP EPROM Reliability Data, Die Related Tests
January 1998 to December 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C4001 (F)		M27C800 (F)		M27C160 (F)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,						
		– 168 hrs	180	0	120	0	180	0
		– 500 hrs	180	0	120	0	180	0
		– 1000 hrs	180	0	120	0	180	0
Retention Bake	1008	150°C,						
		– 168 hrs	180	0	120	0	180	0
		– 500 hrs	180	0	120	0	180	0
		– 1000 hrs	180	0	120	0	180	0
		– 2000 hrs	-	-	-	-	-	-

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 14. CMOS E6DM/0.6µm Process OTP EPROM Reliability Data, Package Related Tests
January 1998 to December 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C4001 (F)		M27C800 (F)		M27C160 (F)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs – 2000 hrs	 180 180 180 -	 0 0 0 -	 120 120 120 -	 0 0 0 -	 180 180 180 -	 0 0 0 -
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V, – 48 hrs – 96 hrs – 168 hrs – 240 hrs	 75 75 50 25	 0 0 0 0	 50 50 25 -	 0 0 0 -	 80 80 50 50	 0 0 0 0
Pressure Pot		121°C, 2Atm, – 48 hrs – 96 hrs – 168 hrs – 240 hrs	 180 180 180 180	 0 0 0 0	 120 120 120 120	 0 0 0 0	 180 180 180 180	 0 0 0 0
Temperature Cycling	1010	–65 to 150°C, – 100 cycles – 500 cycles – 1000 cycles	 180 180 180	 0 0 0	 120 120 120	 0 0 0	 180 180 180	 0 0 0
Solderability								
– PLCC/TSOP Packages	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	Cumulative Sample/Fail = 116/0					
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	Cumulative Sample/Fail = 44/0					
Resistance to solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 52/0					

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 15. CMOS T5/0.8µm Process (–20% upgrade) Flash Memory Reliability Data, Die Related Tests
January 1998 to December 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F256 (B)		M28F512 (B)		M28F101 (B)		M28F102 (B)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test (1)	1005	140°C, V_{CC} = 6V,f = 500kHz,								
		– 24 hrs	180	0	645	0	28,627	0	8,468	0
		– 168 hrs	180	0	520	0	610	0	530	0
		– 500 hrs	180	0	460	0	580	0	530	0
		– 1000 hrs	180	0	460	0	470	0	480	0
Retention Bake (1)	1008	150°C,								
		– 168 hrs	180	0	520	0	430	0	530	0
		– 500 hrs	180	0	460	0	370	0	530	0
		– 1000 hrs	60	0	460	0	320	0	480	0
Retention Bake	1008	250°C,								
		– 168 hrs	-	-	-	-	376	0	60	0
		– 500 hrs	-	-	-	-	376	0	60	0
		– 1000 hrs	-	-	-	-	376	0	-	-
Write/Erase Cycling		1,000 cycles	1,184	0	4,667	0	8,243	0	13,280	0
		10,000 cycles	-	-	-	-	797	0	-	-
Retention Bake	1008	150°C, 36 hrs	1,184	0	4,667	0	7,446	0	13,280	0

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.
1. A quarter of sample size was subjected to 10,000 Write/Erase cycles before operating life test and retention bake.

Table 16. CMOS T5/0.8µm Process (–20% upgrade) Flash Memory Reliability Data, Package Related Tests
January 1998 to December 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F256 (B)		M28F512 (B)		M28F101 (B)		M28F102 (B)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,								
		– 168 hrs	180	0	520	0	640	0	530	0
		– 500 hrs	180	0	460	0	580	0	530	0
		– 1000 hrs	180	0	460	0	530	0	480	0
		– 2000 hrs	-	-	-	-	-	-	-	-
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,								
		– 48 hrs	90	0	220	0	295	0	245	0
		– 96 hrs	90	0	220	0	295	0	245	0
		– 168 hrs	90	0	220	0	295	0	245	0
		– 240 hrs	-	-	165	0	90	0	95	0
Pressure Pot		121°C, 2Atm,								
		– 48 hrs	180	0	460	0	580	0	530	0
		– 96 hrs	180	0	460	0	580	0	530	0
		– 168 hrs	180	0	360	0	530	0	530	0
		– 240 hrs	180	0	360	0	530	0	530	0
Temperature Cycling	1010	–65 to 150°C,								
		– 100 cycles	120	0	400	0	546	0	530	0
		– 500 cycles	120	0	400	0	496	0	530	0
		– 1000 cycles	120	0	400	0	436	0	480	0
Thermal Shock	1011	–55 to 125°C,								
		– 100 cycles	-	-	-	-	-	-	-	-
		– 500 cycles	-	-	-	-	-	-	-	-
Solderability										
– TSOP/PLCC Packages	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	Cumulative Sample/Fail = 405/0							
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	Cumulative Sample/Fail = 90/0							
Resistance to solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 172/0							

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 17A. CMOS T6/0.6µm Process Flash Memory Reliability Data, Die Related Tests
January 1998 to December 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F201 (B)		M28F210 (C) M28F211 (C) M28F220 (C)		M28F411 (C) M28F410 (C) M28F420 (C)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test (1)	1005	140°C, V_{CC} = 6V,f = 500kHz,						
		– 24 hrs	14,860	0	121,413	0	16,407	0
		– 168 hrs	120	0	530	0	60	0
		– 500 hrs	120	0	530	0	60	0
		– 1000 hrs	120	0	480	0	60	0
Retention Bake (1)	1008	150°C,						
		– 168 hrs	120	0	530	0	60	0
		– 500 hrs	120	0	530	0	60	0
		– 1000 hrs	120	0	480	0	60	0
Retention Bake	1008	250°C,						
		– 168 hrs	361	0	-	-	180	0
		– 500 hrs	361	0	-	-	180	0
		– 1000 hrs	361	0	-	-	180	0
Write/Erase Cycling		1,000 cycles	1,632	0	12,923	0	1,824	0
		10,000 cycles	-	-	-	-	64	0
		100,000 cycles	-	-	-	-	-	-
		200,000 cycles	-	-	-	-	-	-
Retention Bake	1008	150°C, 36 hrs	1,632	0	12,923	0	1,760	0

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.
1. A quarter of sample size was subjected to 10,000 Write/Erase cycles before operating life test and retention bake.

Table 17B. CMOS T6/0.6µm Process Flash Memory Reliability Data, Die Related Tests
January 1998 to December 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M29F102 M29F105		M29F002		M29F200 M29F100		M29F040 (C) M29W040		M29F400 M29W400	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test (1)	1005	140°C, V_{CC} = 6V,f = 500kHz,										
		– 24 hrs	203,297	0	62,132	0	33,998	0	153,230	0	107,849	0
		– 168 hrs	170	0	170	0	230	0	1,170	0	650	0
		– 500 hrs	170	0	110	0	230	0	1,170	0	650	0
		– 1000 hrs	170	0	110	0	230	0	1,170	0	650	0
Retention Bake (1)	1008	150°C,										
		– 168 hrs	270	0	170	0	230	0	750	0	590	0
		– 500 hrs	270	0	110	0	230	0	750	0	590	0
		– 1000 hrs	170	0	110	0	230	0	750	0	590	0
Retention Bake	1008	250°C,										
		– 168 hrs	120	0	126	0	51	0	617	0	162	0
		– 500 hrs	120	0	126	0	51	0	617	0	162	0
		– 1000 hrs	120	0	66	0	51	0	617	0	162	0
Write/Erase Cycling		1,000 cycles	21,761	0	8,359	0	3,520	0	18,796	0	12,058	0
		10,000 cycles	671	0	64	0	-	-	896	0	671	0
		100,000 cycles	63	0	-	-	-	-	478	0	319	0
		200,000 cycles	-	-	-	-	-	-	63	0	60	0
Retention Bake	1008	150°C, 36 hrs	21,090	0	8,295	0	3,520	0	18,019	0	11,387	0

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.
1. A quarter of sample size was subjected to 10,000 Write/Erase cycles before operating life test and retention bake.

Table 18A. CMOS T6/0.6µm Process Flash Memory Reliability Data, Package Related Tests
January 1998 to December 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F201 (B)		M28F211 (C) M28F210 (C) M28F220 (C)		M28F411 (C) M28F410 (C) M28F420 (C)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,						
		– 168 hrs	120	0	530	0	60	0
		– 500 hrs	120	0	530	0	60	0
		– 1000 hrs	120	0	480	0	60	0
		– 2000 hrs	-	-	-	-	-	-
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,						
		– 48 hrs	60	0	240	0	30	0
		– 96 hrs	60	0	240	0	30	0
		– 168 hrs	60	0	240	0	30	0
		– 240 hrs	-	-	95	0	-	-
Pressure Pot		121°C, 2Atm,						
		– 48 hrs	120	0	530	0	60	0
		– 96 hrs	120	0	530	0	60	0
		– 168 hrs	120	0	530	0	60	0
		– 240 hrs	120	0	530	0	60	0
Temperature Cycling	1010	–65 to 150°C,						
		– 100 cycles	60	0	530	0	60	0
		– 500 cycles	60	0	530	0	60	0
		– 1000 cycles	60	0	530	0	60	0
Thermal Shock	1011	–55 to 125°C,						
		– 100 cycles	-	-	-	-	-	-
		– 500 cycles	-	-	-	-	-	-
Solderability								
– TSOP/SO Packages	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	(See cumulative data on Table 18B)					
Resistance to solvents	2015	4 Solvent Solutions	(See cumulative data on Table 18B)					

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 18B. CMOS T6/0.6µm Process Flash Memory Reliability Data, Package Related Tests
January 1998 to December 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M29F102 M29F105		M29F002		M29F200 M29F100		M29F040 (C) M29W040		M29F400 M29W400	
			Fail	Fail	Samp.	Fail	Samp.	Samp.	Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,										
		– 168 hrs	270	0	170	0	230	0	1,220	0	650	0
		– 500 hrs	270	0	110	0	230	0	1,220	0	650	0
		– 1000 hrs	170	0	110	0	230	0	1,170	0	650	0
		– 2000 hrs	-	-	-	-	-	-	-	-	-	-
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,										
		– 48 hrs	110	0	70	0	110	0	560	0	270	0
		– 96 hrs	110	0	70	0	110	0	560	0	270	0
		– 168 hrs	109	0	70	0	110	0	560	0	270	0
		– 240 hrs	109	0	45	0	20	0	205	0	120	0
Pressure Pot		121°C, 2Atm,										
		– 48 hrs	270	0	110	0	230	0	1,220	0	650	0
		– 96 hrs	270	0	110	0	230	0	1,220	0	650	0
		– 168 hrs	270	0	110	0	230	0	1,120	0	650	0
		– 240 hrs	270	0	110	0	230	0	1,120	0	650	0
Temperature Cycling	1010	–65 to 150°C,										
		– 100 cycles	270	0	110	0	170	0	1,217	0	645	0
		– 500 cycles	270	0	110	0	170	0	1,217	0	642	0
		– 1000 cycles	170	0	110	0	170	0	1,107	0	642	0
Thermal Shock	1011	–55 to 125°C,										
		– 100 cycles	-	-	-	-	-	-	-	-	-	-
		– 500 cycles	-	-	-	-	-	-	-	-	-	-
Solderability												
– TSOP/SO Packages	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	Cumulative Sample/Fail = 530/0									
Resistance to solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 244/0									

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 19. CMOS F4/1.2µm Process EEPROM Reliability Data, Die Related Tests
January 1998 to December 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST93Cxxx	
			Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V,		
		– 24 hrs	7,310	0
		– 168 hrs	1,110	0
		– 500 hrs	1,110	0
		– 1000 hrs	-	-
Retention Bake	1008	150°C,		
		– 168 hrs	700	0
		– 500 hrs	700	0
		– 1000 hrs	700	0
		– 2000 hrs	-	-
Write/Erase Cycling		100,000 cycles	1,090	0
		1,000,000 cycles	545	0
Retention Bake	1008	150°C, 168 hrs	-	-

Table 20. CMOS F4/1.2µm Process EEPROM Reliability Data, Package Related Tests
January 1998 to December 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST93Cxxx	
			Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs – 2000 hrs	 540 540 540 -	 0 0 0 -
Pressure Pot		121°C, 2Atm, – 48 hrs – 96 hrs – 168 hrs – 240 hrs	 1,350 1,350 1,350 700	 0 0 0 0
Temperature Cycling	1010	–65 to 150°C, – 100 cycles – 200 cycles –40 to 150°C, – 500 cycles – 1000 cycles	 1,250 600 - -	 0 0 - -
Soderability				
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	(See cumulative data on Table 24B)	
– SO Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	(See cumulative data on Table 24B)	
Resistance to solvents	2015	4 Solvent Solutions	(See cumulative data on Table 24B)	
Resistance to Surface Mount: – SO Package			(See cumulative data on Table 24B)	

Table 21A. CMOS F4S/1.0µm Process EEPROM Reliability Data, Die Related Tests
January 1998 to December 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST24C01 ST24W01		ST24C02 ST24W02		ST24C04 ST24W04		ST24C08		ST24C16 ST25C16		ST24LC21	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V,												
		– 24 hrs	2,070	0	4,390	0	6,870	0	1,110	0	2,400	0	-	-
		– 168 hrs	470	0	790	0	870	0	310	0	400	0	-	-
		– 500 hrs	470	0	790	0	870	0	310	0	400	0	-	-
		– 1000 hrs	-	-	-	-	-	-	-	-	-	-	-	-
Retention Bake	1008	150°C,												
		– 168 hrs	250	0	450	0	500	0	150	0	250	0	-	-
		– 500 hrs	250	0	450	0	500	0	150	0	250	0	-	-
		– 1000 hrs	250	0	450	0	500	0	150	0	250	0	-	-
		– 2000 hrs	-	-	-	-	-	-	-	-	-	-	-	-
Write/Erase Cycling		100,000 cycles	-	-	3,960	0	2,881	1 (a)	2,134	1 (a)	2,280	0	-	-
		1,000,000 cycles	-	-	1,980	0	2,881	3 (a)	1,067	1 (a)	1,140	0	-	-
Retention Bake	1008	150°C, 168 hrs	-	-	-	-	-	-	-	-	-	-	-	-

Note: a. Single bit fail.
Oxide quality improvements are addressed in two directions:
– Continuous quality improvement by fab task force.
– “Build in” robustness through product and process design.

Table 21B. CMOS F4S/1.0µm Process EEPROM Reliability Data, Die Related Tests
January 1998 to December 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M24C16		M93C06		M93C46		M93C56		M93C66		M28C64D M28C64	
			Samp	Fail	Samp	Fail	Samp	Fail	Samp	Fail	Samp	Fail	Samp	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V,												
		– 24 hrs	-	-	480	0	2,320	0	480	0	960	0	2,110	0
		– 168 hrs	-	-	80	0	320	0	80	0	160	0	2,110	0
		– 500 hrs	-	-	80	0	320	0	80	0	160	0	1,270	0
		– 1000 hrs	-	-	-	-	-	-	-	-	-	-	370	0
Retention Bake	1008	150°C,												
		– 168 hrs	-	-	50	0	200	0	50	0	100	0	580	0
		– 500 hrs	-	-	50	0	200	0	50	0	100	0	580	0
		– 1000 hrs	-	-	50	0	200	0	50	0	100	0	580	0
		– 2000 hrs	-	-	-	-	-	-	-	-	-	-	-	-
Write/Erase Cycling		50,000 cycles	-	-	900	0	900	0	945	0	945	0	-	-
		1,000,000 cycles	-	-	450	0	450	0	473	0	473	0	-	-
Retention Bake	1008	150°C, 168 hrs	-	-	-	-	-	-	-	-	-	-	-	-

Table 22A. CMOS F4S/1.0µm Process EEPROM Reliability Data, Package Related Tests
January 1998 to December 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST24C01 ST24W01		ST24C02 ST24W02		ST24C04 ST24W04		ST24C08	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,								
		– 168 hrs	340	0	540	0	180	0	460	0
		– 500 hrs	340	0	540	0	180	0	460	0
		– 1000 hrs	340	0	540	0	180	0	460	0
		– 2000 hrs	-	-	-	-	-	-	-	-
Pressure Pot		121°C, 2Atm,								
		– 48 hrs	900	0	1,250	0	650	0	1,200	0
		– 96 hrs	900	0	1,250	0	650	0	1,200	0
		– 168 hrs	900	0	1,250	0	650	0	1,200	0
		– 240 hrs	400	0	650	0	200	0	600	0
Temperature Cycling	1010	–65 to 150°C,								
		– 100 cycles	750	0	1,100	0	700	0	1,150	0
		– 200 cycles	350	0	500	0	200	0	550	0
		–40 to 150°C,								
		– 500 cycles	-	-	-	-	-	-	-	-
		– 1000 cycles	-	-	-	-	-	-	-	-
Solderability										
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	(See cumulative data on Table 24B)							
– SO Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	(See cumulative data on Table 24B)							
Resistance to solvents	2015	4 Solvent Solutions	(See cumulative data on Table 24B)							
Resistance to Surface Mount:										
– SO Package			(See cumulative data on Table 24B)							

Table 22B. CMOS F4S/1.0µm Process EEPROM Reliability Data, Package Related Tests
January 1998 to December 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST24C16 ST25C16		M24C16		M93C46	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,						
		– 168 hrs	380	0	-	-	160	0
		– 500 hrs	380	0	-	-	160	0
		– 1000 hrs	380	0	-	-	160	0
		– 2000 hrs	-	-	-	-	-	-
Pressure Pot		121°C, 2Atm,						
		– 48 hrs	950	0	-	-	650	0
		– 96 hrs	950	0	-	-	650	0
		– 168 hrs	950	0	-	-	650	0
		– 240 hrs	450	0	-	-	200	0
Temperature Cycling	1010	–65 to 150°C,						
		– 100 cycles	850	0	-	-	400	0
		– 200 cycles	400	0	-	-	200	0
		–40 to 150°C,						
		– 500 cycles	-	-	-	-	-	-
		– 1000 cycles	-	-	-	-	-	-
Solderability								
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	(See cumulative data on Table 24B)					
– SO Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	(See cumulative data on Table 24B)					
Resistance to solvents	2015	4 Solvent Solutions	(See cumulative data on Table 24B)					
Resistance to Surface Mount:								
– SO Package			(See cumulative data on Table 24B)					

Table 22C. CMOS F4S/1.0µm Process EEPROM Reliability Data, Package Related Tests
January 1998 to December 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M93C56		M93C66		M28C64 M28C64D	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,						
		– 168 hrs	40	0	80	0	880	0
		– 500 hrs	40	0	80	0	370	0
		– 1000 hrs	40	0	80	0	370	0
		– 2000 hrs	-	-	-	-	-	-
Pressure Pot		121°C, 2Atm,						
		– 48 hrs	150	0	300	0	1,190	0
		– 96 hrs	150	0	300	0	1,190	0
		– 168 hrs	150	0	300	0	1,070	0
		– 240 hrs	50	0	100	0	950	0
Temperature Cycling	1010	–65 to 150°C,						
		– 100 cycles	100	0	400	0	1,440	0
		– 200 cycles	50	0	100	0	690	0
		–40 to 150°C,						
		– 500 cycles	-	-	-	-	-	-
		– 1000 cycles	-	-	-	-	-	-
Solderability								
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	(See cumulative data on Table 24B)					
– SO Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	(See cumulative data on Table 24B)					
– PLCC Package			(See cumulative data on Table 24B)					
– TSOP Package			(See cumulative data on Table 24B)					
Resistance to solvents	2015	4 Solvent Solutions	(See cumulative data on Table 24B)					
Resistance to Surface Mount:								
– SO Package			(See cumulative data on Table 24B)					
– TSOP Package			(See cumulative data on Table 24B)					
– PLCC Package			(See cumulative data on Table 24B)					

Table 23A. CMOS F6 0,6µm Process EEPROM Reliability Data, Die Related Tests
January 1998 to December 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M24C01		M24C02		M24C04		M24C08	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V,								
		– 24 hrs	2,320	0	4,400	0	2,800	0	2,370	0
		– 168 hrs	320	0	400	0	400	0	320	0
		– 500 hrs	320	0	400	0	400	0	320	0
		– 1000 hrs	-	-	-	-	-	-	-	-
Retention Bake	1008	150°C,								
		– 168 hrs	200	0	250	0	250	0	200	0
		– 500 hrs	200	0	250	0	250	0	200	0
		– 1000 hrs	200	0	250	0	250	0	200	0
		– 2000 hrs	-	-	-	-	-		-	-
Write/Erase Cycling		100,000 cycles	4,606	0	4,606	0	4,606	0	4,200	0
		1,000,000 cycles	2,303	0	2,303	0	2,303	0	2,100	0
Retention Bake	1008	150°C, 168 hrs	-	-	-	-	-	-	-	-

Table 23B. CMOS F6 0,6µm Process EEPROM Reliability Data, Die Related Tests
January 1998 to December 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M24C16		M24C32		M24C64	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V,						
		– 24 hrs	5,280	0	2,400	0	1,840	0
		– 168 hrs	480	0	400	0	240	0
		– 500 hrs	480	0	400	0	240	0
		– 1000 hrs	-	-	-	-	-	-
Retention Bake	1008	150°C,						
		– 168 hrs	300	0	250	0	150	0
		– 500 hrs	300	0	250	0	150	0
		– 1000 hrs	300	0	250	0	150	0
		– 2000 hrs	-	-	-		-	-
Write/Erase Cycling		100,000 cycles	4,200	1 (a)	5,656	0	-	-
		1,000,000 cycles	2,100	1 (a)	2,828	0	-	-
Retention Bake	1008	150°C, 168 hrs	-	-	-	-	-	-

Note: a. Single bit fail.
Oxide quality improvements are addressed in two directions:
– Continuous quality improvement by fab task force.
– “Build in” robustness through product and process design.

Table 24A. CMOS F6 0,6µm Process EEPROM Reliability Data, Package Related Tests
January 1998 to December 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M24C01		M24C02		M24C04		M24C08	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,								
		– 168 hrs	80	0	200	0	280	0	320	0
		– 500 hrs	80	0	200	0	280	0	320	0
		– 1000 hrs	80	0	200	0	280	0	320	0
		– 2000 hrs	-	-	-	-	-	-	-	-
Pressure Pot		121°C, 2Atm,								
		– 48 hrs	600	0	1,050	0	950	0	1,150	0
		– 96 hrs	600	0	1,050	0	950	0	1,150	0
		– 168 hrs	600	0	1,050	0	950	0	1,150	0
		– 240 hrs	100	0	450	0	350	0	450	0
Temperature Cycling	1010	–65 to 150°C,								
		– 100 cycles	450	0	1,200	0	950	0	950	0
		– 200 cycles	100	0	450	0	350	0	450	0
		–40 to 150°C,								
		– 500 cycles	-	-	-	-	-	-	-	-
		– 1000 cycles	-	-	-	-	-	-	-	-
Soderability										
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	(See cumulative data on Table 24B)							
– SO Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	(See cumulative data on Table 24B)							
Resistance to solvents	2015	4 Solvent Solutions	(See cumulative data on Table 24B)							
Resistance to Surface Mount:										
– SO Package			(See cumulative data on Table 24B)							

Table 24B. CMOS F6 0,6µm Process EEPROM Reliability Data, Package Related Tests
January 1998 to December 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M24C16		M24C32		M24C64	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,						
		– 168 hrs	120	0	80	0	-	-
		– 500 hrs	120	0	80	0	-	-
		– 1000 hrs	120	0	80	0	-	-
		– 2000 hrs	-	-	-	-	-	-
Pressure Pot		121°C, 2Atm,						
		– 48 hrs	500	0	250	0	300	0
		– 96 hrs	500	0	250	0	300	0
		– 168 hrs	500	0	250	0	300	0
		– 240 hrs	250	0	100	0	-	-
Temperature Cycling	1010	–65 to 150°C,						
		– 100 cycles	500	0	250	0	600	0
		– 200 cycles	250	0	100	0	300	0
		–40 to 150°C,						
		– 500 cycles	-	-	-	-	-	-
		– 1000 cycles	-	-	-	-	-	-
Solderability								
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	Cumulative Sample/Fail = 25/0					
– SO Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	Cumulative Sample/Fail = 25/0					
– PLCC Package			Cumulative Sample/Fail = 25/0					
– TSOP Package			Cumulative Sample/Fail = 25/0					
Resistance to solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 192/0					
Resistance to Surface Mount:								
– SO Package			Cumulative Sample/Fail = 11,940/0					
– TSOP Package			Cumulative Sample/Fail = 810/0					
– PLCC Package			Cumulative Sample/Fail = 730/0					

Table 25. HCMOS S3/1.2µm Process ZEROPOWER NVRAM Reliability Data, Die Related Tests
January 1998 to December 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M48T08 M48T18	
			Samp.	Fail
Operating Life Test	1005	125°C, V_{CC} = 7V, f = 1MHz, – 168 hrs – 500 hrs – 1000 hrs	 1,958 1,599 1,595	 0 0 1(a)

Note: a. Slightly elevated standby current due to gate oxide breakdown in P Channel pull down transistor in the periphery of the die.

Table 26. HCMOS S3/1.2µm Process ZEROPOWER NVRAM Reliability Data, Package Related Tests
January 1998 to December 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M48T08 M48T18	
			Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs	 847 846 767	 0 0 0
Temperature Cycling Caphat	1010	–40 to 100°C, – 100 cycles – 500 cycles – 1000 cycles	 800 - -	 0 - -
Resistance to solvents	2015	4 Solvent Solutions	80	0

Table 27. HCMOS 4DZ/0.8µm Process ZEROPOWER NVRAM Reliability Data, Die Related Tests
January 1998 to December 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M48T35 M48T35Y		M48T58 M48T58Y M48T559Y	
			Samp.	Fail	Samp.	Fail
Operating Life Test	1005	125°C, V_{CC} = 6V, f = 1MHz,				
		– 168 hrs	-	-	1,259	0
		– 500 hrs	-	-	1,256	0
		– 1000 hrs	-	-	1,244	0
		– 2000 hrs	-	-	-	-

Table 28. HCMOS 4DZ/0.8µm Process ZEROPOWER NVRAM Reliability Data, Package Related Tests
January 1998 to December 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M48T35 M48T35Y		M48T58 M48T58Y M48T559Y	
			Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,				
		– 168 hrs	-	-	539	0
		– 500 hrs	-	-	533	0
		– 1000 hrs	-	-	530	0
Hast	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,				
		– 96 hrs	-	-	-	-
		– 168 hrs	-	-	-	-
		– 240 hrs	-	-	-	-
Temperature Cycling	1010	–65 to 150°C,				
		– 100 cycles	-	-	640	0
		– 500 cycles	-	-	640	0
		– 1000 cycles	-	-	478	0
Resistance to solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 60/0			

Table 29. HCMOS 4DZ/0.7µm Process ZEROPOWER HYBRID MODULE Reliability Data, Die Related Tests
January 1998 to December 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M48T37Y (5V)	
			Samp.	Fail
Operating Life Test	1005	125°C, V_{CC} = 6V, f = 1MHz, – 168 hrs – 500 hrs – 1000 hrs – 2000 hrs	 967 967 963 -	 0 0 0 -

Table 30. HCMOS 4DZ/0.7µm Process ZEROPOWER HYBRID MODULE Reliability Data, Package Related Tests
January 1998 to December 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M48T37Y (5V)	
			Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs	 - - -	 - - -
Hast	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V, – 96 hrs – 168 hrs – 240 hrs	 171 171 -	 0 0 -
Temperature Cycling	1010	–40 to 100°C, – 100 cycles – 500 cycles – 1000 cycles	 299 259 258	 0 0 0
Resistance to solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 72/0	

Table 31. ZEROPOWER HYBRID MODULE Reliability Data, Die Related Tests
January 1998 to December 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M48Z512A M48Z2M1		M48Z128 M48Z30	
			Samp.	Fail	Samp.	Fail
Operating Life Test	1005	125°C, V_{CC} = 6V, f = 1MHz,				
		– 168 hrs	-	-	135	0
		– 500 hrs	-	-	134	0
		– 1000 hrs	-	-	89	0
		– 2000 hrs	-	-	-	-

Table 32. ZEROPOWER HYBRID MODULE Reliability Data, Package Related Tests
January 1998 to December 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M48Z512A M48Z2M1		M48Z128 M48Z30	
			Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,				
		– 168 hrs	-	-	104	0
		– 500 hrs	-	-	62	0
		– 1000 hrs	-	-	62	0
Hast	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,				
		– 96 hrs	-	-	-	-
		– 168 hrs	-	-	-	-
		– 240 hrs	-	-	-	-
Temperature Cycling	1010	–40 to 100°C,				
		– 100 cycles	-	-	135	0
		– 500 cycles	-	-	-	-
		– 1000 cycles	-	-	-	-
Resistance to solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = -/-			

Table 33. Statistical Process Control: CMOS E5/0.6µm Process (–35% upgrade) UV EPROM and OTP EPROM, Agrate - Italy F8 Diffusion Line

Key Process Parameters	1Q98	2Q98	3Q98	4Q98
	CPK	CPK	CPK	CPK
Pad Oxide Thickness	2.2	2.66	(*)	(*)
Silicon Nitride Thickness	1.7	1.85	(*)	(*)
Field Oxide Thickness	2.61	3.47	(*)	(*)
Gate Oxide Thickness	2.06	2.20	(*)	(*)
Interpoly Oxide Thickness	2.4	2.58	(*)	(*)
Intermediate Dielectric Thickness	1.71	1.7	(*)	(*)
Polysilicon 1 Thickness	1.91	2.72	(*)	(*)
Active Area Critical Dimensions	2.51	1.75	(*)	(*)
Policide Critical Dimensions	1.6	2.00	(*)	(*)

Key Electrical Parameters	1Q98	2Q98	3Q98	4Q98
	CPK	CPK	CPK	CPK
VT N-Channel Square Tr.	1.74	3.94	(*)	(*)
VT P-Channel Square Tr.	2.56	2.17	(*)	(*)
VT Natural Square Tr.	4.74	3.92	(*)	(*)
VT Memory Cell	2.22	1.9	(*)	(*)
I_{DON} N-Channel	3.1	3.48	(*)	(*)
N+ Active Area Contact Chain	9.67	5.85	(*)	(*)
AL-W Silicide Contact Chain Resistance	5.99	1.92	(*)	(*)

Note: (*) No production data during 3Q98, 4Q98.

Table 34. Statistical Process Control: CMOS E6DM/0.6µm Process UV EPROM and OTP EPROM, Phoenix - USA PF1 Diffusion Line

Key Process Parameters	1Q98	2Q98	3Q98	4Q98
	CPK	CPK	CPK	CPK
Pad Oxide Thickness	1.97	2.02	(*)	(*)
Silicon Nitride Thickness	1.63	1.78	(*)	(*)
Field Oxide Thickness	2.86	5.20	(*)	(*)
Gate Oxide Thickness	2.18	2.76	(*)	(*)
Interpoly Oxide Thickness	1.35	1.34	(*)	(*)
Intermediate Dielectric Thickness	1.34	1.34	(*)	(*)
Polysilicon 1 Thickness	4.56	2.90	(*)	(*)
Active Area Critical Dimensions	2.34	2.06	(*)	(*)
Policide Critical Dimensions	2.64	1.37	(*)	(*)

Key Electrical Parameters	1Q98	2Q98	3Q98	4Q98
	CPK	CPK	CPK	CPK
VT N-Channel Square Tr.	3.09	3.08	(*)	(*)
VT P-Channel Square Tr.	1.67	1.60	(*)	(*)
VT Natural Square Tr.	3.92	4.55	(*)	(*)
VT Memory Cell	1.61	1.15 (1)	(*)	(*)
I_{DON} N-Channel	1.73	1.14 (1)	(*)	(*)
N+ Active Area Contact Chain	4.61	4.77	(*)	(*)
AL-W Silicide Contact Chain Resistance	1.59	1.35	(*)	(*)

Note: (*) No production data during 3Q98, 4Q98.
1. Photo spec. retargeted at poly gate.

Table 35. Statistical Process Control: CMOS E6/0.6µm Process (–10% upgrade) UV EPROM and OTP EPROM, Agrate - Italy F8 Diffusion Line

Key Process Parameters	1Q98	2Q98	3Q98	4Q98
	CPK	CPK	CPK	CPK
Pad Oxide Thickness	-	2.27	2.22	2.17
Silicon Nitride Thickness	-	1.33	1.94	1.59
Field Oxide Thickness	-	2.03	3.12	3.70
Gate Oxide Thickness	-	2.20	1.72	1.99
Interpoly Oxide Thickness	-	2.58	2.37	2.03
Intermediate Dielectric Thickness	-	1.72	1.62	1.59
Polysilicon 1 Thickness	-	2.72	1.97	2.46
Active Area Critical Dimensions	-	2.43	2.26	3.68
Policide Critical Dimensions	-	2.07	2.03	1.59

Key Electrical Parameters	1Q98	2Q98	3Q98	4Q98
	CPK	CPK	CPK	CPK
VT N-Channel 10 x 10µm	-	2.33	4.35	3.89
VT P-Channel 10 x 10µm	-	2.53	2.08	3.27
VT Natural 10 x 10µm	-	1.35	2.31	1.93
VT Memory Cell 0.65 x 0.65µm	-	1.33	1.51	1.56
I_{DON} N-Channel 10 x 10µm	-	2.01	3.15	2.04
N+ Active Area Contact Chain	-	5.6	2.87	4.01
AL-W Silicide Contact Chain Resistance	-	2.22	2.05	1.87

Table 36. Statistical Process Control: CMOS E6/0.6µm Process (–10% upgrade) UV EPROM and OTP EPROM, Catania - Italy M5 Diffusion Line

Key Process Parameters	1Q98	2Q98	3Q98	4Q98
	CPK	CPK	CPK	CPK
Pad Oxide Thickness	-	1.38	1.55	1.62
Silicon Nitride Thickness	-	1.33	1.38	1.42
Field Oxide Thickness	-	2.59	2.87	2.59
Gate Oxide Thickness	-	1.81	2.08	1.81
Interpoly Oxide Thickness	-	1.57	1.48	1.57
N-Well Oxidation	-	3.74	3.53	3.74
Polysilicon 1 Thickness	-	1.51	1.68	1.51
Active Area Critical Dimensions	-	2.4	2.98	2.95
Policide Critical Dimensions	-	1.44	1.95	1.94

Key Electrical Parameters	1Q98	2Q98	3Q98	4Q98
	CPK	CPK	CPK	CPK
VT N-Channel Square Tr.	-	4.12	1.73	2.91
VT P-Channel Square Tr.	-	2.76	2.72	3.10
VT Natural Square Tr.	-	4.34	1.52	2.08
VT Memory Cell	-	1.33	1.44	1.34
I_{DON} N-Channel	-	2.72	2.62	2.60
N+ Active Area Contact Chain	-	5.51	6.01	6.20
AL-W Silicide Contact Chain Resistance	-	2.22	1.72	2.97

Table 37. Statistical Process Control: CMOS T5/0.8µm Process (-20% upgrade) Flash Memory, Agrate - Italy F8 Diffusion Line

Key Process Parameters	1Q98	2Q98	3Q98	4Q98
	CPK	CPK	CPK	CPK
Field Oxide Thickness	2.15	2.44	2.23	2.83
Polysilicon 1 Thickness	2.96	3.64	2.81	4.37
Gate Oxide Thickness	1.82	2.61	1.88	2.01
Tunnel Oxide Thickness	2.23	2.79	2.65	2.60
ONO Bottom Oxide Thickness	2.22	2.06	1.80	2.12
ONO Nitride Thickness	1.92	1.34	1.67	2.19
ONO Top Oxide Thickness	2.67	2.00	2.21	2.58
Active Area Critical Dimensions	2.96	1.73	2.26	1.67
Polysilicon 2 Critical Dimensions	1.69	2.39	2.49	1.82

Key Electrical Parameters	1Q98	2Q98	3Q98	4Q98
	CPK	CPK	CPK	CPK
VT N-Channel 25 x 25 µm	2.77	2.71	1.55	2.19
VT P-Channel 25 x 25 µm	1.69	2.17	1.80	2.33
BV N-Channel 25 x 0.8 µm	1.63	3.36	1.60	1.37
BV P-Channel 25 x 0.9 µm	3.68	4.11	4.10	3.66
VT Memory Cell 0.8 x 0.8 µm	1.36	3.08	2.24	1.59
I_{DON} N-Channel 25 x 0.8 µm	2.02	1.76	2.63	2.56
Al+N+ Contact Chain	4.58	5.16	4.18	4.53
AL-W Silicide Contact Chain Resistance	1.81	5.76	3.81	3.05

Table 38A. Statistical Process Control: CMOS T6/0.6µm Process Flash Memory, Agrate - Italy R1 Diffusion Line

Key Process Parameters	1Q98	2Q98	3Q98	4Q98
	CPK	CPK	CPK	CPK
Field Oxide Thickness	1.77	1.92	2.07	2.23
First Poly Thickness	1.04 (1)	1.33	2.05	1.97
Gate Oxide HV Thickness	2.48	2.77	3.05	2.94
Tunnel Oxide Thickness	1.92	1.76	2.17	1.66
Gate Oxide LV Thickness	1.94	1.94	2.22	1.83
ONO Bottom Oxide Thickness	1.33	1.37	1.81	1.34
ONO Nitride Thickness	1.88	1.84	1.89	2.15
ONO Top Oxide Thickness	1.90	1.49	1.96	1.83
Active Area CD	2.15	0.97 (2)	1.15 (2)	1.39
Second Poly CD	1.35	0.99 (3)	1.22 (4)	1.05 (5)

Note: 1. The low value of CPK is due to low run uniformity on two furnaces. A modification of hardware has been done on the furnace with good results. At the end of this month the same modification will be done also on the other furnace.
2. New resist and new equipment under evaluation.
3. Low CPK value due to new target.
4. Change in exposure energy according to new target.
5. Fine tuning ongoing to align different production island.

Table 38B. Statistical Process Control: CMOS T6/0.6μm Process Flash Memory, Agrate - Italy R1 Diffusion Line

Key Electrical Parameters	1Q98	2Q98	3Q98	4Q98
	CPK	CPK	CPK	CPK
LV-NCh LVS (10 x 0.8) Saturation Current	3.42	3.34	4.46	4.79
LV-PCh LVS (10 x 0.9) BV	3.10	2.27	5.4	3.39
LV-PCh LVS (10 x 0.9) Saturation Current	1.68	1.34	2.32	3.90
LV-PCh SQ. VTh	1.68	2.65	1.79	2.23
HV-NCh SQ. VTh	1.82	1.88	1.82	2.09
HV-NCh (10 x 1.2) LVS Saturation Current	2.38	3.34	12.2	14.4
HV-PCh (10 x 1.3) BV	2.61	2.27	3.14	3.31
HV-PCh (10 x 1.3) Saturation Current	2.02	3.29	4.96	5.32
HV-PCh SQ. VTh	1.33	1.59	1.46	1.47
UV Erased Cell VTh	1.64	1.36	1.40	1.49
N+ Contact Chain	1.67	2.54	6.33	7.73
Silicide Contact Chain	2.08	2.36	3.11	3.65
LV-NCh (10 x 0.8) BV	3.28	3.63	4.34	4.92

Table 39A. Statistical Process Control: CMOS T6/0.6µm Process Flash Memory, Catania - Italy M5 Diffusion Line

Key Electrical Parameters	1Q98	2Q98	3Q98	4Q98
	CPK	CPK	CPK	CPK
Field Oxide Thickness	1.85	2.19	2.82	2.28
First Poly Thickness	1.49	1.78	1.45	1.39
Gate Oxide HV Thickness	1.34	(*)	1.61	1.48
Tunnel Oxide Thickness	1.84	1.95	1.51	1.75
Gate Oxide LV Thickness	1.33	1.39	1.66	1.45
ONO Bottom Oxide Thickness	1.33	1.33	1.44	1.33
ONO Nitride Thickness	1.78	1.63	1.52	1.34
ONO Top Oxide Thickness	2.3	1.89	1.83	2.35
Active Area CD	1.79	1.57	2.65	1.88
Second Poly CD	1.47	1.92	2.25	1.41

Note: (*).No production during 2Q98.

Table 39B. Statistical Process Control: CMOS T6/0.6µm Process Flash Memory, Catania - Italy M5 Diffusion Line

Key Electrical Parameters	1Q98	2Q98	3Q98	4Q98
	CPK	CPK	CPK	CPK
LV-NCh LVS (10 x 0.8) Saturation Current	5.77	2.45	1.70	2.91
LV-PCh LVS (10 x 0.9) BV	2.61	2.3	2.29	2.41
LV-PCh LVS (10 x 0.9) Saturation Current	1.67	1.89	1.37	1.87
LV-PCh SQ. VTh	1.78	1.73	1.58	1.97
HV-NCh (10 x 1.2) LVS BV	1.57	(*)	1.99	1.6
HV-NCh SQ. VTh	0.98 (1)	(*)	1.53	1.63
HV-NCh (10 x 1.2) LVS Saturation Current	4.15	(*)	3.3	2.8
HV-PCh (10 x 1.3) BV	2.31	(*)	2.44	2.73
HV-PCh (10 x 1.3) Saturation Current	4.38	(*)	2.6	2.3
HV-PCh SQ. VTh	1.44	(*)	1.39	1.36
UV Erased Cell VTh	1.68	1.65	1.88	1.82
N+ Contact Chain	3.84	4.58	3.28	4.51
Silicide Contact Chain	0.92 (2)	1.38	1.35	2.55
LV-NCh (10 x 0.8) BV	2.27	3.05	2.08	3.69

Note: 1. Low CPK due to ox tunnel equipment, now replaced.
2. Low CPK due to one w deposition chamber equipment adjustment in progress.
(*). No production during 2Q98.

Table 40A. Statistical Process Control: CMOS T6XU35/0.35µm Process Flash Memory, Agrate - Italy R1 Diffusion Line

Key Process Parameters	1Q98	2Q98	3Q98	4Q98
	CPK	CPK	CPK	CPK
Field Oxide Thickness	-	-	-	3.16
First Poly Thickness Gate	-	-	-	1.33
Gate Oxide HV Thickness	-	-	-	2.44
Tunnel Oxide Thickness	-	-	-	2.22
Gate Oxide LV Thickness	-	-	-	2.09
ONO Nitride Thickness	-	-	-	1.03 (1)
ONO Top Oxide Thickness	-	-	-	1.01 (1)
Active Area CD	-	-	-	1.33
Second Poly CD	-	-	-	1.37

Note: 1. Process optimization to improve thickness uniformity.

Table 40B. Statistical Process Control: CMOS T6XU35/0.35µm Process Flash Memory, Agrate - Italy R1 Diffusion Line

Key Electrical Parameters	1Q98	2Q98	3Q98	4Q98
	CPK	CPK	CPK	CPK
LV-NCh LVS Saturation Current	-	-	-	1.88
LV-PCh LVS BV	-	-	-	1.65
LV-PCh LVS Saturation Current	-	-	-	1.44
LV-PCh SQ. VTh	-	-	-	1.63
HV-NCh SQ. VTh	-	-	-	2.56
HV-NCh LVS Saturation Current	-	-	-	2.21
HV-PCh BV	-	-	-	4.55
HV-PCh Saturation Current	-	-	-	3.82
HV-NCh LVS BV	-	-	-	3.51
LV-NCh LVS BV	-	-	-	3.20
LV-NCh SQ. VTh	-	-	-	4.41
HV-PCh SQ. VTh	-	-	-	1.39
Word Line Resistant	-	-	-	1.48
UV Erased Cell VTh	-	-	-	0.65 (1)
N+ Contact Chain	-	-	-	1.69

Note: 1. Test structure problem suspected. Further investigation in progress.

Table 41. Statistical Process Control: CMOS F6 0.6µm Process EEPROM Memory, Agrate - Italy F8 Diffusion Line

Key Process Parameters	1Q98	2Q98	3Q98	4Q98
	CPK	CPK	CPK	CPK
Pad Oxide Thickness	-	2.27	2.22	2.17
Silicon Nitride Thickness	-	1.37	1.90	1.86
Field Oxide Thickness	-	2.44	2.23	2.83
Gate Oxide 1 Thickness	-	2.20	1.86	2.23
Gate Oxide 2 Thickness	-	1.90	2.34	1.81
Tunnel Oxide Thickness	-	3.24	2.50	2.62
Dialectric Thickness	-	1.53	1.73	2.20
Active Area Critical Dimensions	-	1.51	1.70	1.81
Policide Critical Dimensions	-	1.77	2.08	1.89
Poly Front Deposition Thickness	-	2.08	1.87	2.21
Contacts Critical Dimension	-	1.62	1.59	1.65

Key Electrical Parameters	1Q98	2Q98	3Q98	4Q98
	CPK	CPK	CPK	CPK
VT N-Channel 10 x 10µm	-	2.35	1.99	2.26
VT P-Channel 10 x 10µm	-	2.61	2.48	2.31
VT Natural 10 x 10µm	-	3.18	1.79	3.56
BV N-Channel 10 x 10µm	-	2.44	2.77	2.26
BV P-Channel 10 x 10µm	-	1.33	2.14	1.42
EBD-LVN	-	5.37	5.43	4.67
N+ Active Area Contact Chain	-	2.56	2.89	3.46
EBD-TUN	-	2.73	1.87	2.92

Table 42. Statistical Process Control: UV EPROM Ceramic Frit-Seal Package Assembly Line, Singapore

Key Process Parameters	1Q98	2Q98	3Q98	4Q98
	CPK	CPK	CPK	CPK
Shear Test (D.A.)	16.11	26.2	4.5	6.9
Stud Pull	1.67	1.57	1.5	1.6
Bond Strength (W.B.)	5.67	5.58	5.5	6.4
SN Thickness (Tin Plate)	1.71	1.77	1.7	1.8

Table 43. Statistical Process Control: TSOP Package Assembly Line, Singapore

Key Process Parameters	1Q98	2Q98	3Q98	4Q98
	CPK	CPK	CPK	CPK
Shear Test (D.A.)	1.78	2.38	2.06	2.33
Ball Shear (W.B.)	2.00	2.65	3.42	3.43
Bond Strength (W.B.)	1.88	2.76	1.67	2.00
Coplanarity	2.83	4.47	2.82	5.47
Plating Thickness	2.24	1.60	2.30	2.03

Table 44. Statistical Process Control: PLCC Package Assembly Line, Singapore

Key Process Parameters	1Q98	2Q98	3Q98	4Q98
	CPK	CPK	CPK	CPK
Shear Test (D.A.)	3.22	3.37	3.5	4.1
Ball Shear (W.B.)	2.13	2.21	2.9	3.2
Bond Strength (W.B.)	1.49	2.10	1.8	1.9
Plating Thickness	2.14	1.90	1.9	1.9
Coplanarity	-	-	6.6	5.7

If you have any questions or suggestion concerning the matters raised in this document please send them to the following electronic mail address:

ask.memory@st.com (for general enquiries)

Please remember to include your name, company, location, telephone number and fax number