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## ST7/ST10/U435 CAN-do SOLUTIONS FOR CAR MULTIPLEXING

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by L. PERIER / A. COEN

Replacing a classical harness with a multiplexing (mux) network makes cars more competitive as it increases their flexibility and simplifies the wiring. CAN is the leading protocol for car mux systems thanks to its large speed spectrum and noise immunity. But each application has specific constraints in terms of protocol, cost and performance. So a single node architecture does not fit all the needs.

This article compares first of all, the major car mux protocols: CAN, J1850 and SCI/UART. The second part describes optimized nodes including microcontrollers (ST725x, ST92F120, ST10F167) with embedded FLASH/ROM and physical line interfaces (U435). Then it presents roadmaps for MCU cores, embedded FLASH memories and super-integrations.

### 1 MULTIPLEXING FOR SMARTER CARS

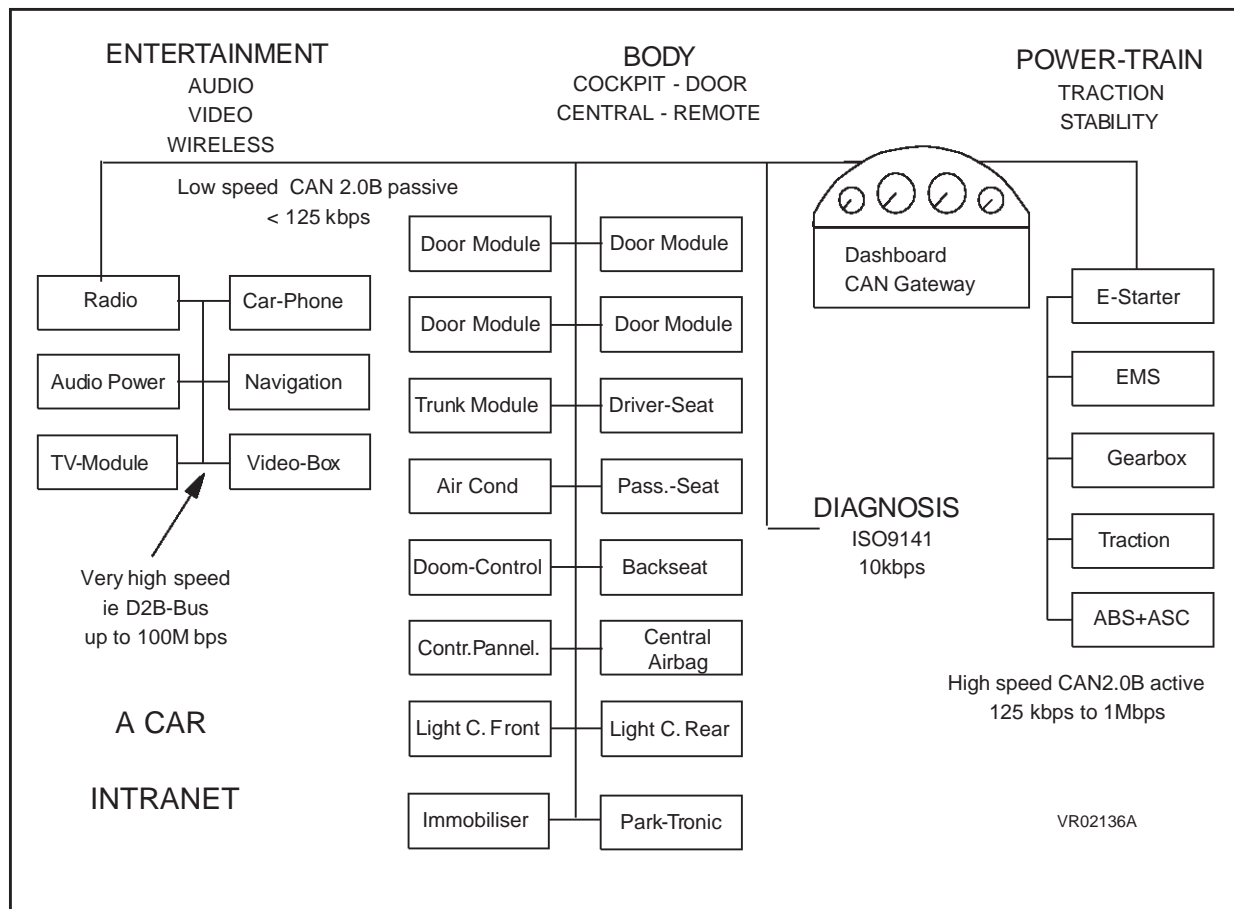
#### 1.1 THE CHALLENGES

Automotive is a tough business: the industry has heavy over-capacities (i.e. 20 to 30% in Europe), cities are overcrowded (i.e. 2/3 of the populations is expected to live in cities in 2025 versus 1/3 now) and governments apply restrictive regulations for safety and environment (i.e. Clean Air Act or airbag deployment act in the USA).

New cars must be cheaper, cleaner, safer, smaller.... and so smarter. One of the weak points is the harness. A typical harness represents 35 kg, 1 mile of wiring and 300 connectors costing over 1k US\$. In addition, systems require distributed intelligence with a lot of communication. A web inside the car enables flexible platforms to be built, sharing more information with less wires, connectors and sensors. In addition, only multiplexing can fit requirements with regard to safety and diagnostics.

But Automotive has harsh constraints: cost, environment and reliability which lead to specific protocols and implementations. Now vehicle multiplexing is a reality in high-end cars with up to 30 nodes in the network (Cf. figure 1) and is spreading rapidly to lower-end models presently in design.

Figure 1. Example of a car CAN network



## 1.2 THE SOLUTIONS

### 1.2.1 The Supply: Available but Noisy

The supply is a two-wire network available "for free" in all cars. But is difficult to use because of the disturbances induced by the different loads (i.e.  $12\text{ V Nominal} = 40\text{ V peak during load-dump and up to }100\text{V during short transients}$ ).

Nevertheless it is used in some applications (i.e. smart sensors) with current modulation at relatively low speed (around 100 kHz). Furthermore, studies are ongoing to move to a double supply architecture ( $42\text{Vdc}/75\text{Vpeak}$  for power loads and  $14\text{Vdc}/33\text{V peak}$  for low power) to decrease the current and the losses in the power loads. Such an approach better uses semiconductor technologies (i.e. BCD3S 1.0u for 42V and BCD5/6 0.5/0.35u for 12V) in developing low cost super-integrated nodes.

### 1.2.2 The Car Web Protocols

#### A Darwinian Selection Process.

Considering the applications' requirements, a dedicated network is obviously needed. The ideal network should use an open system, reliable if noisy, with low CPU usage, short transmission times...and all that for free. It should support different data link classes (Cf. table 1) and safe diagnosis from an external system.

**Table 1. Messages Speed Classes**

Class	Speed kbps	Application	message latency	protocol
A	<10	electric diagnostic	100 ms	CAN J1850 (GM-Chrysler) SCI/UART
B	10 to 125	display, sensor	20 ms	CAN J1850 (Ford)
C	> 125	real time	5 ms	CAN

However, the ideal network does not exist and 3 main protocols are in use: CAN, J1850 and SCI/UART. Table 3 summarizes their main characteristics.

CAN is the only protocol really designed to cover a large speed spectrum (up to 1Mbps) in noisy environments (thanks to powerful error management, multimaster architecture and physical lines interface definitions). It is now used extensively in European automotive and industrial markets. An open operating system is available (Osek/VDX) to describe the application layer (long messages, interrupt management,...). In addition, conformance tests (i.e. Dassault, IVS/C&S) are now available to validate that the microcontrollers operate in compliance to the CAN standard. Two major configurations are in use: "CAN 2.0B Active" for power train (29-bit identifier supported) and "CAN 2.0B Passive" for body and entertainment (11-bit identifier supported, 29-bit identifier tolerated).

J1850 and SCI/UART are more restricted to specific areas: Diagnostics and body in USA for J1850; Diagnostics in Europe and simple "node to node" customized networks independent from the main network for SCI/UART.

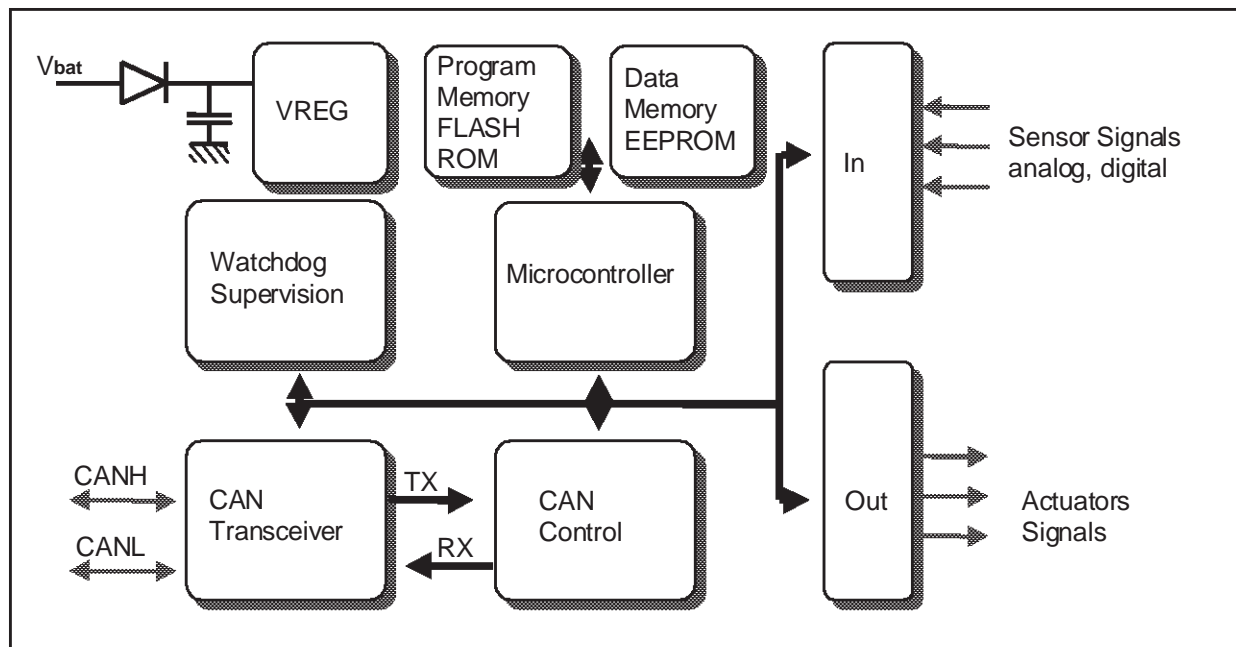
## 2 SYSTEM SOLUTIONS FOR MUX NODES

Due to the diversity of the applications, a single node architecture can not fit all the needs. Thanks to a strong partnership with major actors of the automotive industry and to a long experience in power, memories and micros, ST has developed a set of cost-effective components optimized for these applications.

### 2.1 THE CORE FOR THE NODE

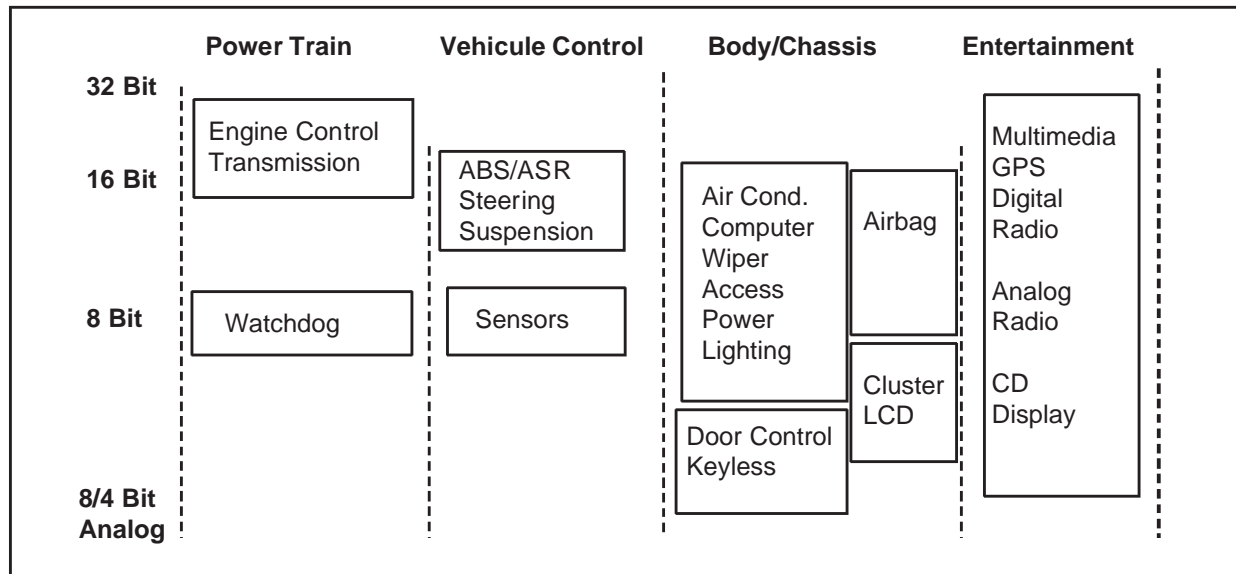
A typical MUX node (figure 2) contains a microcontroller (MCU), FLASH or ROM program memory, EEPROM data memory and power devices for physical line interface and supply management.

Figure 2. Typical node block diagram



MCU core requirement can move for the same application, i.e. body controller from 8-bit to 16-bit, depending on the application complexity (figure 3).

**Figure 3. Microcore versus application**



ST provides a complete range of MCU cores to cover this variety of needs (table 2). The products derived from these cores use a design flow fully compliant with automotive requirements: This maximizes the test coverage through VHDL description, Scan chain, JTAG and specific test flows (i.e. Iddq); Electro Magnetic Compatibility (EMC) is taken into account in the design thanks to a macrocell library optimized to minimize emission and ensure high robustness; Measurement tools are dedicated to investigate the practical EMC results; Product families are derived from a FLASH or EPROM master using the same basic technologies and CAD flow.

**Table 2. Table 2: ST MCU cores: 8 and 16-bit**

FEATURES	ST6	ST7	ST9	ST10
Architecture	Serial 8bit Accumulator	Parallel 8bit Accumulator	Parallel 8/16bit Register File	Parallel 16bit Register file
Direct Address Space	8k	64k	4M	16M
External clock speed	8MHz	16MHz	24MHz	50MHz
Instruction speed (load/move)	6.5µs	250ns	250ns	160ns
Nb of instructions	42	63	87	84
Multiply	SW	HW (1,375µs)	HW (920ns)	H/W (400ns)
Divide	SW	SW	HW (1,08µs)	H/W (800ns)
"C" instructions	No	No	Yes	Yes
DMA	No	Yes	Yes	Yes
Interrupt	5 vectors	16 vectors	128 vectors	56 vectors
Low voltage	3V	1.8V	1.8V	1.8V
Relative core area (core + itc + dma + reg. file)	< 1	1	2.5	6.5 (incl. 512B DPRAM)

(\*) ST6 / ST7 figures are given for 0.8 µ technology, ST9 / ST10 for 0.5 µ.  
(except for Relative core area where the four cores are compared in the same technology)

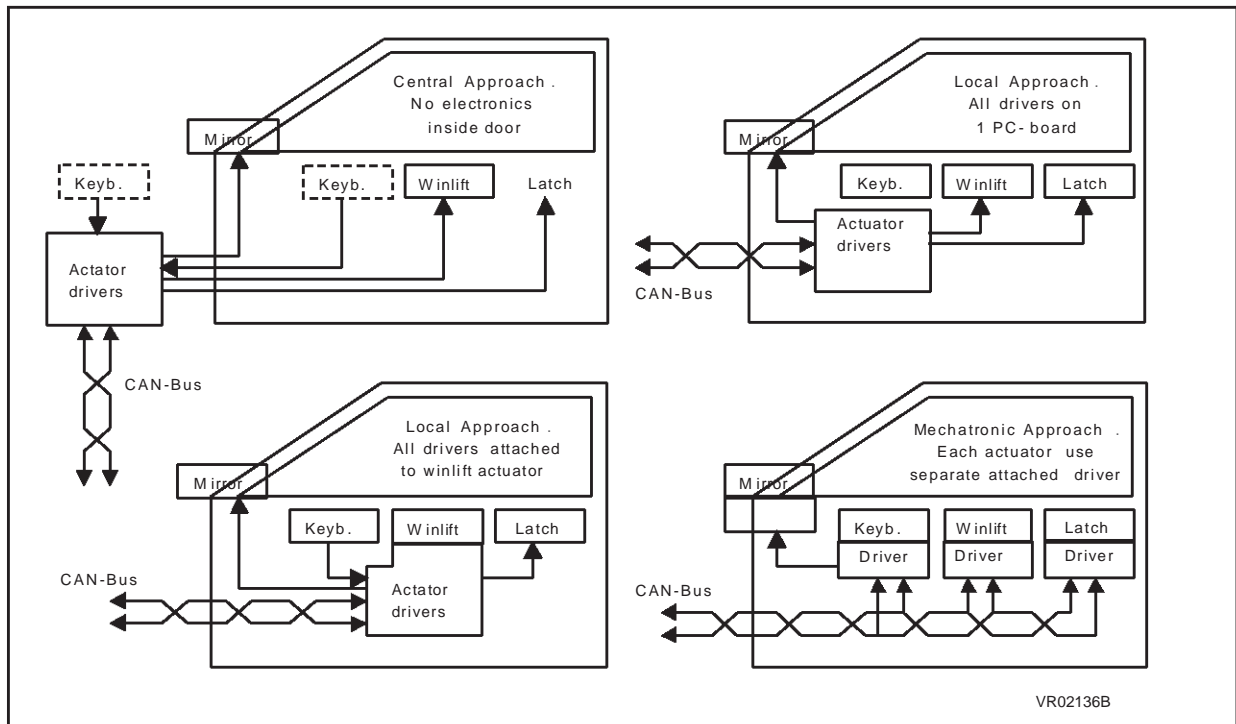
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Two microcontroller families have been designed to cover the CAN application: The ST725xx for CAN passive "low speed" applications (mainly body) and the ST10F16x for CAN active "high speed" systems (mainly power train). All these devices include also an SCI/UART to provide diagnostic capability. For J1850, the ST92F120 family has been designed. It supports the Chrysler/Delco protocol.

## 2.2 BODY CAN NODE: SOLUTIONS FOR DOOR MUX

Door multiplexing shows different possible implementations, from centralized to decentralized architecture. The following drawings present block diagrams of possible implementations from the simplest one to the most advanced Mechatronic approach (figure 4)

**Figure 4. Possible Door System partitioning**



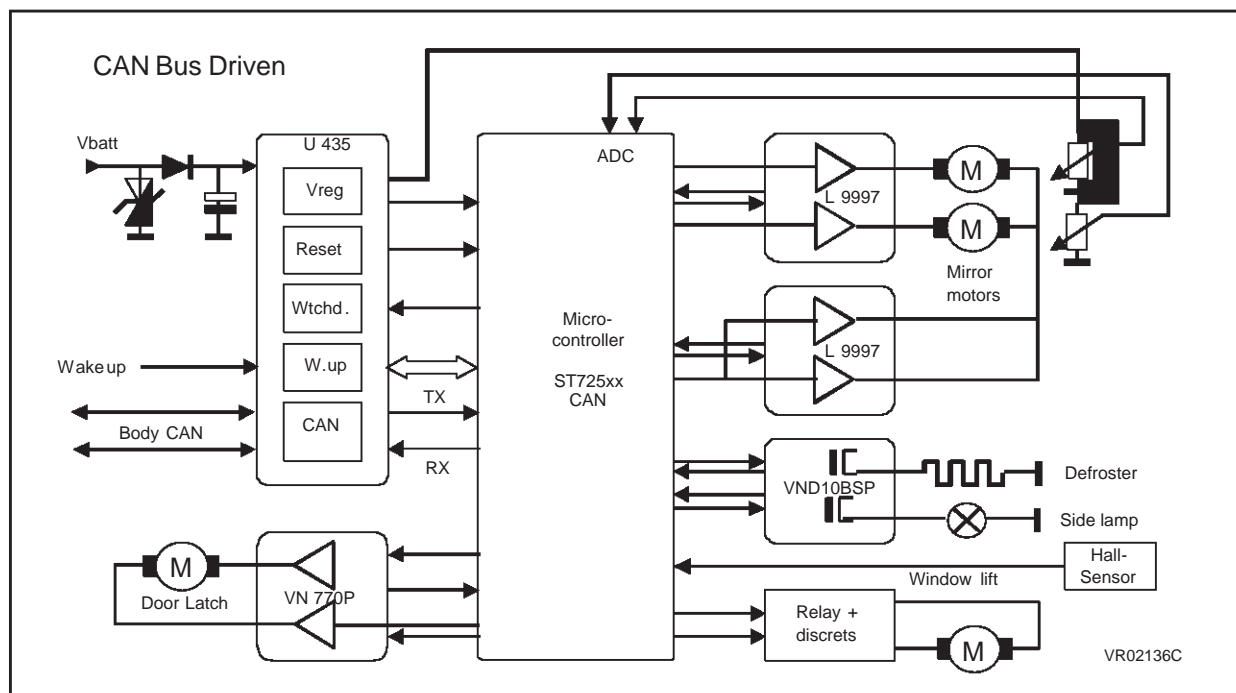
The local approaches (figure 5) are built around the ST725xx microcontroller. This family includes several subset ROM versions derived from the following master:

8-bit ST7 core, 60kbyte program, 2kbyte RAM, SPI, SCI/UART, CAN 2.0B passive, 2x16-bit Timers, 8-bit ADC, low power modes in TQFP64 package.

The other components, mainly power devices, are developed in BCD technology.

The Mirrors could be also controlled independently from the CAN network through an SCI/UART communication, if judged necessary for safety reasons.

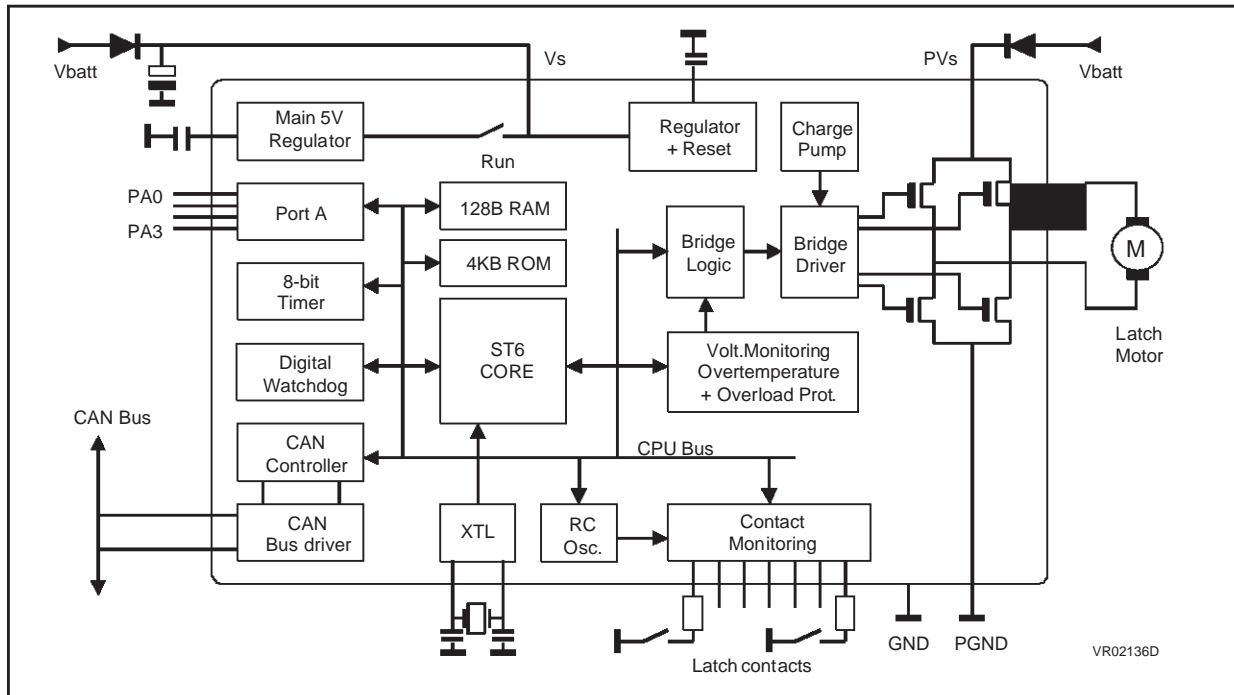
**Figure 5. A door controller on one PC-board**





The Mechatronic power latch presented in figure 6 embeds in the same SuperSmartPower (SSP) chip an 8-bit microcore (ST6) with a power stage to supply the circuit and drive the latch motor. This L9942 was developed in BCD3 (1.2um) technology. Later versions are in design using BCD5 (0.6um) and embed logic and memory features similar to the ST725xx. Such an approach is especially advantageous in applications where size is very critical.

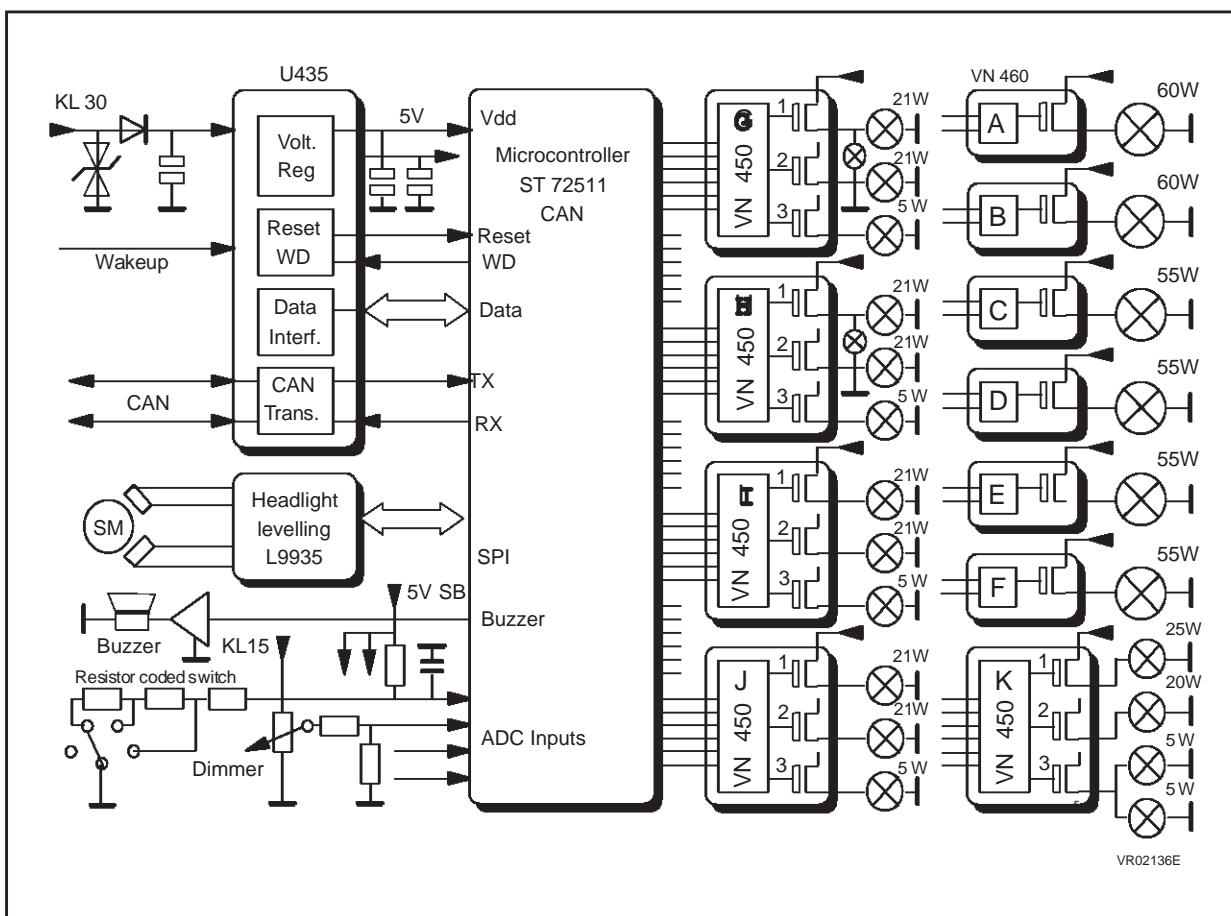
**Figure 6. Mechatronic Power Latch L9942**



### 2.3 LIMITS OF INTEGRATION: A LIGHT CENTER

The following example (figure 7) presents an example of a highly integrated lighting control center using the same master ST725xx microcontroller and dedicated power devices. Due to the power requirements, an integration with SSP is not considered. An application requiring very high voltage capability (i.e. up to 400V in Xenon Gas discharge headlight) would have a similar partitioning.

### Figure 7. Automotive light center

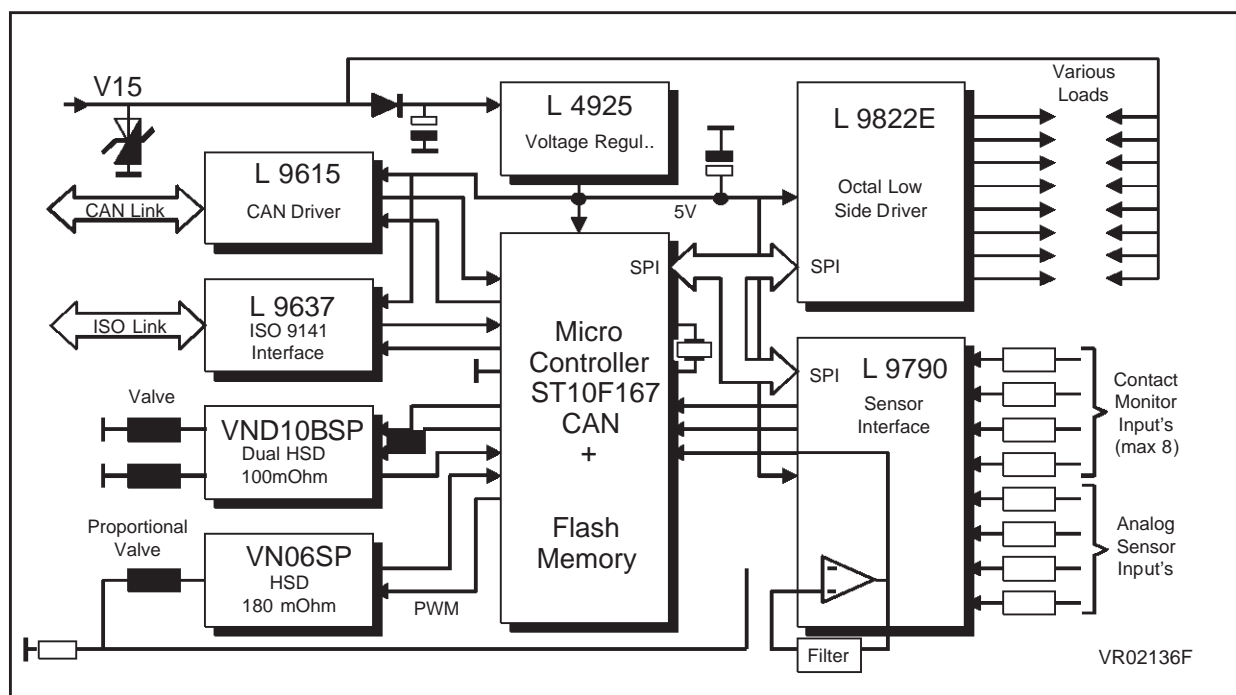


## 2.4 POWER TRAIN CAN NODE WITH 16-BIT MICROCONTROLLER

The following example (figure 8) uses an ST10 16-bit microcontroller, a dedicated high speed CAN line interface L9615 and several other power ICs. The ST10F167 includes 128kbyte FLASH (or ROM), 4kbyte RAM, SCI/UART, SPI, CAN 2.0B active, 2x16-bit Timer Blocks, 8 channel CAPCOM. It is housed in PQFP144.

Using the ST10 instead of the ST7, the processing speed is more than doubled and a CAN Active protocol can be managed. So this configuration is adapted to applications requiring fast communication speed and heavy calculation.

**Figure 8. Automatic Transmission Unit**



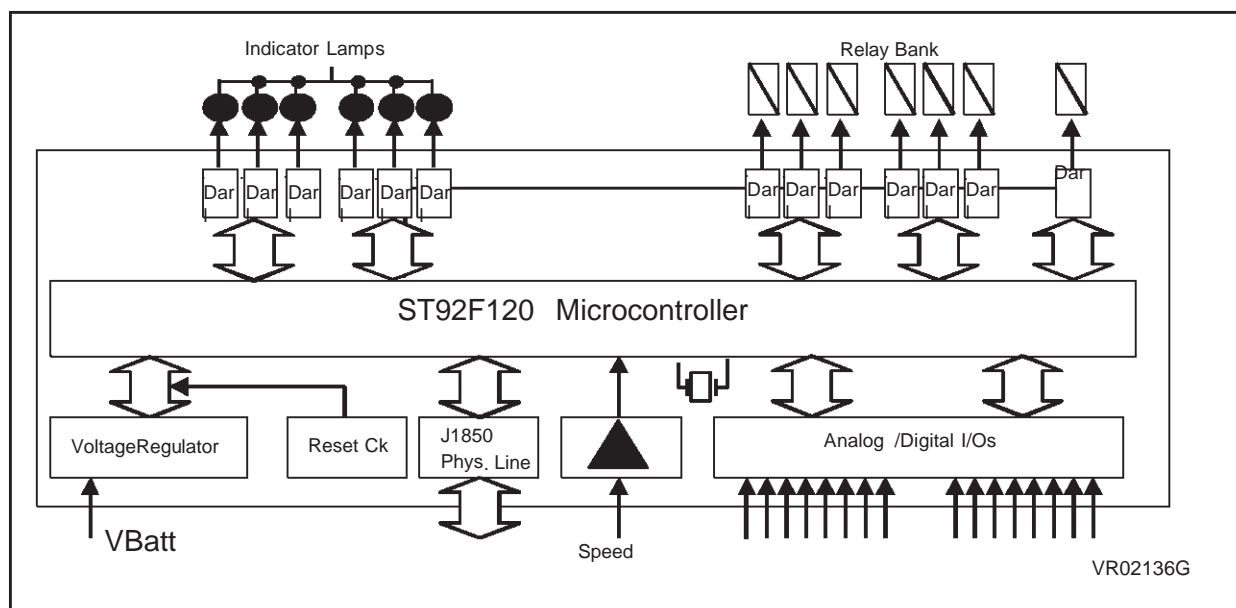
### 2.5 A BODY CONTROLLER WITH J1850

The ST92F120 microcontrollers family is used for body J1850 applications (figure 9). This family includes several subset FLASH versions derived from the following FLASH master:

8/16-bit ST9 core with DMA capability, 128kbyte FLASH, 2kbyte RAM, 1xSPI, 2xSCI/UART, J1850 Chrysler/Delco, 1xI2C, 6x16-bit Timers, 16 channels 8-bit ADC, low power modes in TQFP80/100 package. An EEPROM of 1kbyte is embedded for safety data storage.

Later versions of the ST725xx with J1850 cell are presently in discussion for applications where the ST9 core features are oversized.

**Figure 9. Body controller with J1850**

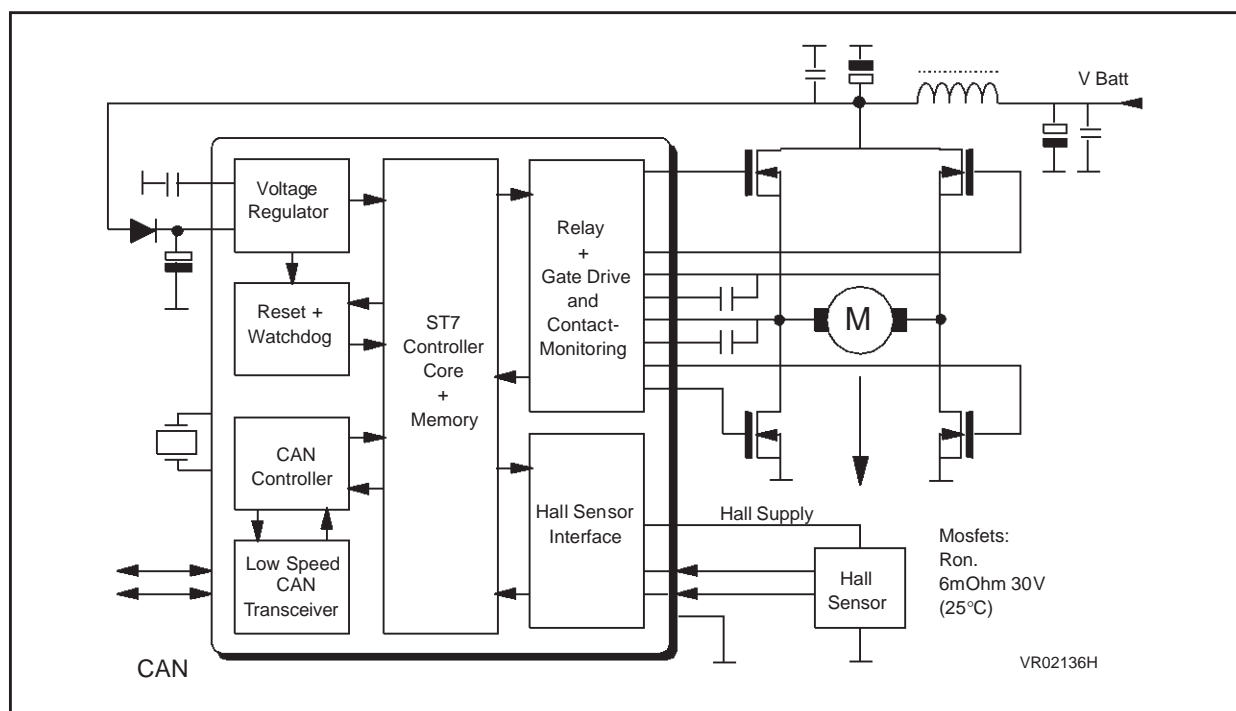


## 2.6 SUPER INTEGRATION

### From Super Smart Power to Distributed Multimedia

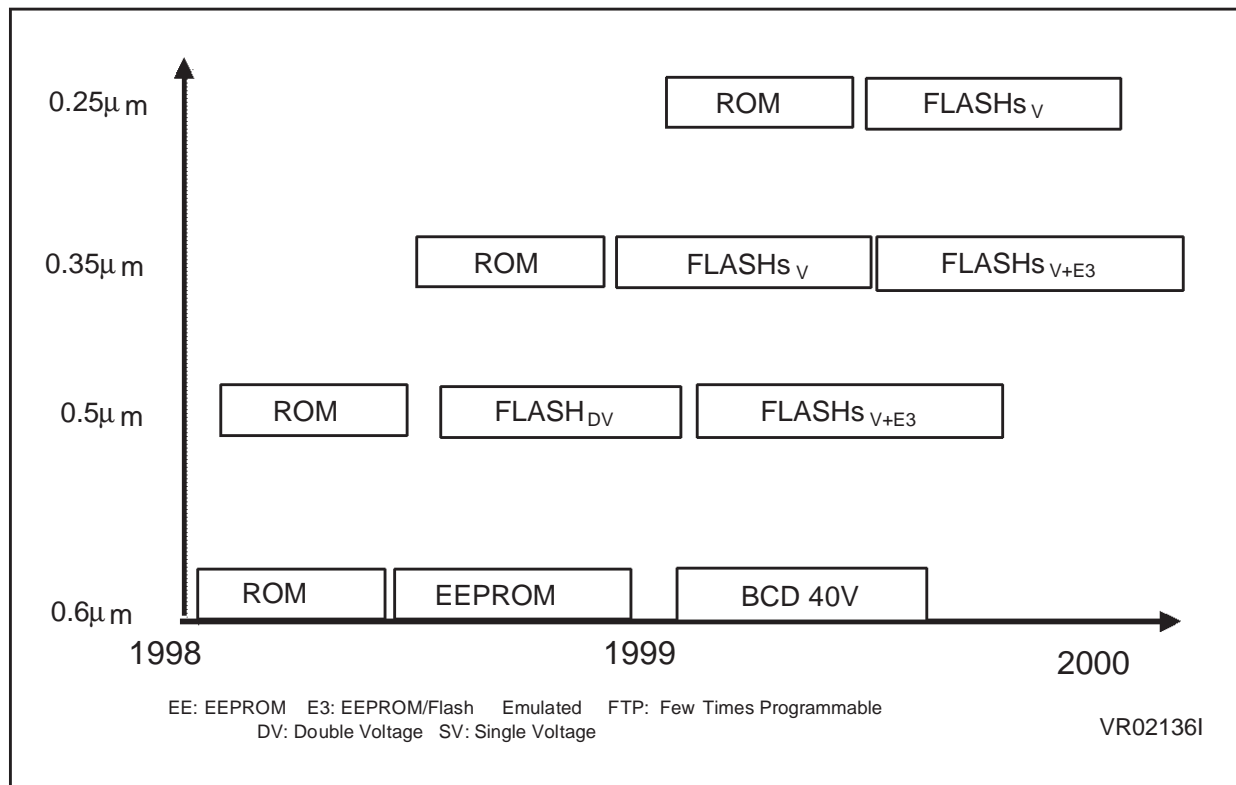
The race for integration is not finished. For low and medium communication speeds (up to 1Mbps) new solutions based on Super Smart Power enable node size reduction by integrating together the physical line interface, the supply and the logic/microcontroller. Products in 0.6um lithography are now in design and the technologies for 0.5um and lower are in development. With these thin lithographies similar to the one uses for standard MCUs, logic and memory features similar to the ST725xx can be embedded (figure 10).

**Figure 10. Embedding capability of a SSP ST7 device**



FLASH embedded memory is also a major requirement in automotive to ensure programming capability at the production line and to reprogram the micro during the lifetime of the car. ST10 FLASH microcontrollers are in full production in 0.5um lithography and samples in 0.35um are available (figure 11). This FLASH process is derived in the 3 versions: a "Full FLASH" enabling above 100k cycles of programming (i.e. for Engine Management control), a "Few Times Programmable" version using a slightly simplified and cheaper process variation (i.e. for body applications) and an upgraded version to embed EEPROM emulation capability (i.e. for safety sensitive applications).

Figure 11. Embedded FLASH roadmap



New applications such as Distributed Multimedia Systems require even higher communication speed and so faster microcontroller cores. To support such applications, system-on-chip solutions are now in design. They embed different 16 and 32-bit cores from ST20 (25/100 MIPS), ST30 (50/150 MIPS), ST40 (200/400 MIPS) and ST50 (64-bit cpu).

## CONCLUSION

Networking is a major trend in our daily life and in system optimisation. Cost effective solutions fully compliant with automotive constraints are now available, based mainly on the CAN protocol.

They are built around high voltage devices with 8 and 16-bit microcontrollers. ST725xx or ST92F120 (FLASH) are used now for low speed body or radio applications and ST10F167 (FLASH) for high speed CAN power train or audio systems.

In partnership with major players of the automotive industry, the next step towards system-on-chip is in design with additional FLASH-Micros, Super Smart Power and 32/64-bit micro circuits.

Table 3. Main characteristics of the most used car mux protocols

Peripheral	SCI/UART	J1850	CAN
Class	A	A-B	A-B-C
<b>Architecture</b>	Open Asynchronous Few nodes Masterslave Error detection: checksum	Open Asynchronous Multimaster Bus access: bit arbitration Error detection: CRC Priority on highest header	Open Asynchronous Multimaster Error Management Bus access by bit arbitration Priority to dominant bit (0)
<b>Protocol</b>	SCI/UART NRZ (3) Speed Data: 9.6/10.4kbps Speed Address: 5 bps Data: 7bit Frame: 10 bit	CSMA/CR <sup>1</sup> Ford: PWM 41.6kbps Chrysler/GM: VPM 10.4kbps Data: 0/12 byte Frame: 6 bit	CSMA/CA <sup>2</sup> NRZ <sup>3</sup> Toggling after 5 success bit Speed up to 1Mbps Data: 0/8 byte Frame standard: 0/64 + 47 bit (up to 2048 addresses) <sup>4</sup> Frame extend: 0/64 + 67 bit (500M addresses) <sup>4</sup> 5 error messages <sup>5</sup>
<b>Software (Typical)</b>		Basic configuration: 2kROM-64RAM	Basic configuration: 4k ROM-64 RAM Full configuration: All by H/W
<b>Physical Layer</b>	Diagnosis ISO9141: 2 pins Data: K pin (Rx/Tx) Address: L pin (Rx) Levels: Referred to Vbatt	Ford: 2 wires Referred to 6.25V differential Xler/GM: 1 wire Referred to 20V max differential Max nodes number: 32 Max distances: 40m	2 wires (1 in failure mode/Low-speed) Levels referred to 5V (and Vbatt in Standby_low speed) Max nodes number: 30 (high speed), 20 (low speed) Max distances: 40m @ 1Mbps, 500m @ 125kbps.
<b>Datalink Physical Standards</b>	In car MUX: No standard  Diagnosis: ISO9141 (Europe) OBD2 (America)	In car MUX: SAE J1850 SAE J2178 ISO 14230-4 Diagnosis: OBD2 J1979 J2190	In car MUX Europe: ISO11898 (>125 kbps, transceiver) ISO11519 (<125 kbps, transceiver) In car MUX America : SAE J2284 (high speed/2 wires) SAE J2411 (low speed/1 wire) SAE J1939/ISO11783 (truck, < 250kbps) Diagnosis: ISO15765, ISO11898
<b>Application Open protocols</b>	None	None	Real time O/S: OSEK/VDX Industry: standard frame only: Devicenet (AllenBradley) SDS (Honeywell) CANOpen (CIA)
<b>Running applications</b>	In car MUX: nodes isolated from main web for safety (i.e. mirrors) or speed (i.e wiper) purpose. Diagnosis: Std in Europe Industry: used extensively	In car MUX (America): average 3 to 5 nodes up to 36 nodes  Diagnosis (America) Industry: none	In car MUX (Europe): average 3 to 5 nodes, up to 36 nodes around 20M nodes in 1998 Industry: Devicenet and SDS (USA), CANOpen (Europe)

- Notes: <sup>1</sup> CSMA/CR: CarrierSense, Multiple Access, Collision resolution  
<sup>2</sup> CSMA/CA: CarrierSense, Multiple Access, Collision avoidance  
<sup>3</sup> NRZ: NonReturn to Zero  
<sup>4</sup> CAN frames identifier: Standard: 11bit, Extended: 29 bit  
A version: std frame only, error with extended frames  
B passive: std frame messages, no error if extended frames  
B active version: std and extended frame messages  
<sup>5</sup> Error messages in 5 cases: bit, bit stuff, message frame, message CRC, message acknowledge errors.

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