ST10X167/F168

Reducing Analog-Digital Conversion Error

APPLICATION NOTE

The ST10X167/F168 contains an Analog / Digital Converter with 10-bit resolution, 9.7 µs conversion time, a sample & hold circuit on-chip, ESD protected analog inputs and a “Total Unadjusted Error” of ±2LSB. An automatic self-calibration adjusts the ADC module to changing temperatures or process variations, giving high performance across the whole automotive temperature range.

This application note identifies the causes of ADC error and gives solutions to optimize ADC performance.

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1 Sources of ADC error

Sources of ADC accuracy error are classified into 3 categories:

- Analog input signal error
- Input overload error
- Reference voltage error

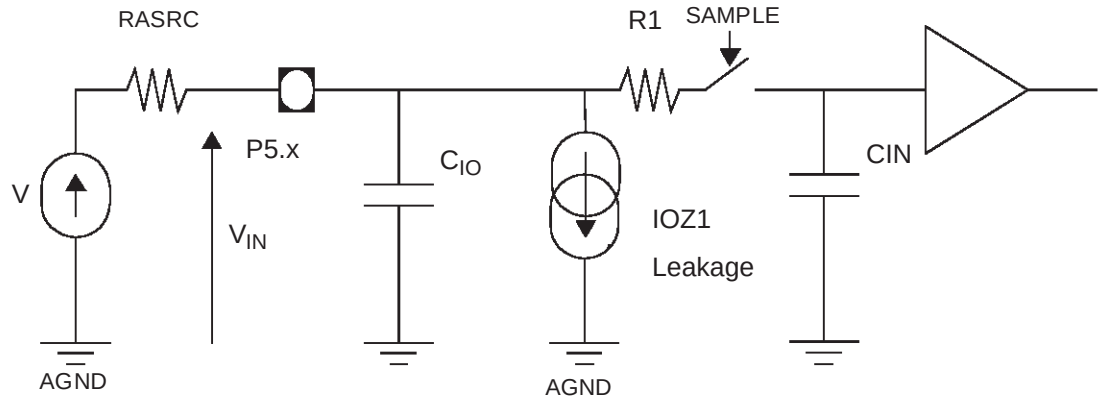
Each of these categories is described in the following sections.

1.1 Analog input signal error

Analog input signal error can be created by poor matching of the source internal resistance with the ADC input parameters, either caused by,

- voltage drop in the voltage source resistance due to input leakage current,
- or by poor charging of the ADC internal capacitance (Cin).

Analog input error can also be caused by noise from the analog input signal. This section described each of these causes.



- I_{OZ1} (Input leakage current Port5): max +/- 500 nA (test Condition: 0.45V<VIN<VDD)
- C_{IO} (Pin capacitance Port5): max 10pF (test Condition: f = 1 MHz, TA = 25 C, guaranteed by design characterization)
- C_{IN} (ADC Internal capacitance): max 23pF (guaranteed by design characterization)
- R1 (series input resistance): max 1.5k Ohms (guaranteed by design characterization)

The parameter defined in the datasheet is (Cio + Cin).

Figure 1 Source internal resistance errors

Refer to *Figure 1* for a schematic of source internal resistance errors.

Voltage drop in the source resistance: The error generated by the voltage source internal resistance is:

$$error(LSB) = \frac{R_{SOURCE} \times I_{0Z1}}{V_{AREF} - V_{AGND}} \times 1024$$

For example: A source resistance of 15Kohm and a specified leakage current (I_{OZ1}) of +/- 500nA will cause a voltage error of +/- 7.5mV or +/- 1.5LSB.

Refer the latest product data sheet for the value of $\mathbf{I_{OZ1}}$.

Note *Input leakage current is caused by parasitic current at input pin protection; this protection is necessary to protect the device against ESD (Electrical Static Discharge) and against overload.*

Poor charging of the ADC internal capacitance: During the sample time, the input capacitance (Cio and Cin) must be charged/discharged by the external source. The internal resistance of the source must allow the capacitance to reach its final value before the end of sample time: see Figure 2.

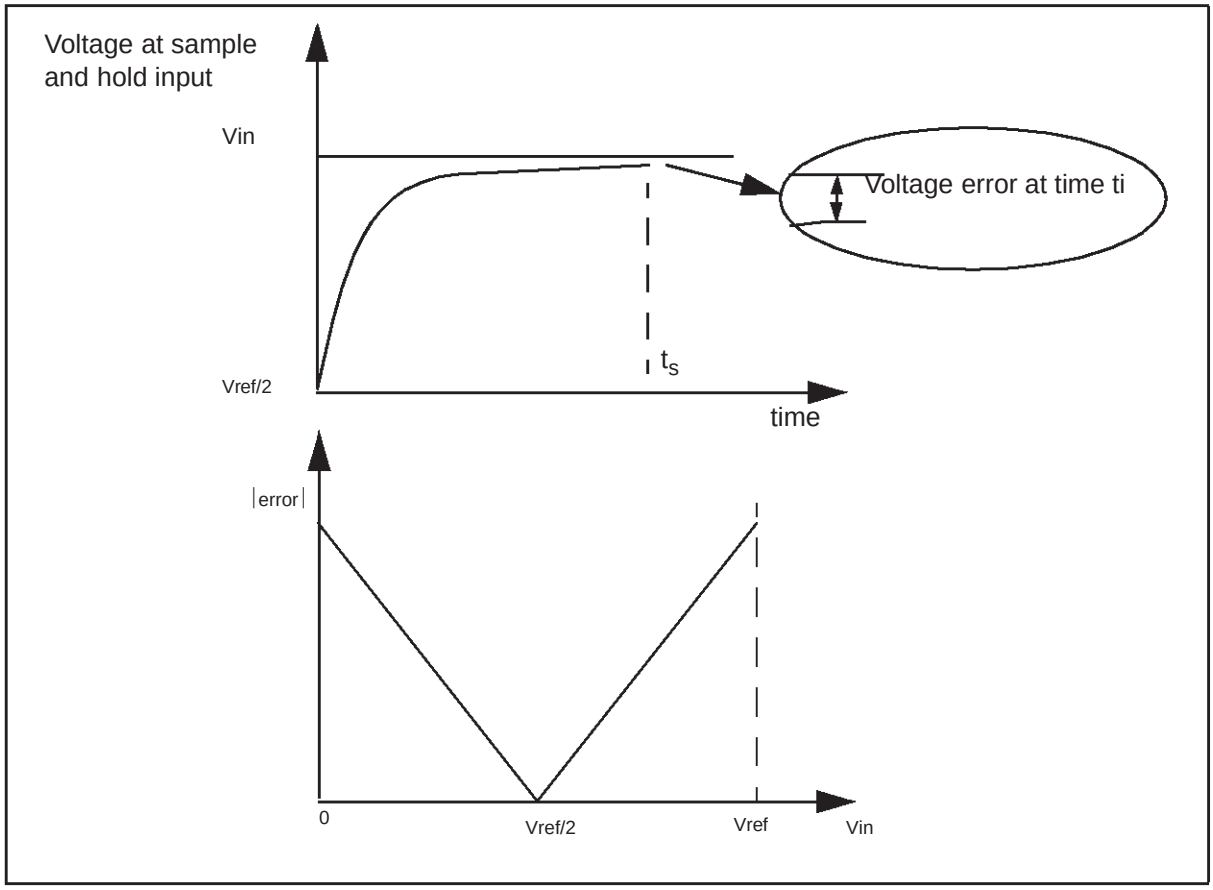


Figure 2 Possible error due to input capacitance charging

If this does not happen, i.e. if the source resistance is mis-matched to the sample time, a voltage loss will occur at the sample and hold stage. This voltage loss causes an accuracy loss when increasing or decreasing the input voltage from Vref/2 (hold capacitor is pre-charged to Vref/2 before sampling to reduce charge/discharge time).

The error is calculated by the formula:

$$\dot{Max}error(LSB) = \frac{1}{2} \times 1024 \times \exp(-t_s/R \times C)$$

Where: T_S = sample time in µs, R = R_{SOURCE} + R1 in Ω, C = Cin + Cio in µF. For example:

Since the error is proportional to the difference between Vin and Vref/2, the effect produces a non-linearity in the conversion of large-amplitude signals. In practice, if Ts>7RC, the maximum error is reduced to <1/2 LSB (<0.05%).

Errors due to noise from the input signal: The sample and hold circuitry is not designed to filter the input analog signal. Noise at the input signal will cause input voltage variation and, therefore, accuracy loss.

1.2 Input overload errors

These errors are caused by input overload. During overload, internal protection-diodes sink current to reduce the overload voltage. Because of the close proximity of the internal protection-diodes and the ADC circuitry, the ADC performance is affected.

The ST10C167 accepts up to 10mA of input overload current while guaranteeing a Total Unadjusted Error (TUE) of +/- 2LSB (refer to the product Data sheet for values).

Overload above the specified limit causes ADC accuracy loss and may damage the circuit.

1.3 Reference voltage errors

The accuracy of the conversion is obviously linked to the accuracy of the reference voltage.

While noise and/or voltage variations are a well known source of error, internal resistance is another source of error from the reference voltage.

During the conversion, the ADC internal capacitance must be repeatedly charged or discharged. The internal resistance of the reference voltage must allow the capacitance to reach its correct voltage within the conversion time (see Figure 2). A mis-match between the conversion time and reference voltage internal resistance will cause accuracy errors.

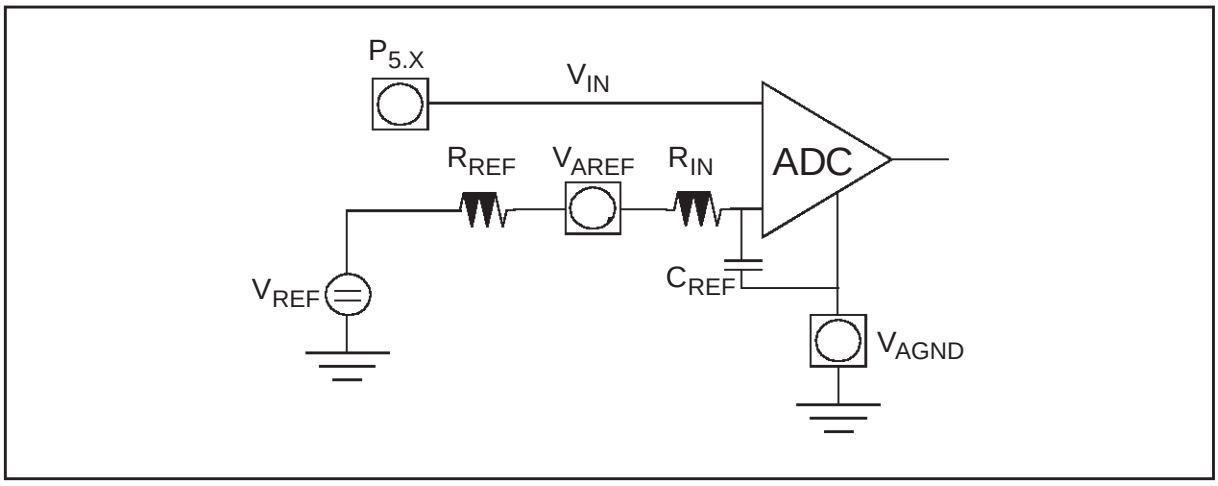


Figure 3 Simplified circuit for analog reference voltage

2 How to minimize error

2.1 Optimize the input signal

There are three possible optimizations:

Minimize the total source impedance seen by the ST10: This means choosing sensors with low output impedance (not always easy for some types of sensor), and minimizing the serial resistance of any protection devices between the analog source and the input pin (while still providing a voltage protection level compatible with the circuit specification).

Match the sample time to the analog source impedance: Use the formula that relates sample time to source internal resistance (given in the ST10 data sheet) to match the source resistance to one of the available sample times.

For example: For a source impedance of 10kOhms, and given

$$R_{ASRC} = t_s / 330 - 0.25$$

then the minimum sample time is:

$$t_s = 330 \times (R_{ASRC} + 0.25)$$

$$t_s = 3380ns(min)$$

Note *This formula includes a safety factor of 10, therefore from the equation for error on page 4, dynamic errors are ≈0.02LSB.*
Furthermore, R_{ASRC} is the total source impedance seen by the device and, therefore, includes any protection components.

Reduce noise at the input pin: Add an external RC filter (with attention to the source internal resistance). Compute the average value of different samples in the software routine.

2.2 Reduce input overload error

Because errors are induced from overload current going into/out of the integrated protection diodes, optimizations minimize this current in 3 ways:

Minimize the over-voltage at the analog source: The possible optimizations depend on the user application, typically, they involve the addition of Zener diodes or transils. For component selection, refer to ST-On-Line Discrete Devices/Protection Circuit data books.

Minimize the over-voltage at the ST10 analog input pins: Either, add protection diode(s) or transil(s), or add a serial resistor. CAUTION: the addition of a serial resistor increases the source internal resistance and, therefore, may impact maximum conversion speed.

Synchronize ADC conversion with analog transitions: Where possible, avoid carrying out conversions when analog inputs are scheduled to go into overload conditions (at least, during the transition phase).

2.3 Reference voltage error reduction

The possible optimizations are:

Reference voltage noise: Reduce noise by careful design; PCB routing and de-coupling of the reference voltage:

- Place the analog source as close as possible to the V_{AREF} pin.
- Avoid routing any high frequency/high amplitude signals near to the analog source.
- Make sure that the Voltage Reference source presents a low impedance from dc to well above the max. sampling frequency ($1/t_c$): see Figure 4.

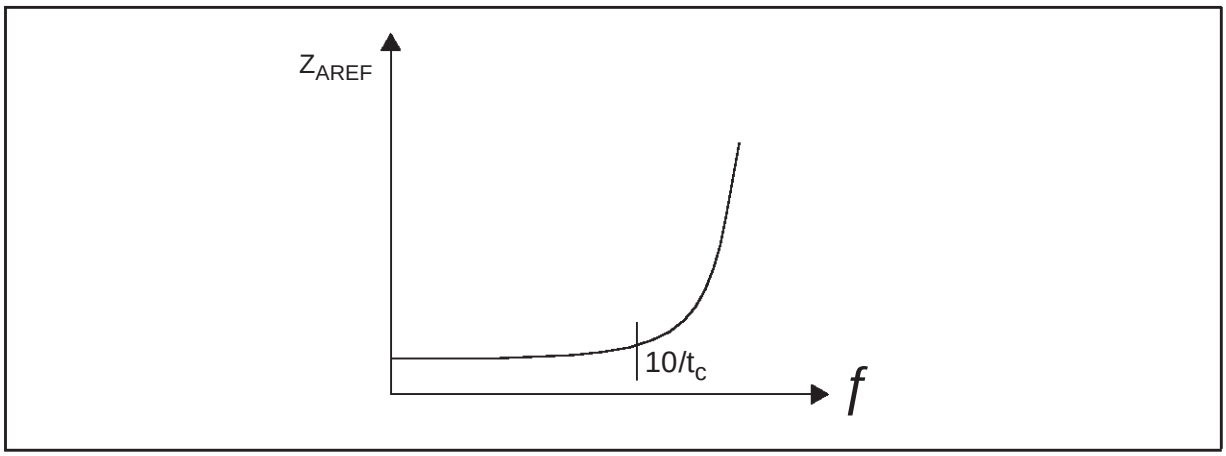


Figure 4 Analog reference source - impedance characteristics

Match the reference voltage internal resistance to conversion time: Use the formula that relates conversion time to source internal resistance (given in the ST10 data sheet) to match the reference voltage to one of the 3 available conversion times.

For example: given

$$R_{AREF} = \frac{t_{cc}}{165} - 0.25$$

then the max. source impedance for t_{cc} of 1200ns is:

$$R_{AREF} = \frac{1200}{165} - 0.25$$
$$= 7kOhms(max)$$

Note This should hold up to f=10/tc, so if $t_c \approx 20\mu s$, $|Z_{AREF}| < 7k\Omega$, up to 500kHz.

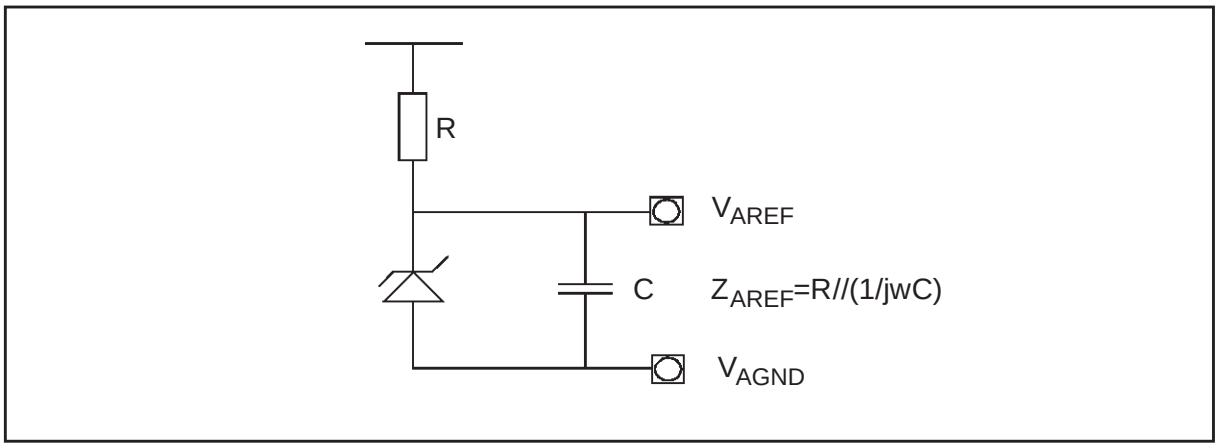


Figure 5 Typical analog reference circuit

Note Figure 5 shows a commonly used circuit for the analog reference voltage.

3 Appendix - Definitions

LSB: Least Significant Bit.

Resolution: defines the smallest input voltage change required to increment the output of the ADC between one code and the next adjacent code. Resolution is a design parameter rather than a performance specification; it says nothing about accuracy. Resolution is either expressed in percent of the full-scale, or in binary bits.

Accuracy: defines the worst case difference between the actual input voltage and the full-scale weighted equivalent of the binary output code. For ST10 devices, the Total Unadjusted Error describes the maximum sum of all errors intrinsic to the ADC.

Intrinsic errors: are errors intrinsic to the ADC itself, such as: quantizing error, scale error, offset error, hysteresis error, linearity error. For simplicity and ease of use, the ST10 ADC specification gives the sum of all intrinsic errors (Total Unadjusted Errors).

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